標題	***參考設計報告：使用 LinkSwitch™-HP LNK6766E 的 30 W 單輸出返馳式轉換器***
規格	90 VAC ～ 265 VAC 輸入；12 V、2.5 A 輸出
應用	轉換器
作者	應用工程部門
文件編號	RDR-313
日期	2012 年 9 月 14 日
修訂	1.2

<u>摘要與功能</u>

- 一次側調節隔離式返馳式轉換器，調節範圍不超過 ±5%。
- 132 kHz 切換頻率，可減小變壓器和輸出濾波器的尺寸。
- 滿載連續導通模式操作，可改善效率並降低輸出電容器漣波電流
- 多重模式操作使滿載範圍內的效率達到最大
- 230 VAC 條件下功耗小於 30 mW。
- 廣泛的保護功能，包括 OVP、OTP、電壓啓動/關閉、線電壓過壓和喪失調節功能 (自動重新啓動)
- 符合 EN-550022 和 CISPR-22 B 級傳導性 EMI (5 dB 餘裕) 標準。
- 符合 IEC61000-4-5，1 kV / 2 kV 突波標準

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目錄

重要附註：
雖然此電路板的設計滿足安全隔離需求，但其工程原型未經相關機構核准。因此，執行所有測試應使用隔離變壓器才能提供 AC 輸入給原型板。

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1 簡介

本報告說明通用電壓輸入、12 V、30 W 隔離式返馳式轉換器，其採用 LinkSwitch-HP IC 系列中的 LNK6766E 裝置。內容涵蓋電源供應器的完整規格、詳細電路圖、打造供電器的完整物料清單、各種變壓器文件，以及最重要的電氣波形的測試資料和波形繪製圖。

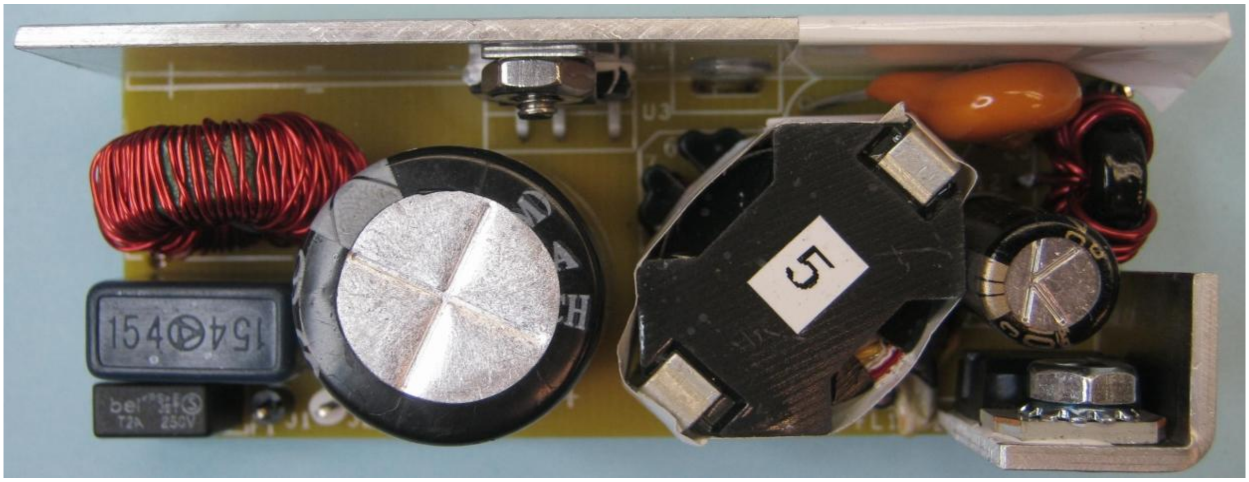

Figure 1 – Prototype Top View.

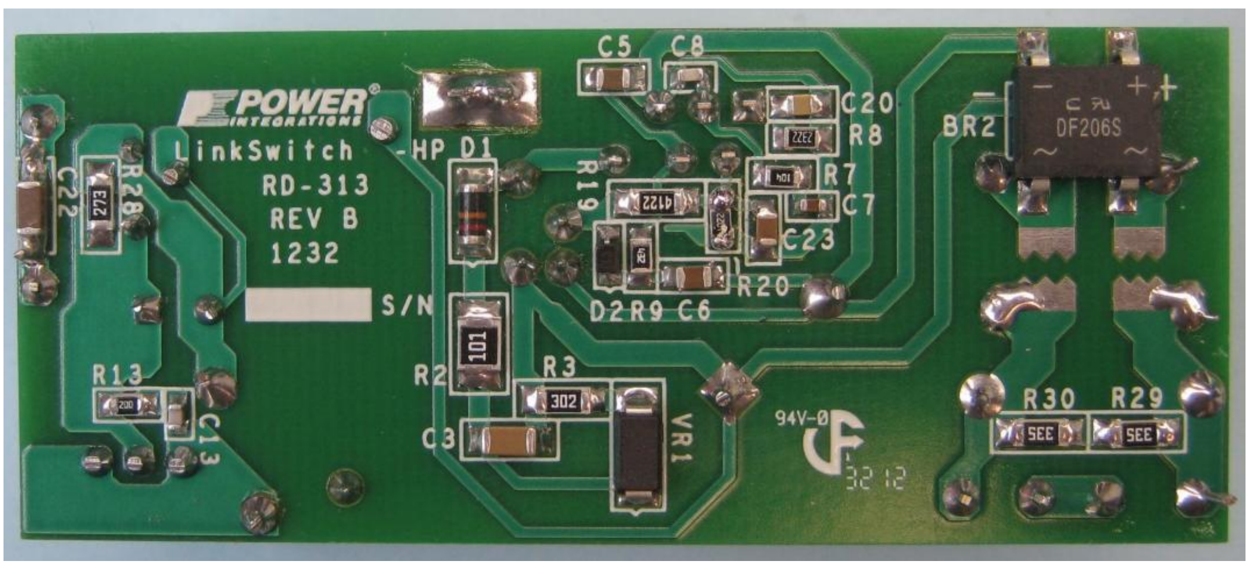

Figure 2 – Prototype Bottom View.

2 電源供應器規格

下表列出可接受此設計的最低效能。實際效能列在結果部分。

說明	符號	最小值	類型	最大值	單位	註解
輸入						
電壓	V_{IN}	90		265	VAC	雙線 – 無 P.E.
頻率	f_{LINE}	47	50/60	64	Hz	
待機輸入功率				30	mW	230 VAC
輸出						
輸出電壓	V_{OUT}	11.4	12	12.6	V	
輸出漣波電壓	V_{RIPPLE}			120	mVpp	20 MHz 頻寬，含穩態負載
輸出電流	I_{OUT}	0.0		2.5	A	
過衝電壓	$V_{OVERSHOOT}$			18	V	待機負載和 AC 輸入週期
總輸出功率						
連續輸出功率	P_{OUT}	0		30	W	
效率						
滿載效率	η	85			%	90 VAC 和滿載
環境						
傳導性 EMI		符合 EN55022B 標準				5dB 餘裕
安全		設計符合 IEC950，UL1950 第 II 級標準				
突波	**DM**	1			kV	1.2/50 µs 突波，IEC 1000-4-5，串聯阻抗： 差模：2 Ω 共模： 12 Ω
	CM	2				
ESD	**空氣**	-15		15	kV	在輸出連接器上空氣放電
	接觸	-8		8	kV	在輸出連接器上接觸放電
環境溫度	T_{AMB}	0		40	^{o}C	自然對流，海平面

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3 電路圖

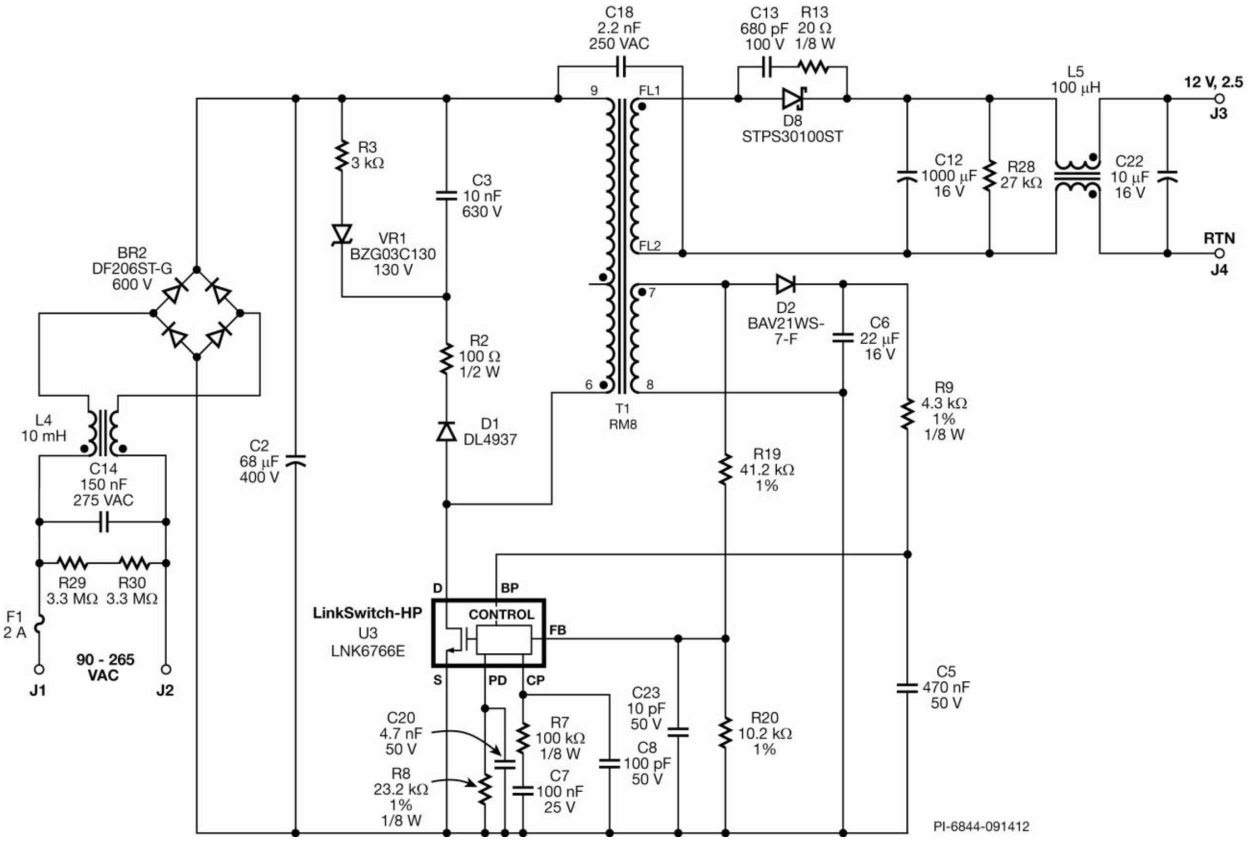

Figure 3 – Schematic.

4 電路說明

4.1 輸入整流和濾波

橋式整流器 BR1 會對 C2 過濾的 AC 輸入進行整流。電感器 L4、C14 和 C2 會用於削減差模和共模傳導性 EMI。遮蔽技術用於變壓器 T1 的構造中，以減少共模 EMI 位移電流。此濾波器排列、遮蔽技術加上 IC 的頻率抖動功能，爲這個採用 Y 電容器和一次側 RZCD 箝位電路的解決方案提供優異的 EMI 效能。

4.2 LinkSwitch-HP 一次側

LNK6766E 裝置 (U3) 將振盪器、誤差放大器和多模共用電路、啓動和保護電路，以及高壓功率 MOSFET 全都整合到一個單晶片 IC 上。

變壓器的一側連接到高壓匯流排，另一側則連接到 U3 的汲極 (D) 接腳。在開始切換週期時，控制器會開啓功率 MOSFET，逐漸增加一次側繞組中的電流，藉此將能量儲存在變壓器的鐵芯。當電流達到內部誤差放大器 (補償 (CP) 接腳電壓) 的輸出端所設定的限制臨界值，控制就會關閉功率 MOSFET。由於變壓器繞組的相位變化和輸出二極體的方向，儲存的能量會接著在二次側繞組上產生電壓，使輸出二極體變爲正向偏壓，然後儲存的能量就會輸送到輸出電容器。

連接到旁路 (BP) 接腳的電容器 C5 (0.47 μF) 會設定過壓保護 (OVP) 和鎖定與喪失調節過溫保護 (OTP)，以便在達到指定的關閉期間 (通常爲 1500 ms) 之後自動嘗試重新啓動。

4.3 一次側 RZCD 箝位

二極體 D1、VR1、C3、R2 和 R3 會形成 RZCD 突波吸收器，以用於限制 LinkSwitch-HP 上的電壓應力。所以，265 VAC 條件下的汲極電壓峰值會限制爲低於 540 V，這樣與汲極電壓 (BV_{DSS}) 650 V 之間就有很大的餘裕。積納二極體 VR1 會防止電容器 C3 完全放電每次切換週期，以降低待機功耗。

二極體 D1、R2、VR1、C3、R5 和 R6 會形成 RCD 突波吸收器，以用於限制 LinkSwitch-HP 上的電壓應力。所以，265 VAC 條件下的汲極電壓峰值會限制爲低於 580 V，這樣與汲極電壓 (BV_{DSS}) 700 V 之間就有很大的餘裕。

4.4 輸出整流

對 12 V 輸出進行整流是由二極體 D8 所提供，濾波則由電容器 C12、C21 及電感器 L5 和 L22 提供。R13 和 C13 形成的突波吸收器提供高頻率過濾，以改善 EMI。

4.5 外部限電流設定

最大週期性電流限制是由連接至程式 (PD) 接腳的電阻器 R8 所設定。本設計中的 23.2 kΩ 電阻器將最大限電流設爲 LNK6766E 預設限電流的 60%。

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4.6 回授和補償網路

輸出電壓在返馳期間，會透過偏壓繞組和分壓電阻器 (R19 和 R20) 進行感測。感測到的輸出電壓會與回授 (FB) 接腳臨界值進行比較，以便調節輸出，或在偵測到過壓情況時停止切換 (OVP)。一次側調節解決方案不僅可降低系統成本，還可以改善系統使用期限，因爲採用 LinkSwitch-HP 設計的電源供應器完全不需要光耦合器 (會明顯降低電源供應器的使用期限)。

分壓電阻器 R19 和 R20 也會用於在整合功率 MOSFET 啓動期間，間接監控匯流排電壓。啓動時，此 IC 只會在匯流排通常達到 100 V (電壓關閉臨界值) 時才會啓用切換。假設例如在電壓關閉情況下，匯流排電壓下降至低於 40 V 典型值，則裝置會停止切換 (電壓關閉保護)。當匯流排電壓達到過大等級 (例如因爲線間突波導致這情況)，則裝置會停止切換。此外，週期性電流限制會在線上補償，以限制可用的過載功率。如需進一步詳細資訊，請參閱裝置規格型錄。

在 FB 接腳處感測到的電壓會在 CP 接腳處產生控制電壓。電阻器 R7 和電容器 C7 和 C8 會用於控制迴路補償。一次側工作峰值電流和工作切換頻率由 CP 接腳電壓所決定。

5 PCB 佈局

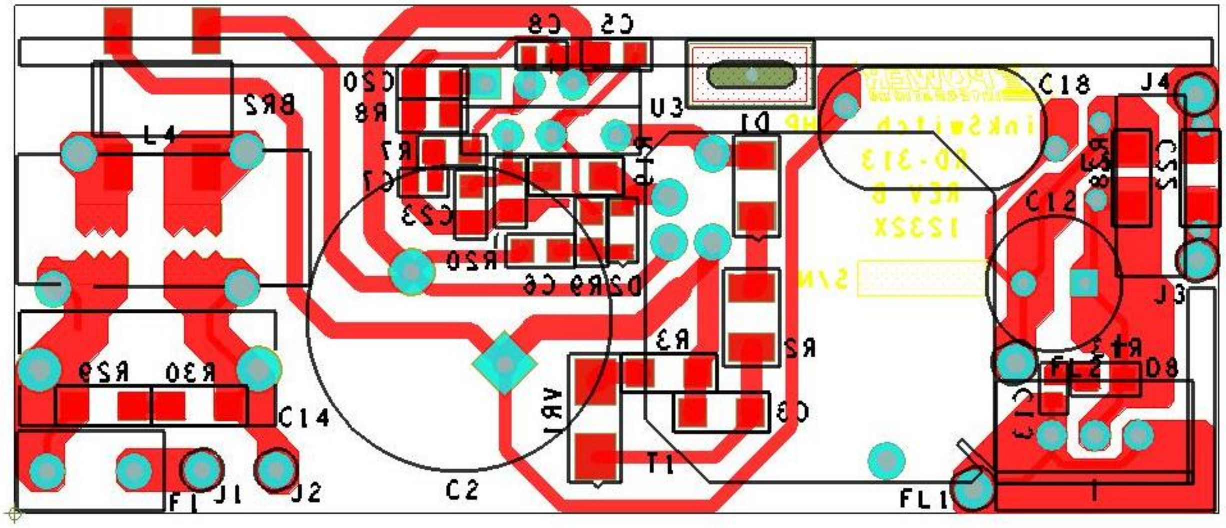

Figure 4 – PCB Top/Bottom Side 2.76" (70.1 mm) x 1.16" (29.4 mm).

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6 物料表

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR2	600 V, 2 A, Bridge Rectifier, SMD, DFS	DF206ST-G	Comchip Technology
2	1	C2	68 μF, 400 V, Electrolytic, (18 x 20)	ERT686M2GL20RR	Samxon
3	1	C3	10 nF, 630 V, Ceramic, X7R, 1206	C1206C103KBRACTU	Kemet
4	1	C5	470 nF, 50 V, Ceramic, X7R, 0805	GRM21BR71H474KA88L	Murata
5	1	C6	22 μF, 16 V, Ceramic, X7R, 0805	C2012X5R1C226K	TDK
6	1	C7	100 nF, 25 V, Ceramic, X7R, 0603	VJ0603Y104KNXAO	Vishay
7	1	C8	100 pF 50 V, Ceramic, NPO, 0603	CC0603JRNPO9BN101	Yageo
8	1	C12	1000 μF, 16 V, Electrolytic, Low ESR, 8 x 20)	16MCZ100M8X20	Rubycon
9	1	C13	680 pF 100 V, Ceramic, NPO, 0603	CGA3E2C0G2A681J	TDK
10	1	C14	150 nF, 275 VAC, Film, X2	LE154-M	OKAYA
11	1	C18	2.2 nF, Ceramic, Y1	440LD22-R	Vishay
12	1	C20	4.7 nF, 50 V, Ceramic, X7R, 0805	08055C472KAT2A	AVX
13	1	C22	10 μF, 16 V, Ceramic, X7R, 1206	C3216X7R1C106M	TDK
14	1	C23	10 pF, 50 V, Ceramic, NPO, 0805	C0805C100J5GACTU	Kemet
15	1	D1	600 V, 1 A, Rectifier, Fast Recovery, MELF (DL-41)	DL4937-13-F	Diodes, Inc.
16	1	D2	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
17	1	D8	100 V, 30 A, Schottky, TO-220AB	STPS30100ST	ST Micro
18	1	F1	2 A, 250 V, Slow, Long Time Lag, RST	RST 2	Belfuse
19	2	FL1 FL2	PCB Terminal Hole, #22 AWG	N/A	N/A
20	2	J1 J3	Test Point, RED, Miniature THRU-HOLE MOUNT	5000	Keystone
21	2	J2 J4	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
22	1	L4	Common Mode Choke Toroidal	P/N T22148-902S	Fontaine Tech
23	1	L5	Core, K5, Toroidal, 10 mm O.D. x 4 mm Th x 6 mm I.D.	K5B T 10*4*6	Kingcore Taiwan
24	1	R2	100 Ω, 5%, 1/2 W, Thick Film, 1210	ERJ-14YJ101U	Panasonic
25	1	R3	3 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ302V	Panasonic
26	1	R7	100 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ104V	Panasonic
27	1	R8	23.2 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2322V	Panasonic
28	1	R9	4.3 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ432V	Panasonic
29	1	R13	20 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ200V	Panasonic
30	1	R19	41.2 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF4122V	Panasonic
31	1	R20	10.2 kΩ, 1%, 1/4 W, Thick Film, 0805	ERJ-6ENF1022V	Panasonic
32	1	R28	27 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ273V	Panasonic
33	2	R29 R30	3.3 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ335V	Panasonic
34	1	T1	Bobbin, RM8, Vertical, 12 pins	RM8/12/1	Schwartzpunkt
35	1	TE1	Terminal, Eyelet, Tin Plated Brass, Zierick PN 190	190	Zierick
36	1	U3	LinkSwitch-HP, eSIP-7F	LNK6766E	Power Integrations
37	1	VR1	130 V, 1.25 W, 5%, DO214AC (SMA)	BZG03C130TR	Vishay

7 變壓器設計試算表

ACDC_LinkSwitch-HP_051612; Rev.0.13; Copyright Power Integrations 2012	INPUT	OUTPUT	UNIT	LinkSwitch-HP Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES				
VACMIN	90	90	V	Minimum AC Input Voltage
VACMAX	265	265	V	Maximum AC Input Voltage
fL	50	50	Hz	AC Mains Frequency
VO	12	12	V	Output Voltage (main)
PO	30	30	W	Output Power
n	0.84	0.84		Efficiency Estimate
Z	0.50	0.50		Loss Allocation Factor
VB	10	10	V	Bias Voltage
tC	3	3	ms	Bridge Rectifier Conduction Time Estimate
CIN	68	68	uF	Input Filter Capacitor
ENTER LINKSWITCH-HP VARIABLES				
LinkSwitch-HP	**LNK6766E**	**LNK6766E**		Selected LinkSwitch-HP
ILIMITMIN		1.814	A	Minimum Current limit
ILIMITMAX		2.087	A	Maximum current limit
KI	0.60	0.600	A	Current limit reduction factor
ILIMITMIN_EXT		1.088	A	External Minimum Current limit
ILIMITMAX_EXT		1.252	A	External Maximum current limit
fS		132000	Hz	LinkSwitch-HP Switching Frequency:Choose between 132 kHz and 66 kHz
fSmin		124000	Hz	LinkSwitch-HP Minimum Switching Frequency
fSmax		140000	Hz	LinkSwitch-HP Maximum Switching Frequency
KP	0.59	0.59		Ripple to Peak Current Ratio (0.4 < KP < 6.0)
VOR	100	100.00	V	Reflected Output Voltage
Voltage Sense				
VUVON	100	100.00	V	Undervoltage turn on
VUVOFF		42.14	V	Undervoltage turn off
VOV		446.44	V	Overvoltage threshold
FMAX_FULL_LOAD		139135	Hz	Maximum switching frequency at full load
FMIN_FULL_LOAD		123234	Hz	Minimum switching frequency at full load
TSAMPLE_FULL_LOAD		3.51	us	Minimum available Diode conduction time at full load.This should be greater than 2.5 us
TSAMPLE_LIGHT_LOAD		1.76	us	Minimum available Diode conduction time at light load.This should be greater than 1.11 us
Rpd		23.20	k-ohm	Program delay Resistor
Cpd	4.7	4.70	nF	Program delay Capacitor
Total programmed delay		0.03	sec	Total program delay
VDS	3.64	3.64	V	LinkSwitch-HP on-state Drain to Source Voltage
VD	0.5	0.50	V	Output Winding Diode Forward Voltage Drop
VDB	0.70	0.70	V	Bias Winding Diode Forward Voltage Drop
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES				
Core Type	**RM8**			
Core		#N/A		Selected Core
Custom Core				Enter name of custom core is applicable
AE	0.5200	0.52	cm^2	Core Effective Cross Sectional Area
LE	3.3500	3.35	cm	Core Effective Path Length
AL	2600.0	2600	nH/T^2	Ungapped Core Effective Inductance
BW	9.0	9	mm	Bobbin Physical Winding Width
M	2.00	2.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	3.00	3		Number of Primary Layers

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NS	7.00	7		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS				
VMIN	100	100	V	Minimum DC Input Voltage
VMAX	375	375	V	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS				
DMAX		0.51		Maximum Duty Cycle
IAVG		0.36	A	Average Primary Current
IP		0.99	A	Peak Primary Current
IR		0.59	A	Primary Ripple Current
IRMS		0.51	A	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS				
LP_TYP		693	uH	Typical Primary Inductance
LP_TOL	7	7	%	Primary inductance Tolerance
NP		56		Primary Winding Number of Turns
NB		6		Bias Winding Number of Turns
ALG		221	nH/T^2	Gapped Core Effective Inductance
BM		2368	Gauss	Maximum Flux Density at PO, VMIN (BM<3000)
BP		3189	Gauss	Peak Flux Density (BP<3700)
BAC		699	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur		1333		Relative Permeability of Ungapped Core
LG		0.27	mm	Gap Length (Lg > 0.1 mm)
BWE		15	mm	Effective Bobbin Width
OD	0.40	0.40	mm	Maximum Primary Wire Diameter including insulation
INS		0.06	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA		0.34	mm	Bare conductor diameter
AWG		28	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM		161	Cmils	Bare conductor effective area in circular mils
CMA		313	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
FEEDBACK SENSING SECTION				
RFB1		41.20	k-ohms	Feedback divider upper resistor
RFB2		9.53	k-ohms	Feedback divider lowerr resistor
TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE OUTPUT EQUIVALENT)				
Lumped parameters				
ISP		7.96	A	Peak Secondary Current
ISRMS		4.04	A	Secondary RMS Current
IO		2.50	A	Power Supply Output Current
IRIPPLE		3.18	A	Output Capacitor RMS Ripple Current
CMS		809	Cmils	Secondary Bare Conductor minimum circular mils
AWGS		21	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS		0.73	mm	Secondary Minimum Bare Conductor Diameter
ODS		0.71	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS		-0.01	mm	Maximum Secondary Insulation Wall Thickness
VOLTAGE STRESS PARAMETERS				
VDRAIN		605	V	Peak voltage acoss drain to source of Linkswitch-HP
PIVS		59	V	Output Rectifier Maximum Peak Inverse Voltage
PIVB		50	V	Bias Rectifier Maximum Peak Inverse Voltage
TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)				
1st output				
VO1		12	V	Output Voltage
IO1		2.50	A	Output DC Current
PO1		30.00	W	Output Power
VD1		0.5	V	Output Diode Forward Voltage Drop
NS1		7.00		Output Winding Number of Turns

ISRMS1		4.043	A	Output Winding RMS Current
IRIPPLE1		3.18	A	Output Capacitor RMS Ripple Current
PIVS1		59	V	Output Rectifier Maximum Peak Inverse Voltage
CMS1		809	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1		21	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1		0.73	mm	Minimum Bare Conductor Diameter
ODS1		0.71	mm	Maximum Outside Diameter for Triple Insulated Wire

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8 變壓器規格

8.1 電氣圖

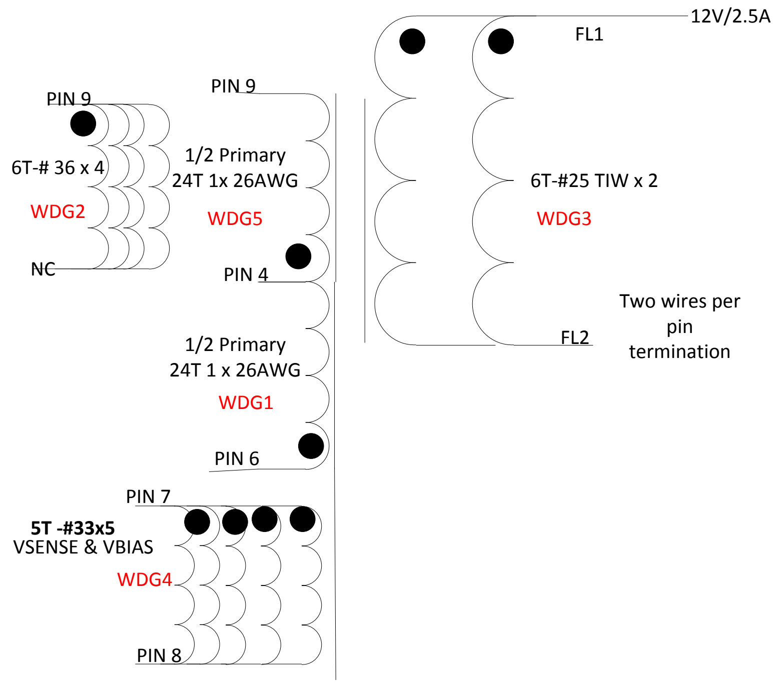


Figure 5 – Transformer Electrical Diagram.

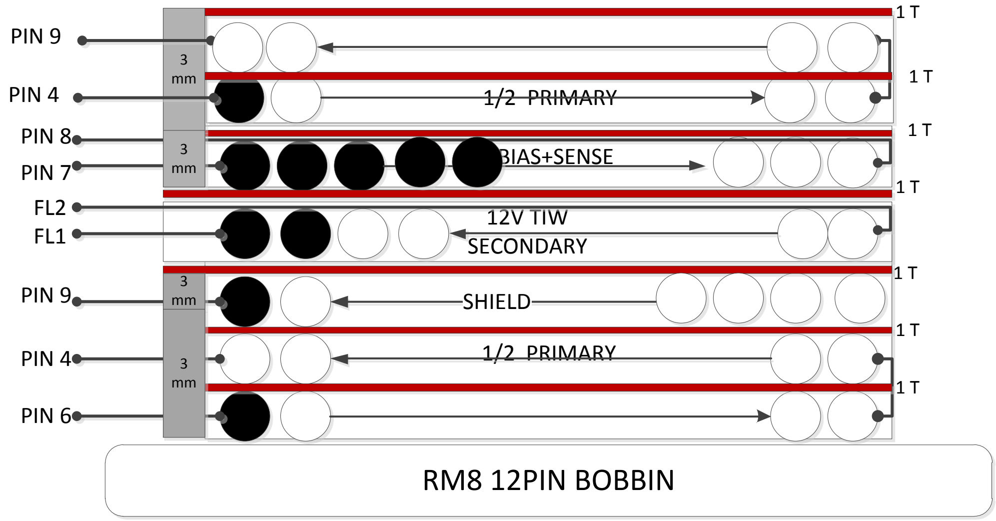
8.2 電氣規格

Electrical Strength	1 second, 60 Hz, from pins 1-3 to pins 6-10.	3000 VAC
Primary Inductance	Pins 6-9, all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	0.693 mH, ±7%
Resonant Frequency	Pins 6-9, all other windings open.	1400 kHz (Min.)
Primary Leakage Inductance	Pins 6-9, with all other pins shorted, measured at 100 kHz, 0.4 V_{RMS}.	15 μH (Max.)

8.3 物料

Item	Description
[1]	Core:RM8, NC-2H (Nicera) or Equivalent, gapped for ALG of 219 nH/t².
[2]	Bobbin:Vertical 12 pin.
[3]	Magnet Wire:#26 AWG.
[4]	Magnet Wire:#33, #36 AWG.
[5]	TIW Wire:#25 AWG.
[5]	Tape:3M 1298 Polyester Film, 2.0 mils thick, 9.8 mm wide.

8.4 變壓器建構圖



Electrical Test Specifications

Parameter	Condition	Spec
Electrical Strength, VAC	60 Hz 1 second, from pins 5-9 to pins 1,2,3,4,10-12.	3000
Nominal Primary Inductance, µH	Measured at 1 V pk-pk, typical switching frequency, between pin 6 to pin 9, with all other Windings open.	693
Tolerance, ±%	Tolerance of Primary Inductance	10.0
Maximum Primary Leakage, µH	Measured between Pin 6 to Pin 9, with all other Windings shorted.	15

Figure 6 – Transformer Build Diagram.

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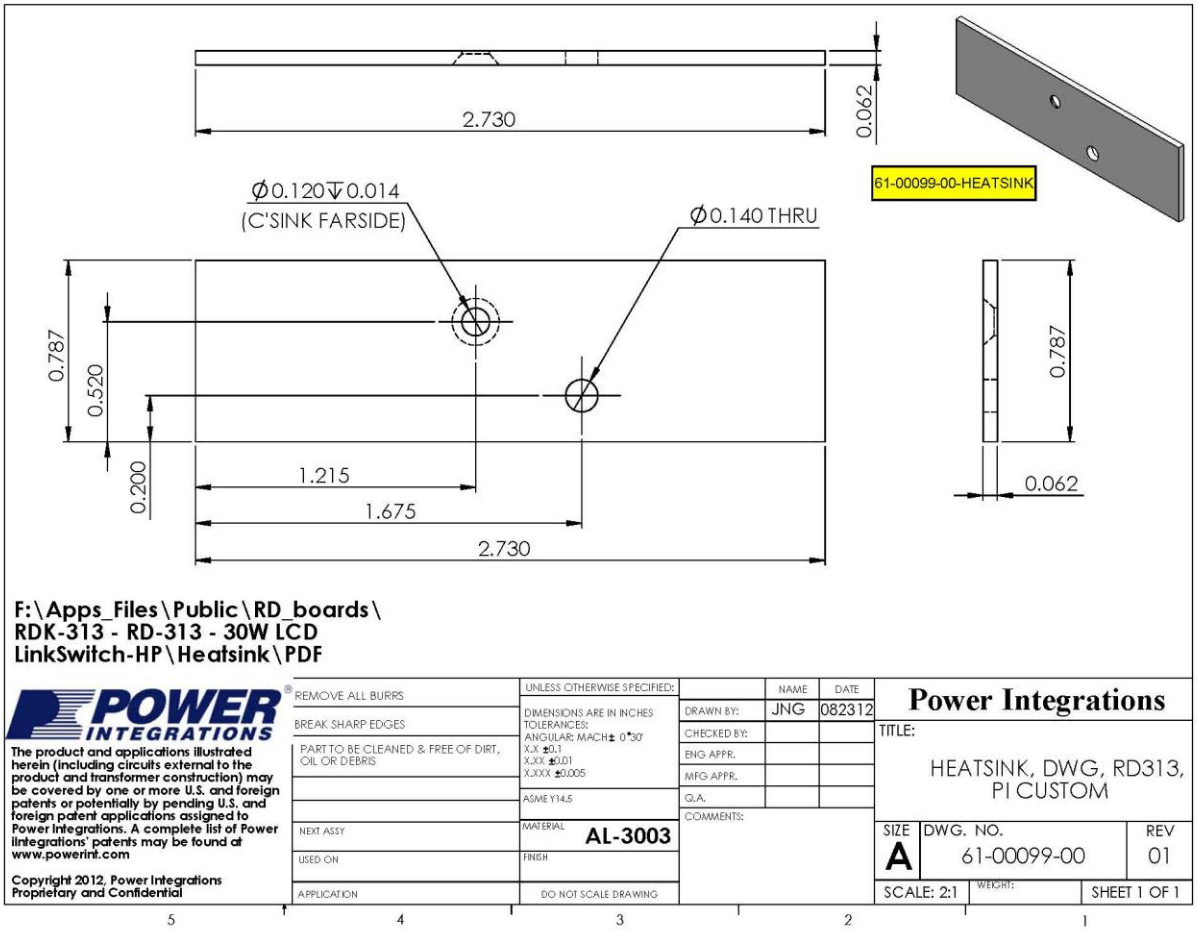
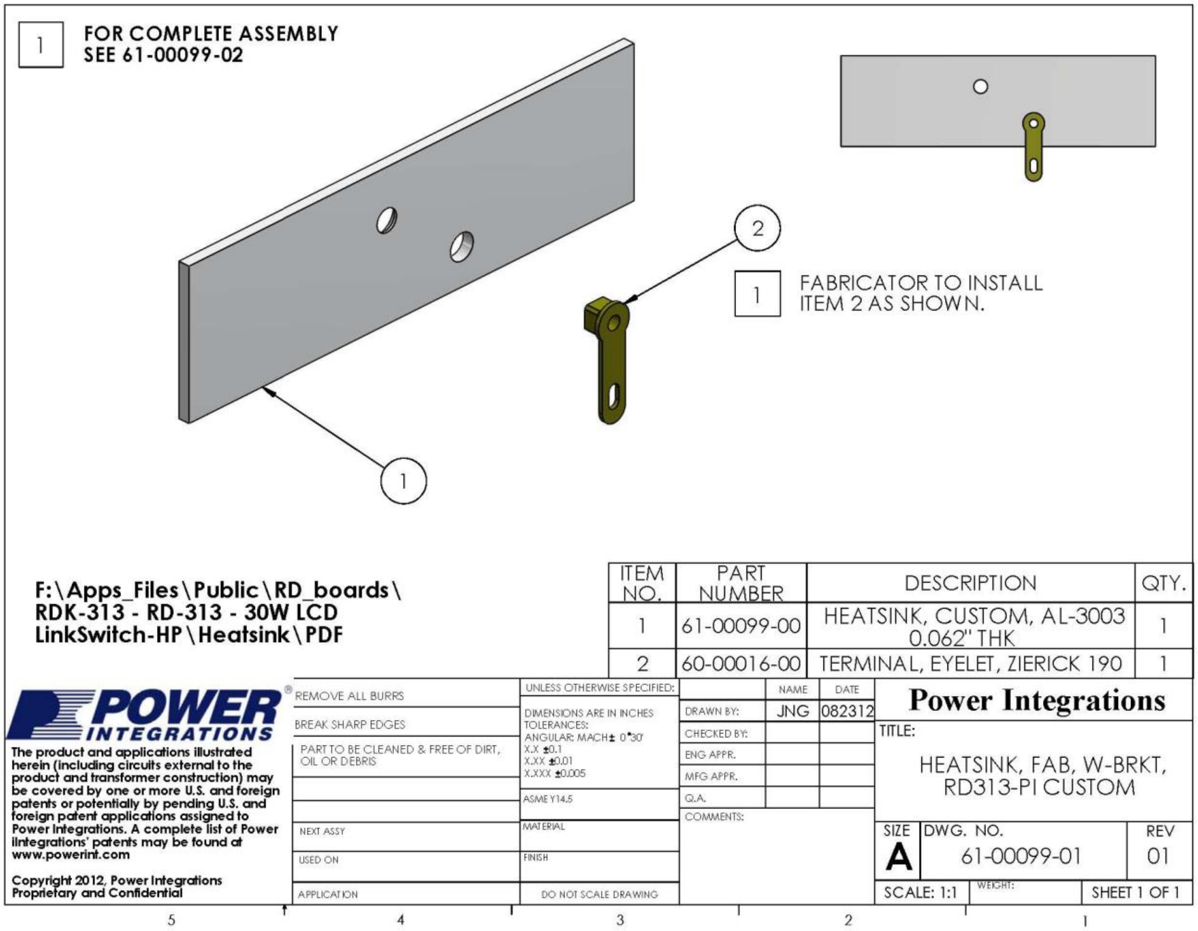
9 散熱片組裝

9.1 eSIP 散熱片

9.1.1 eSIP 散熱片製造圖



9.1.2 eSIP 散熱片組裝圖



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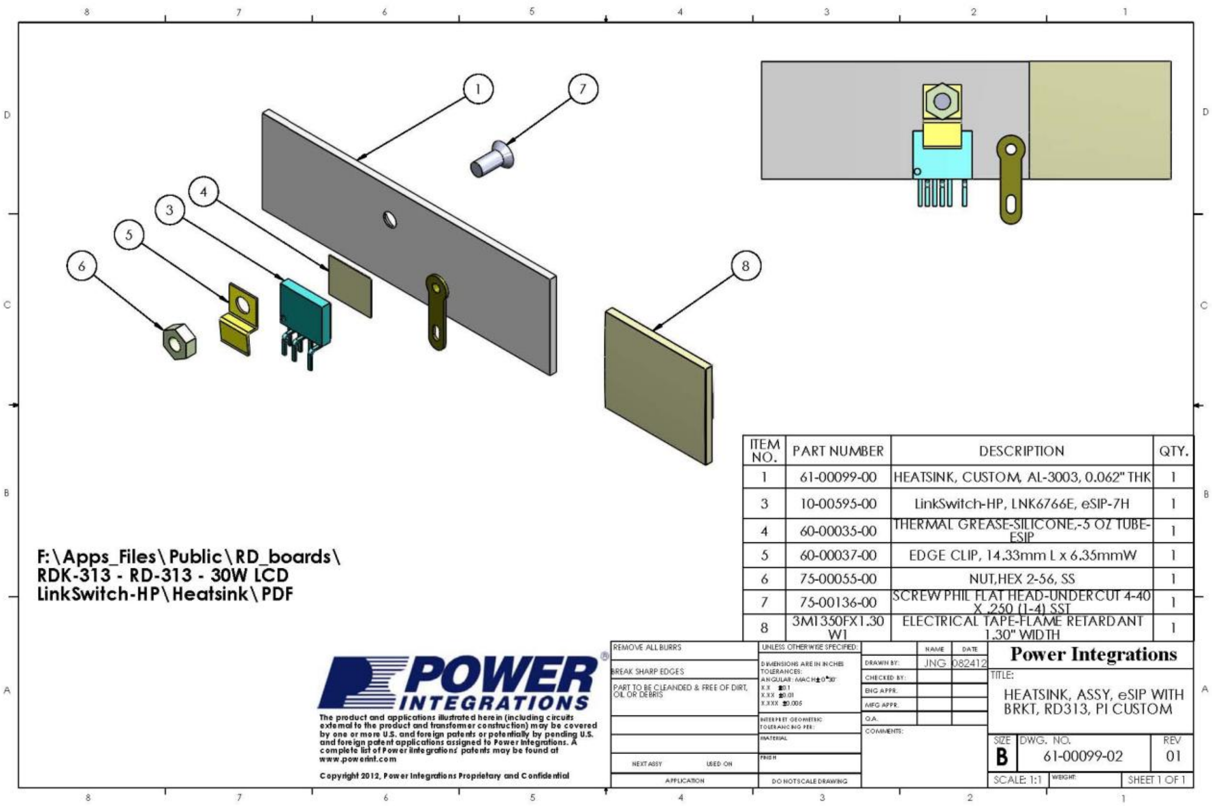
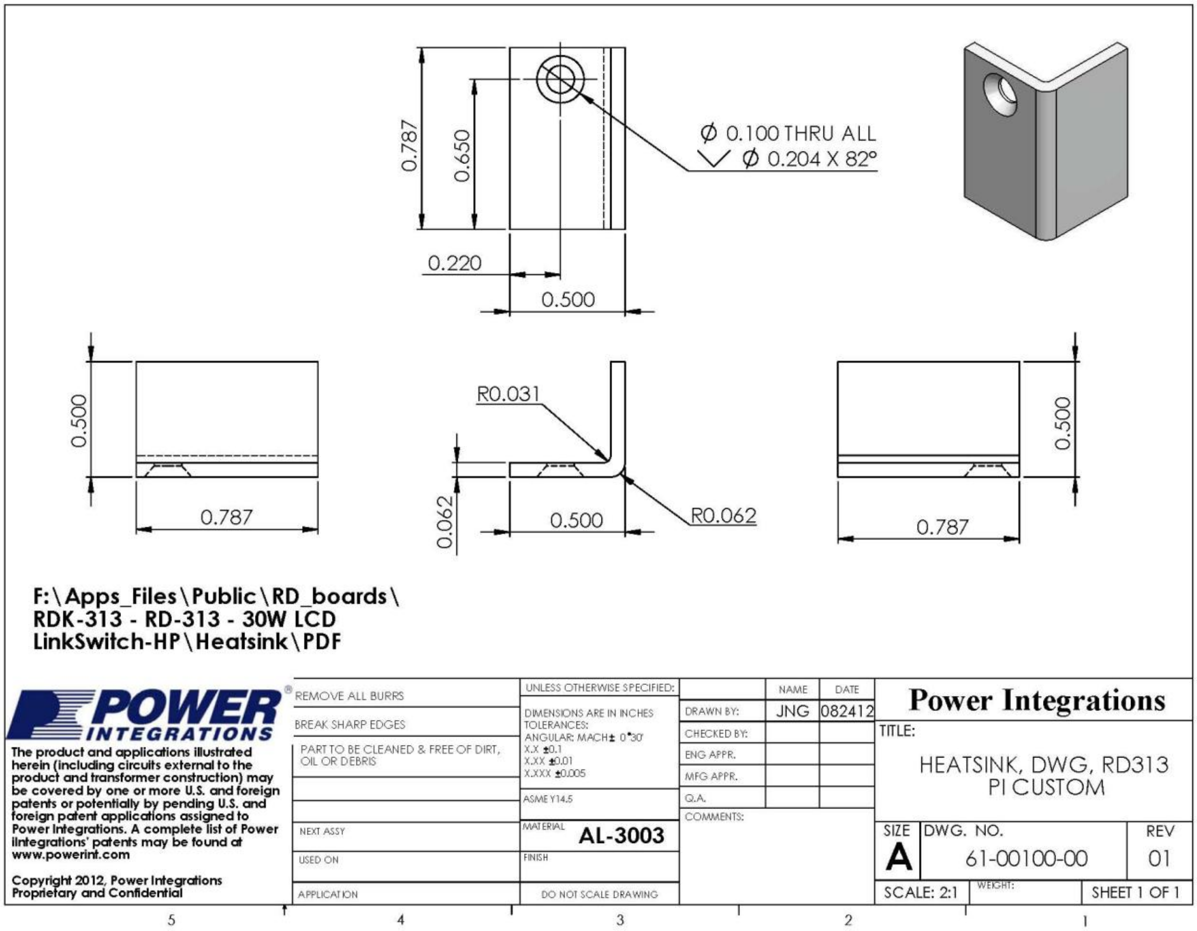
9.1.3 ESIP 和散熱片組裝圖



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00099-00	HEATSINK, CUSTOM, AL-3003, 0.062" THK	1
3	10-00595-00	LinkSwitch-HP, LNK6766E, eSIP-7H	1
4	60-00035-00	THERMAL GREASE-SILICONE,-5 OZ TUBE-ESIP	1
5	60-00037-00	EDGE CLIP, 14.33mm L x 6.35mmW	1
6	75-00055-00	NUT,HEX 2-56, SS	1
7	75-00136-00	SCREW PHIL FLAT HEAD-UNDERCUT 4-40 X .250 (1-4) SST	1
8	3M1350FX1.30 W1	ELECTRICAL TAPE-FLAME RETARDANT 1.30" WIDTH	1

9.2 二極體散熱片

9.2.1 二極體散熱片製造圖



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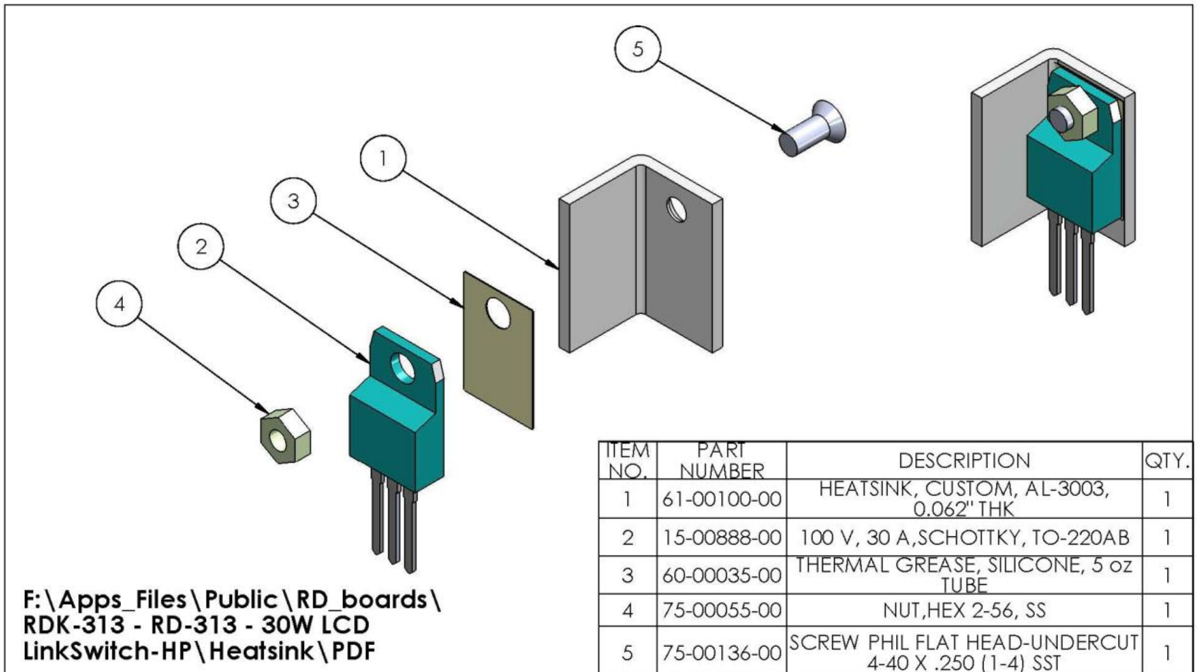
9.2.2 二極體和散熱片組裝圖面



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00100-00	HEATSINK, CUSTOM, AL-3003, 0.062" THK	1
2	15-00888-00	100 V, 30 A,SCHOTTKY, TO-220AB	1
3	60-00035-00	THERMAL GREASE, SILICONE, 5 oz TUBE	1
4	75-00055-00	NUT,HEX 2-56, SS	1
5	75-00136-00	SCREW PHIL FLAT HEAD-UNDERCUT 4-40 X .250 (1-4) SST	1

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The product and applications illustrated herein (including circuits external to the product and transformer construction) may be covered by one or more U.S. and foreign patents or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Iintegrations' patents may be found at www.powerint.com

REMOVE ALL BURRS
BREAK SHARP EDGES
PART TO BE CLEANED & FREE OF DIRT, OIL OR DEBRIS
NEXT ASSY
USED ON
APPLICATION

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES:
ANGULAR: MACH± 0°30'
X.X ±0.1
X.XX ±0.01
X.XXX ±0.005
ASME Y14.5
MATERIAL
FINISH
DO NOT SCALE DRAWING

	NAME	DATE
DRAWN BY:	JNG	082412
CHECKED BY:		
ENG APPR.		
MFG APPR.		
Q.A.		

COMMENTS:

Power Integrations

TITLE: HEATSINK, ASSY, DIODE, RD313, PI CUSTOM

SIZE: A | DWG. NO.: 61-00100-02 | REV: 01

SCALE: 1:1 | WEIGHT: | SHEET 1 OF 1

5 4 3 2 1

10 效能資料

於室溫、50 Hz 線電壓頻率下進行所有測量 (除非另有指定)。所有測試的滿載均為 2.5 A。

10.1 工作模式效率

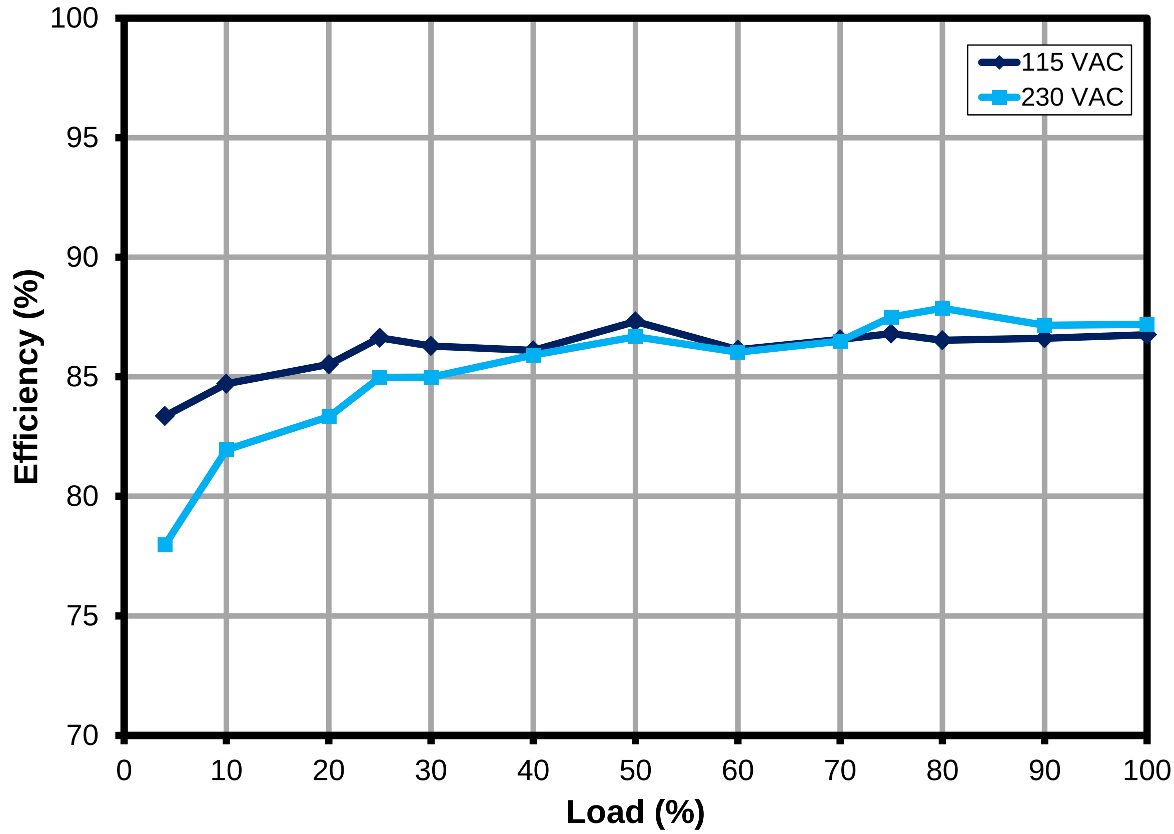

Figure 7– Active mode Efficiency, Room Temperature

115 VAC			
V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	η
12.1	0.625	8.73	86.63%
12	1.251	17.18	87.3%
11.94	1.875	25.79	86.8%
11.91	2.5	34.32	86.76%
		Avg	86.88%

230 VAC			
V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	η
12.1	0.625	8.9	84.97%
12.01	1.251	17.32	86.7%
11.97	1.875	25.65	87.5%
11.94	2.5	34.25	87.19%
		Avg	86.58%

Table 1 – Four Point Average Efficiency (25%, 50%, 75% and 100%), Room Temperature.

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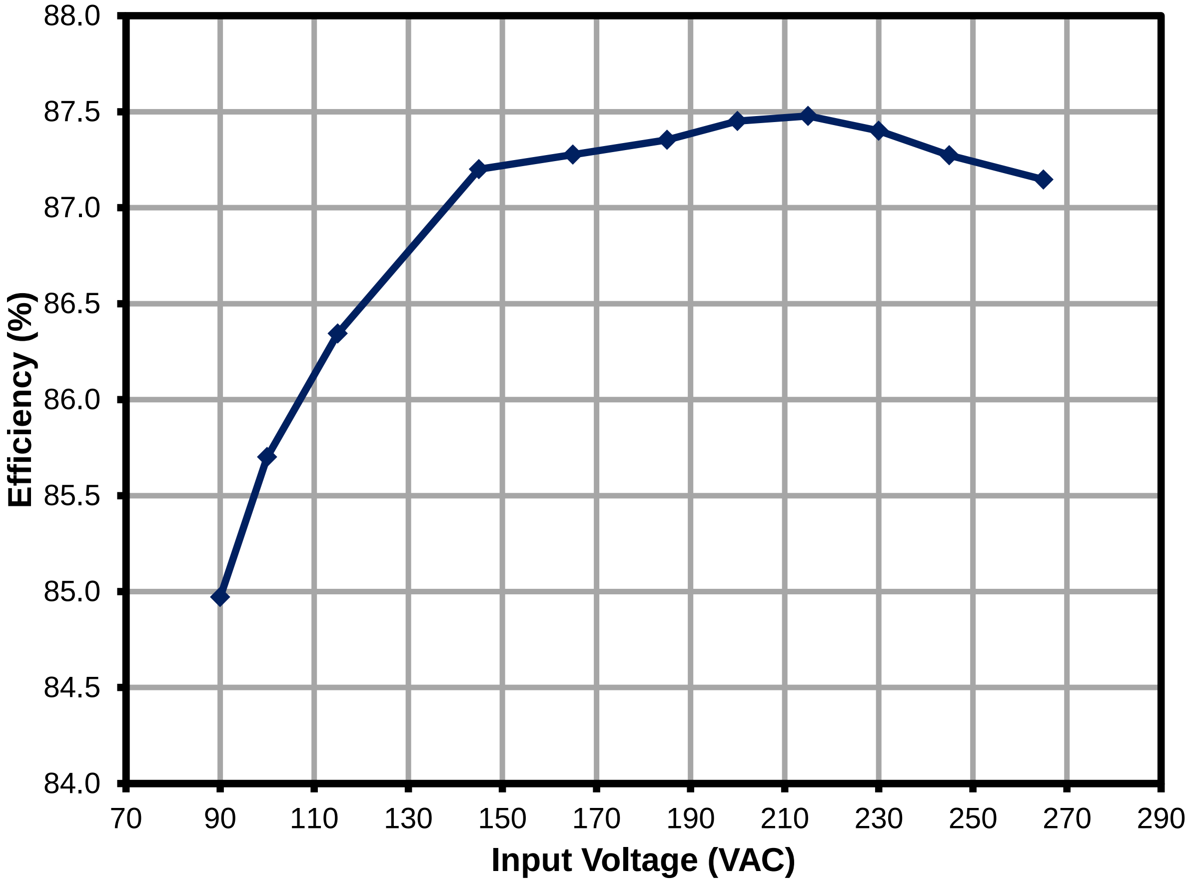

Figure 8 – Full Load Efficiency vs. Input Voltage, Room Temperature.

10.2 無負載輸入功率

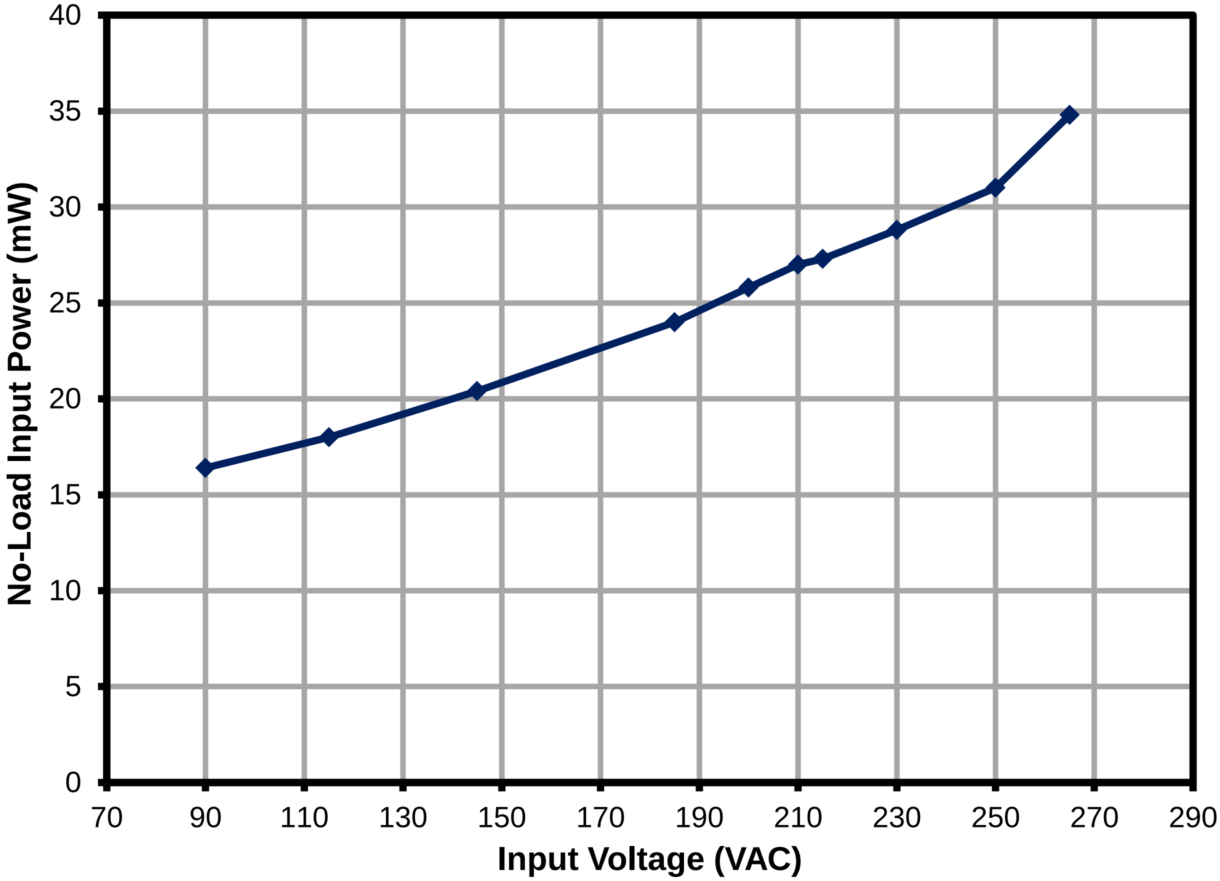

Figure 9 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

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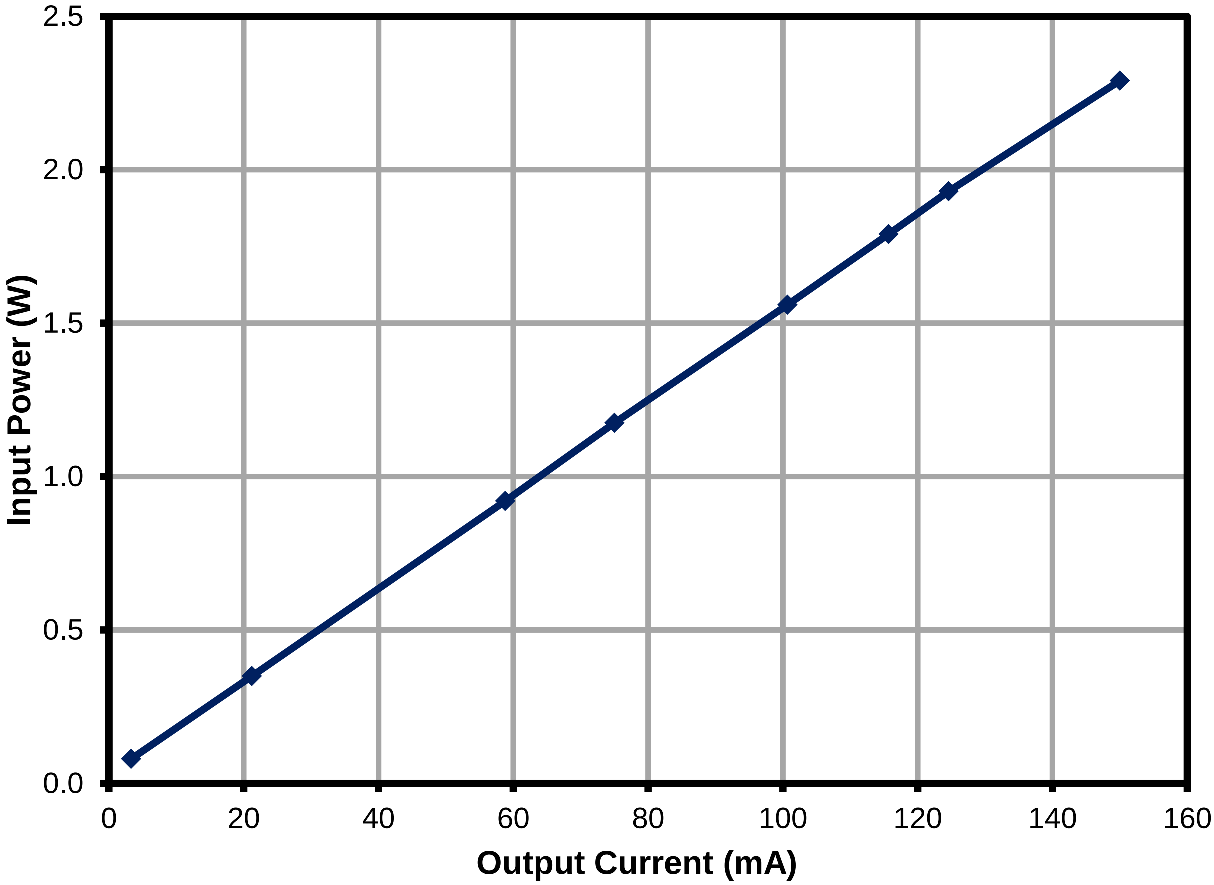

Figure 10 – Standby Performance at 230 VAC, Room Temperature.

10.3 線電壓調節

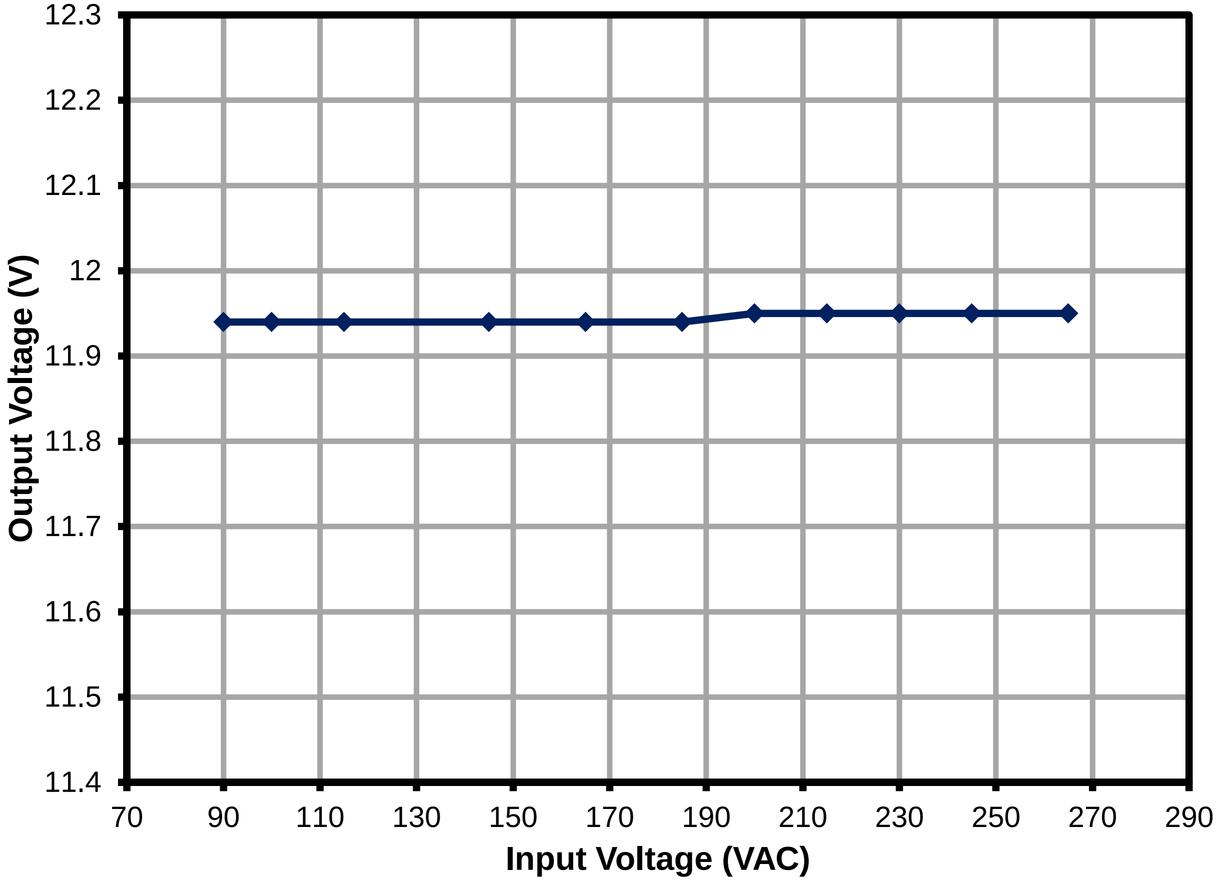

Figure 11 – Line Regulation under Full Load, Room Temperature.

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10.4 負載調節

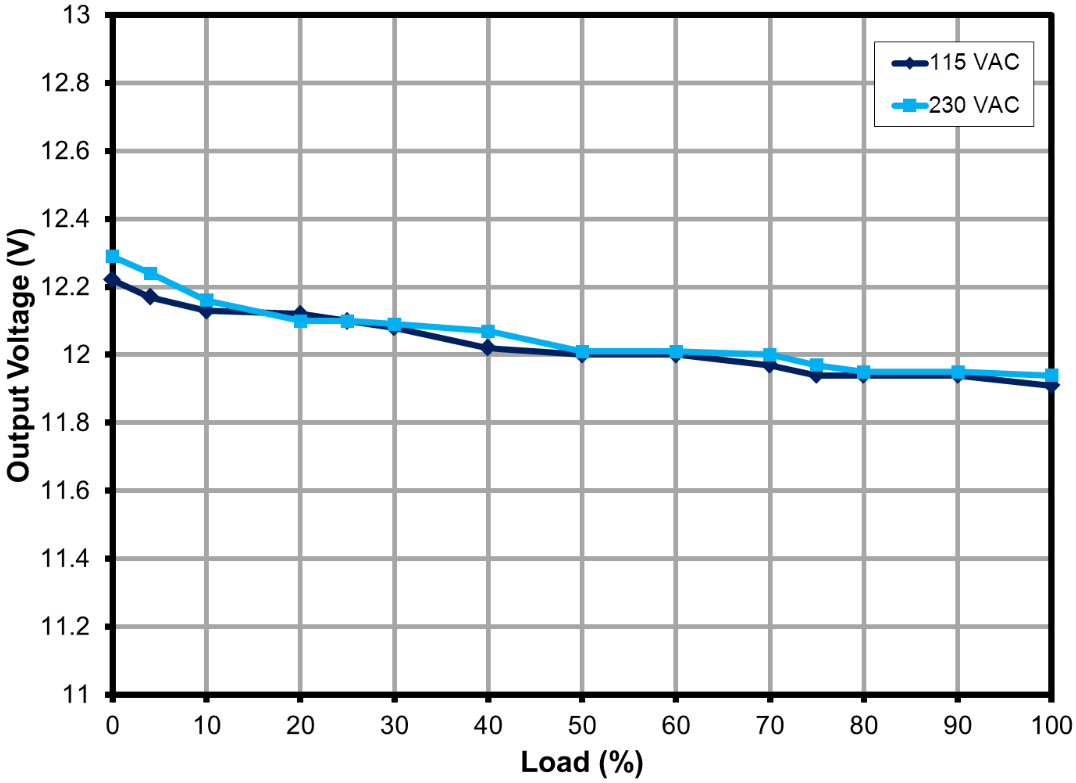

Figure 12 – Load Regulation, Room Temperature.

10.5 功率限制

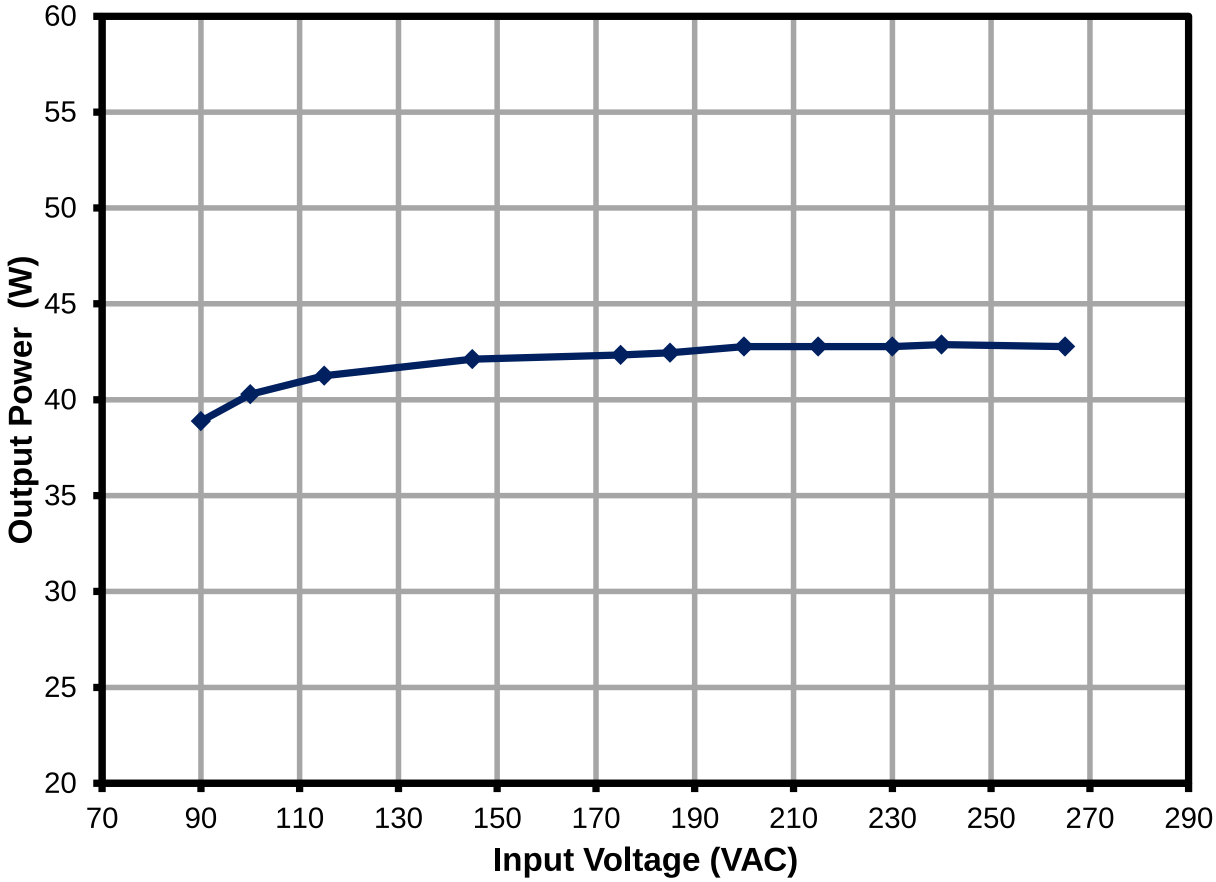

Figure 13 – Overload Power vs. Line Voltage.

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11 波形

11.1 汲極電壓和電流，正常操作

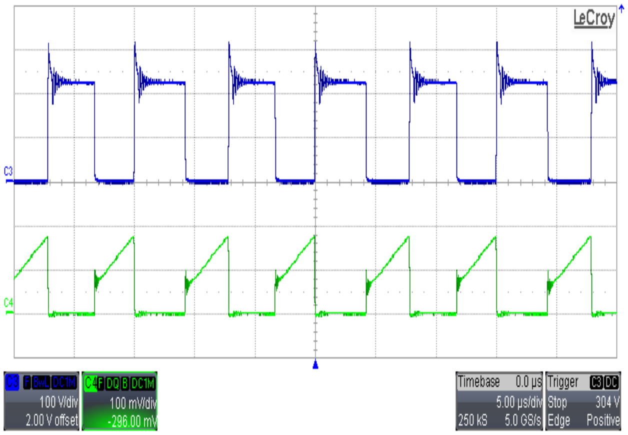

Figure 14 – 90 VAC, Full Load.
Upper:V_{DRAIN}, 100 V / div.
Lower:I_{DRAIN}, 0.5 A / div., 10 µs / div.

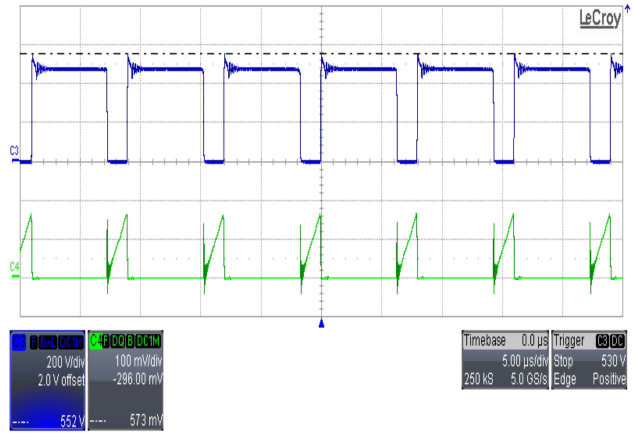

Figure 15 – 265 VAC, Full Load.
Upper:V_{DRAIN}, 200 V / div.
Lower:I_{DRAIN}, 0.5 A / div., 10 µs / div.

11.2 汲極電壓和電流，過載功率

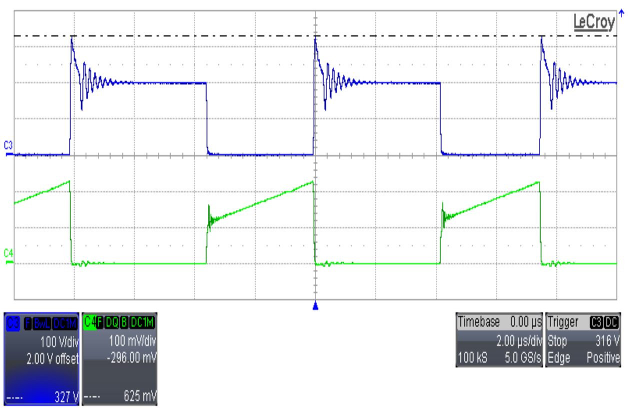

Figure 16 – 90 VAC, 38.8 W Overload Power.
Upper:V_{DRAIN}, 100 V / div.
Lower:I_{DRAIN}, 0.5 A / div., 10 µs / div.

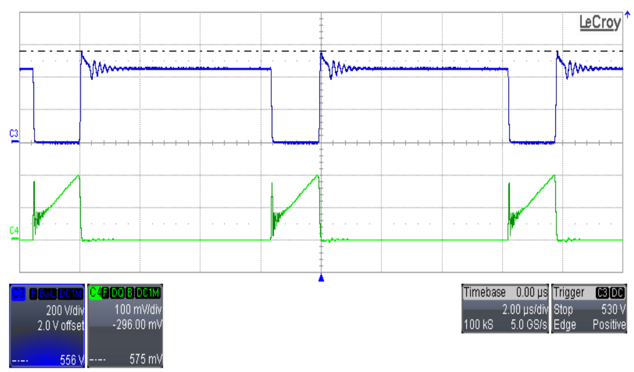

Figure 17 – 265 VAC, 42.78 W Overload Power.
Upper:V_{DRAIN}, 200 V / div.
Lower:I_{DRAIN}, 0.5 A / div., 10 µs / div.

11.3 電壓應力，過載功率

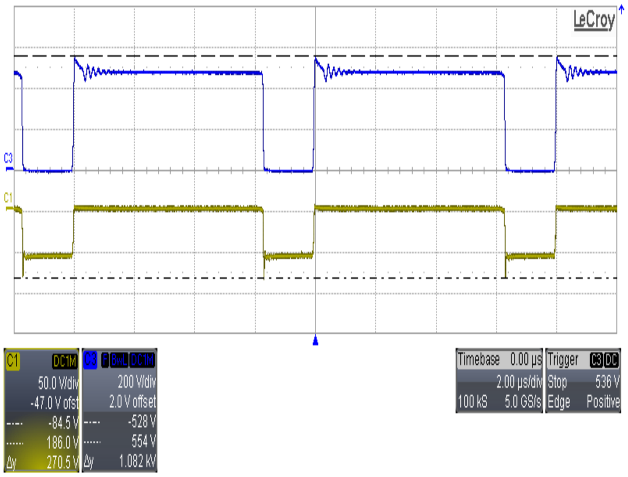

Figure 18 – 265 VAC, Overload Power.
Upper:V_{DRAIN}, 200 V / div.
Lower:PIV_{DIODE}, 50 V / div., 2.0 μs / div.

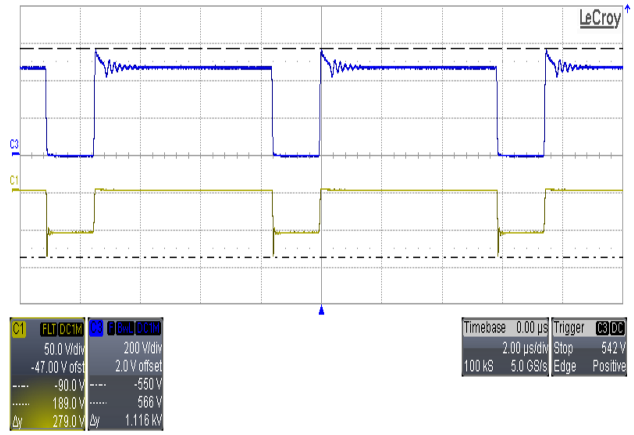

Figure 19 – 265 VAC, Overload Power.
Upper:V_{DRAIN}, 200 V / div.
Lower:PIV_{DIODE}, 50 V / div., 2.0 μs / div.

11.4 汲極電壓和電流啓動輪廓

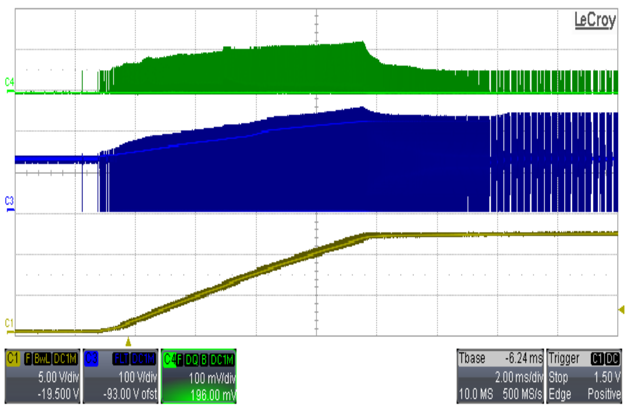

Figure 20 – 90 VAC, No-Load.
Upper:I_{DRAIN}, 0.5 A, 2 ms / div.
Middle:V_{DRAIN}, 100 V / div.
Lower:V_{OUT}, 5 V / div.

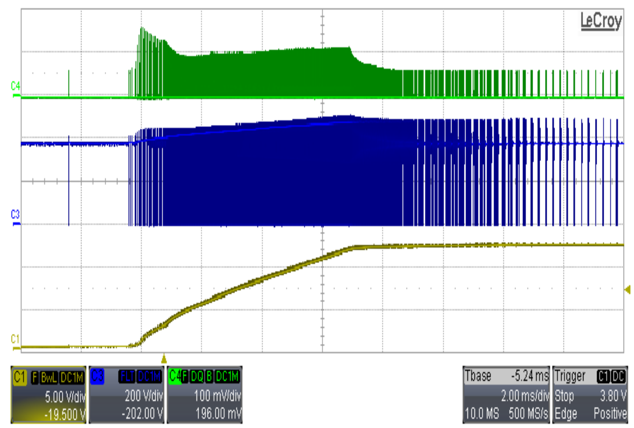

Figure 21 – 265 VAC, No-Load.
Upper:I_{DRAIN}, 0.5 A, 2 ms / div.
Middle:V_{DRAIN}, 200 V / div.
Lower:V_{OUT}, 5 V / div.

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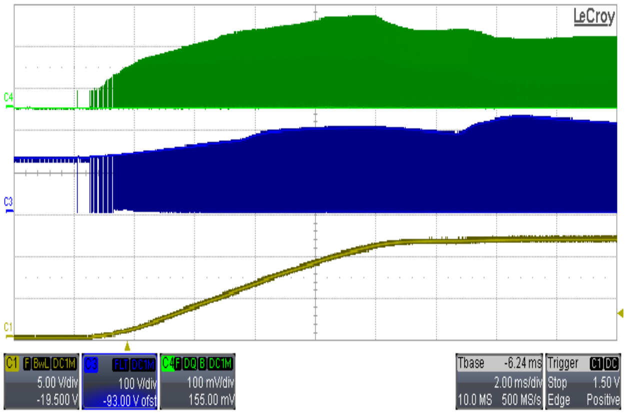

Figure 22 – 90 VAC, Full Load.
Upper:I_{DRAIN}, 0.5 A, 2 ms / div
Middle:V_{DRAIN}, 100 V / div.
Lower:V_{OUT}, 5 V / div.

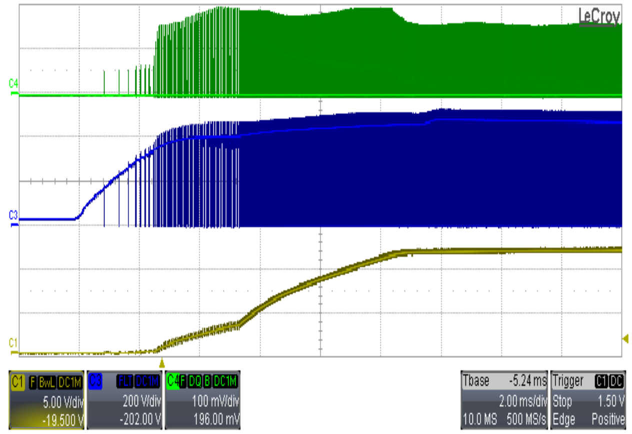

Figure 23 – 265 VAC, Full Load.
Upper:I_{DRAIN}, 0.5 A, 2 ms / div
Middle:V_{DRAIN}, 200 V / div.
Lower:V_{OUT}, 5 V / div.

11.5 負載暫態反應

In the figures shown below, the output was AC coupled to view the load transient response.The oscilloscope was triggered using the load current step as a trigger source.

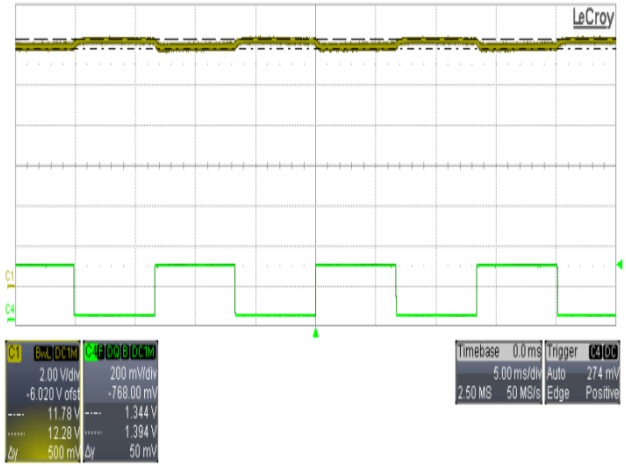

Figure 24 – Transient Response, 115 VAC, 5%<-->55% Step Load. Upper:V_{OUT}, 2 V / div. Lower:I_{OUT}, 1 A / div., 5 ms / div.

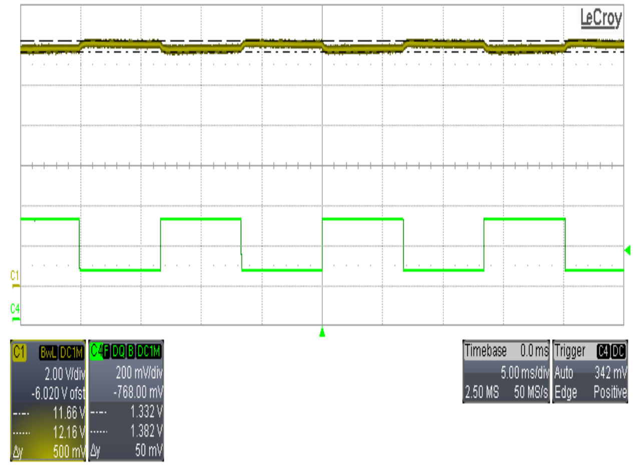

Figure 25 – Transient Response, 115 VAC, 50%<-->100% Step Load. Upper:V_{OUT}, 2 V / div. Lower:I_{OUT}, 1 A / div., 5 ms / div.

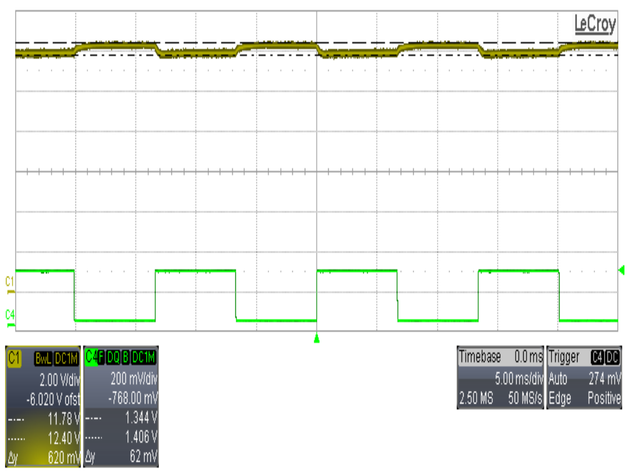

Figure 26 – Transient Response, 230 VAC, 5%<-->55% Step Load. Upper:V_{OUT}, 2.0 V / div. Lower:I_{OUT}, 1 A / div., 5 ms / div.

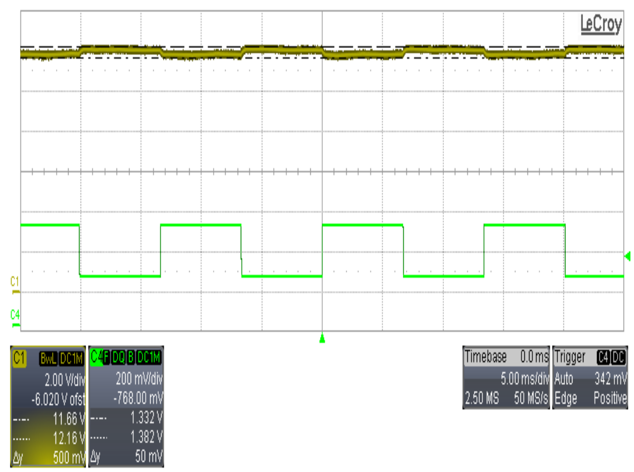

Figure 27 – Transient Response, 230 VAC, 50%<-->100% Step Load. Upper:V_{OUT}, 2.0 V / div. Lower:I_{OUT}, 1 A / div., 5 ms / div.

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11.6 輸出漣波和雜訊測量

11.6.1 漣波測量技術

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up.Details of the probe modification are provided in the figures below.
The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip.The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 4.7 μF / 50 V aluminum electrolytic.***The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).***

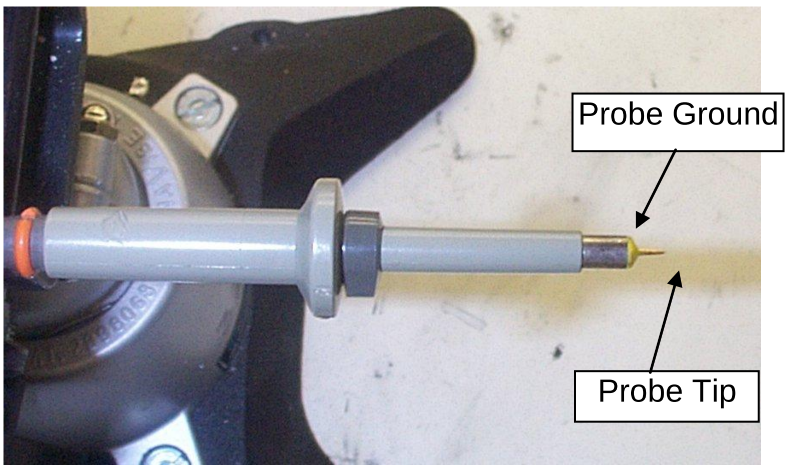

Figure 28 – Oscilloscope Probe Prepared for Ripple Measurement (End Cap and Ground Lead Removed).

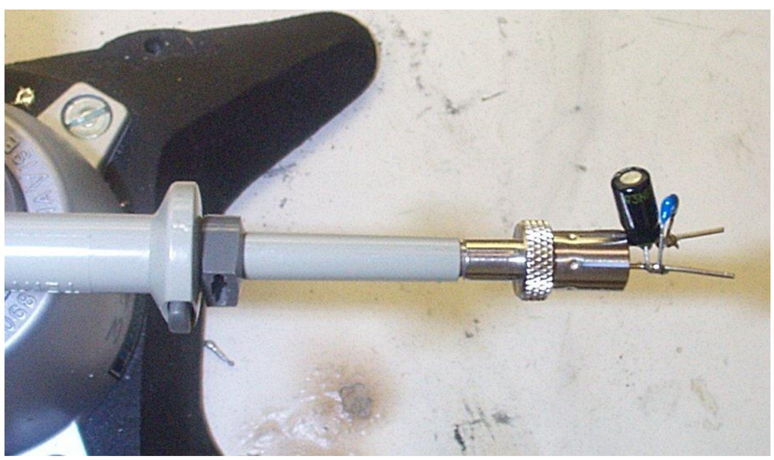

Figure 29 – Oscilloscope Probe with Probe Master 5125BA BNC Adapter (Modified with Wires for Probe Ground for Ripple Measurement, and Two Parallel Decoupling Capacitors Added).

11.6.2 漣波和雜訊測量結果

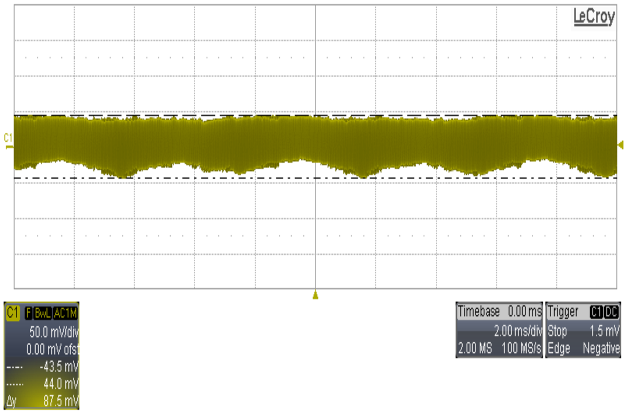

Figure 30 – Low Frequency Ripple, 115 VAC, Full Load.
V_{OUT}, 50 mV / div.

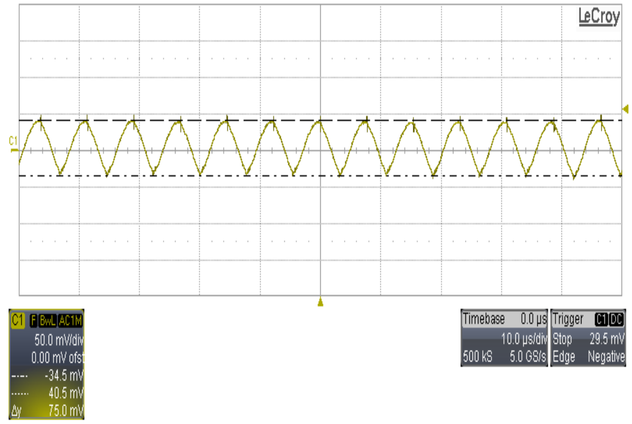

Figure 31 – Switching Noise, 115 VAC, Full Load.
V_{OUT}, 50 mV / div.

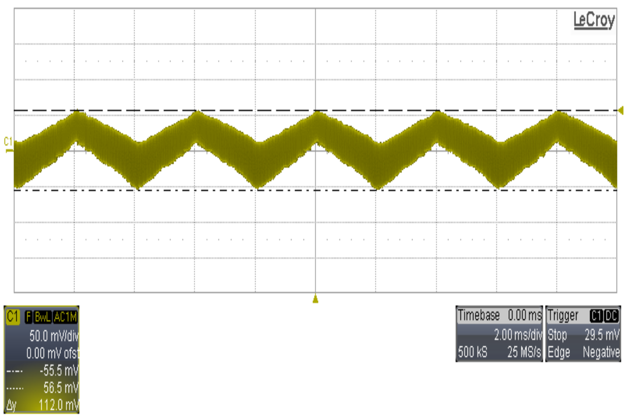

Figure 32 – Low Frequency Ripple, 230 VAC, Full Load.
V_{OUT}, 50 mV / div.

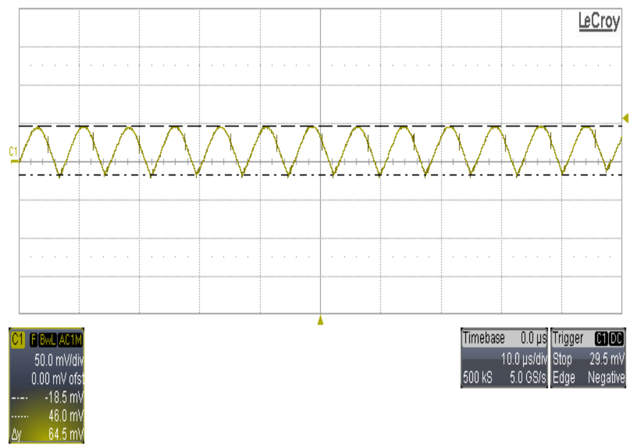

Figure 33 – Switching Noise, 230 VAC, Full Load.
V_{OUT}, 50 mV / div.

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12 保護功能

12.1 短路自動重新啓動

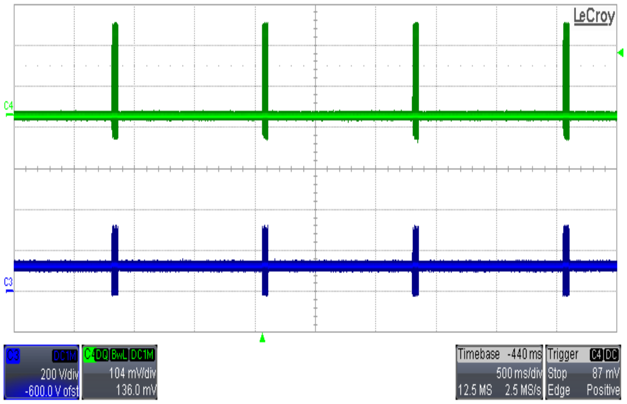

Figure 34 – Auto-restart Under Short-Circuit, 90 VAC.
Upper: I_{DRAIN}, 0.52 A / div., 500 ms / div.
Lower: V_{DRAIN}, 200 V / div.
Input Power = 1.38 W.

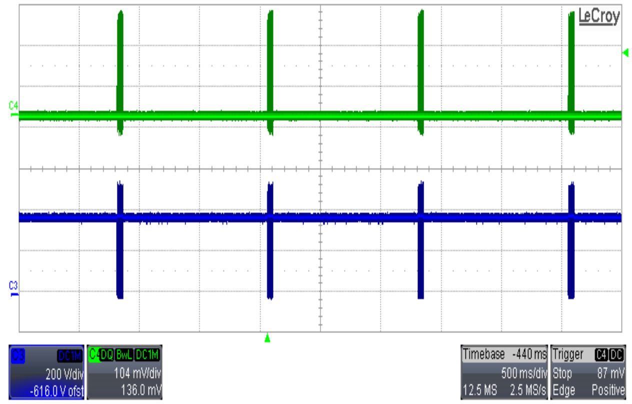

Figure 35 – Auto-restart Under Short-Circuit, 265 VAC.
Upper: I_{DRAIN}, 0.52 A / div., 500 ms / div.
Lower: V_{DRAIN}, 200 V / div.
Input Power = 1.41 W.

12.2 欠壓鎖定保護 (開路測試)

OVP is initiated by inserting a 100 kΩ between BP and CP pin during normal operation.

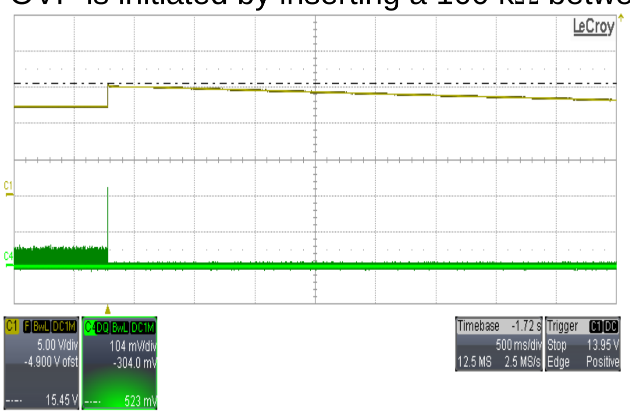

Figure 36 – OVP at 90 VAC, No-Load.
Upper: V_{OUT}, 5 V / div., 500 ms / div.
Lower: I_{DRAIN}, 0.52 A / div.
OVP Trip Point = 15.45 V.

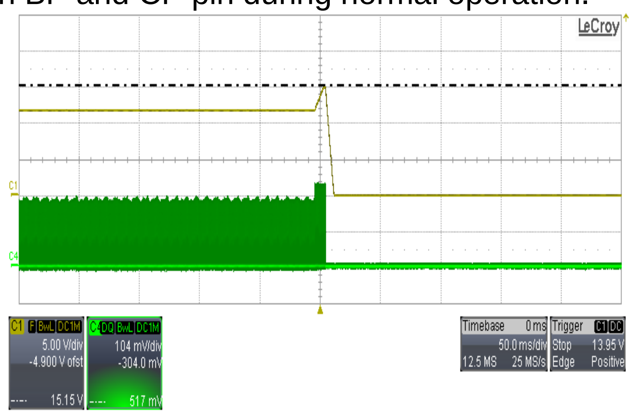

Figure 37 – OVP at 90 VAC, Full Load.
Upper: V_{OUT}, 5 V / div., 500 ms / div.
Lower: I_{DRAIN}, 0.52 A / div.
OVP Trip Point = 15.15 V.

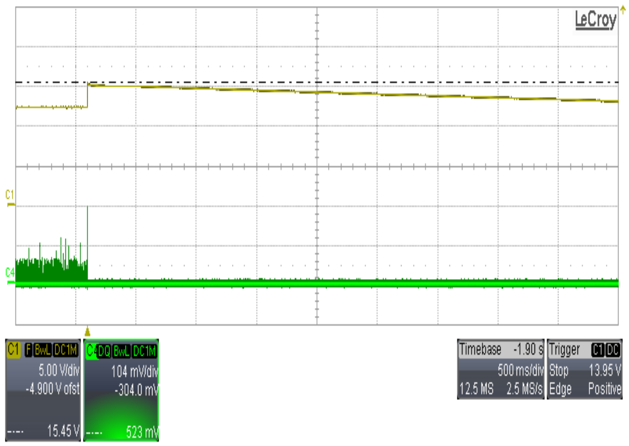

Figure 38 – OVP at 265 VAC, No-Load.
Upper: V_{OUT}, 5 V / div., 500 ms / div.
Lower: I_{DRAIN}, 0.52 A / div.
OVP Trip Point = 15.45 V.

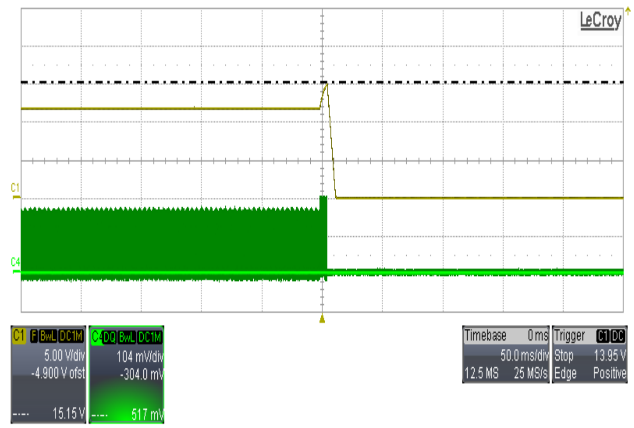

Figure 39 – OVP at 265 VAC, Full Load.
Upper: V_{OUT}, 5 V / div., 500 ms / div.
Lower: I_{DRAIN}, 0.52 A / div.
OVP Trip Point = 15.15 V.

12.3 電壓啓動與電壓關閉 (使用 DC 輸入源極測試)

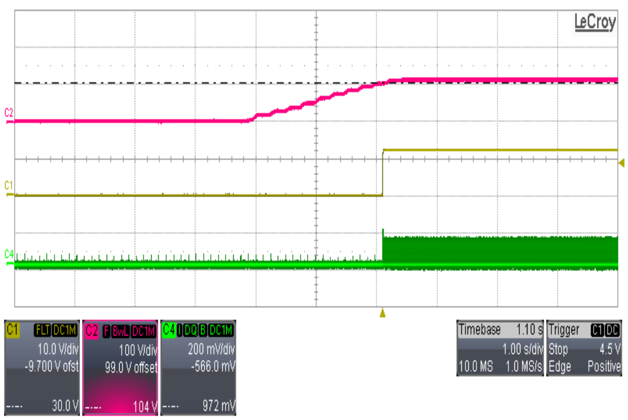

Figure 40 – Brown-in.
Upper: V_{IN}, 100 V / div., 1 s / div.
Middle: V_{OUT}, 10 V / div.
Lower: I_{DRAIN}, 1.0 A / div.

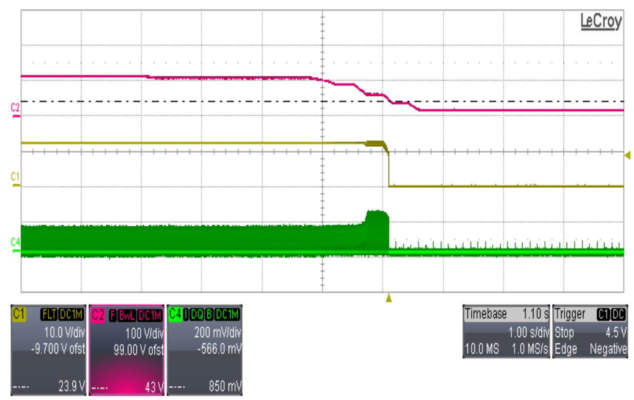

Figure 41 – Brown-out.
Upper: V_{IN}, 100 V / div., 1 s / div.
Middle: V_{OUT}, 10 V / div.
Lower: I_{DRAIN}, 1.0 A / div.

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12.4 線電壓欠壓保護 (使用 DC 輸入源極測試)

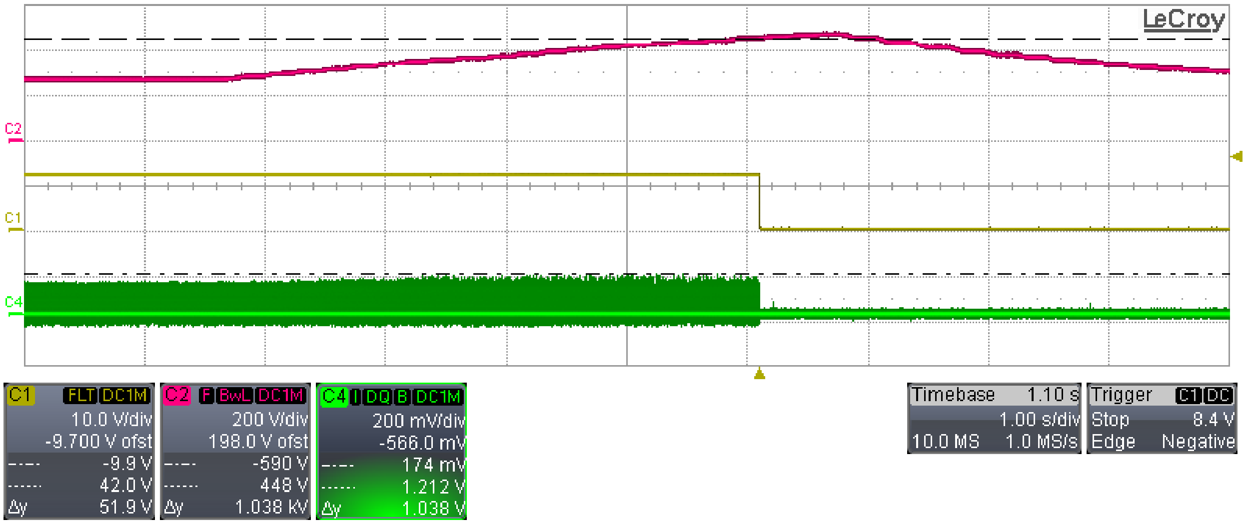


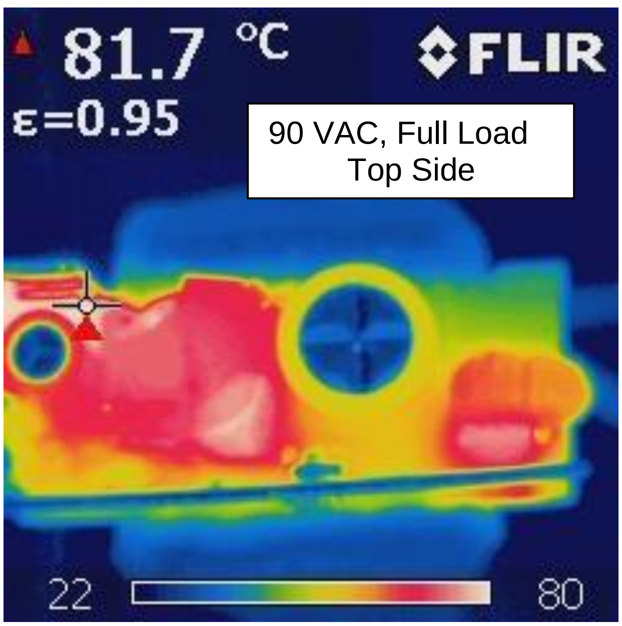
Figure 42 – Line Overvoltage Protection (Triggered at 448 V).
Upper:V_{IN}, 200 V / div., 1 s / div.
Middle:V_{OUT}, 10 V / div.
Lower:I_{DRAIN}, 1.0 A / div.

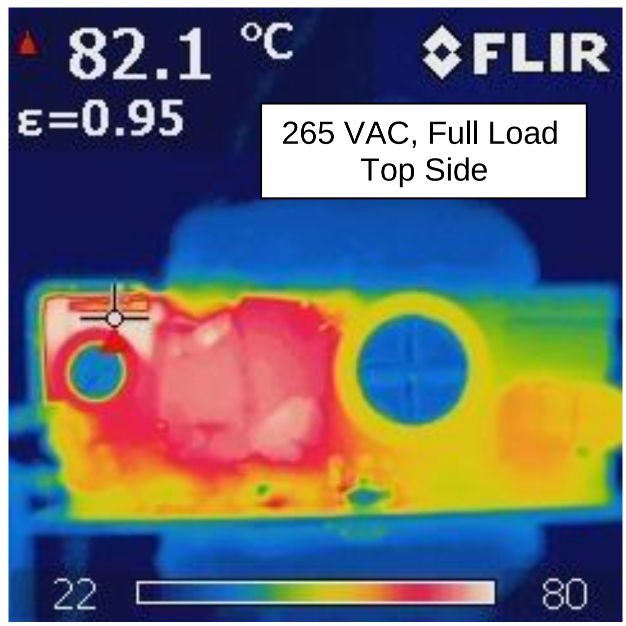
Note: Also programmed for latching under OTP conditions.

13 散熱效能 ($T_{AMBIENT}$ = 25 °C)

Thermal performance was measured at full load operation, open frame at ambient temperature of 25 °C.The transformer winding temperature was taken on the outermost layer.

Item	Description	90 VAC Full Load	265 VAC Full Load
1	Output Diode	81.7	82.1
2	LNK6766E	68	65
3	Transformer	73.3	75
4	Input Capacitor	58	43
5	Output CMC	62	55
6	Input CMC	61	35
7	Bridge Diode	77	52
8	Zener Clamp	73	63





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14 AC 突波 (輸出電阻滿載)

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Results (Pass/Fail # Strikes)
D.M.		**(2Ω source)**		**10 Strikes Each Level**
+1000	230	L1 to L2	90	Pass
-1000	230	L1 to L2	270	Pass
C.M.		**(12Ω source)**		
+2000	230	L1, L2 to PE	90	Pass
-2000	230	L1, L2 to PE	270	Pass

15 ESD (輸出電阻滿載)

Device	Discharge Type	Discharge Location	Voltage	# of Events (1/sec)	Remarks
LNK6766E	Contact	+ Output Terminal	+8 kV	10	PASS
			-8 kV	10	PASS
		- Output Terminal	+8 kV	10	PASS
			-8 kV	10	PASS
	Air	+ Output Terminal	+15 kV	10	PASS
			-15 kV	10	PASS
		- Output Terminal	+15 kV	10	PASS
			-15 kV	10	PASS

PASS = No output glitch or latch-off.

16 滿載時的 EMI 測試

Conducted emissions tests were performed at 115 VAC and 230 VAC at full load.Composite EN55022B / CISPR22B conducted limits are shown.All the tests show excellent EMI performance.

16.1 EMI 結果

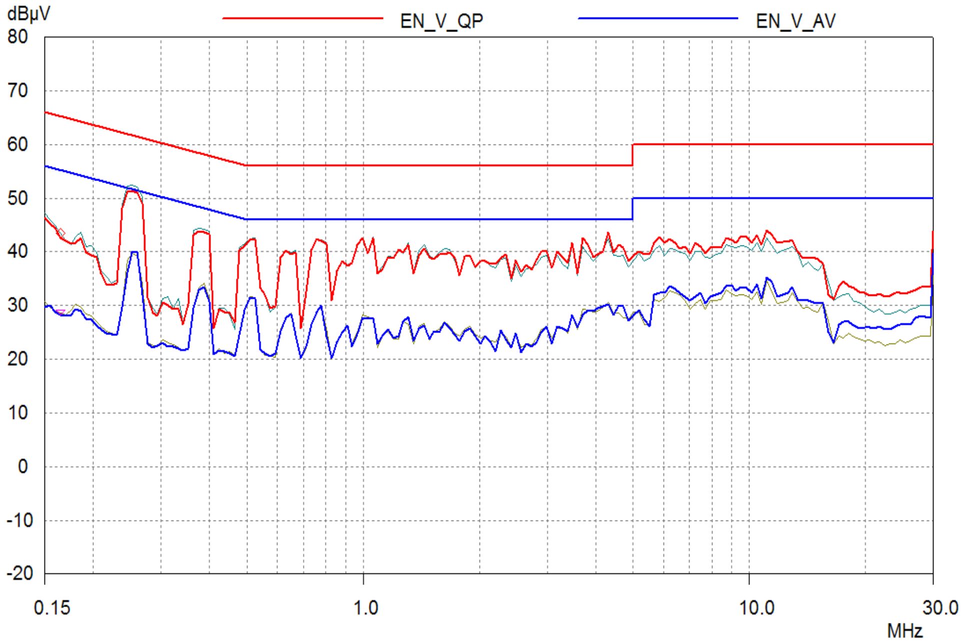

Figure 43 – Conducted EMI at 115 VAC 60 Hz, Full Load, and Output Return Connected to Ground.

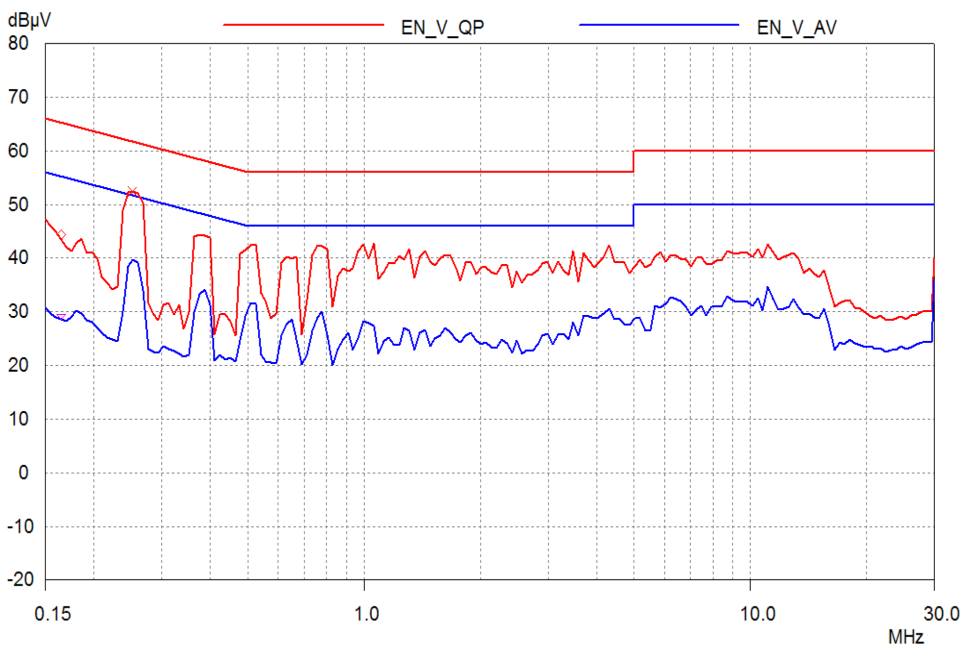

Figure 44 – Conducted EMI at 115 VAC 60 Hz, Full Load, and Output Return Connected to Artificial Hand.

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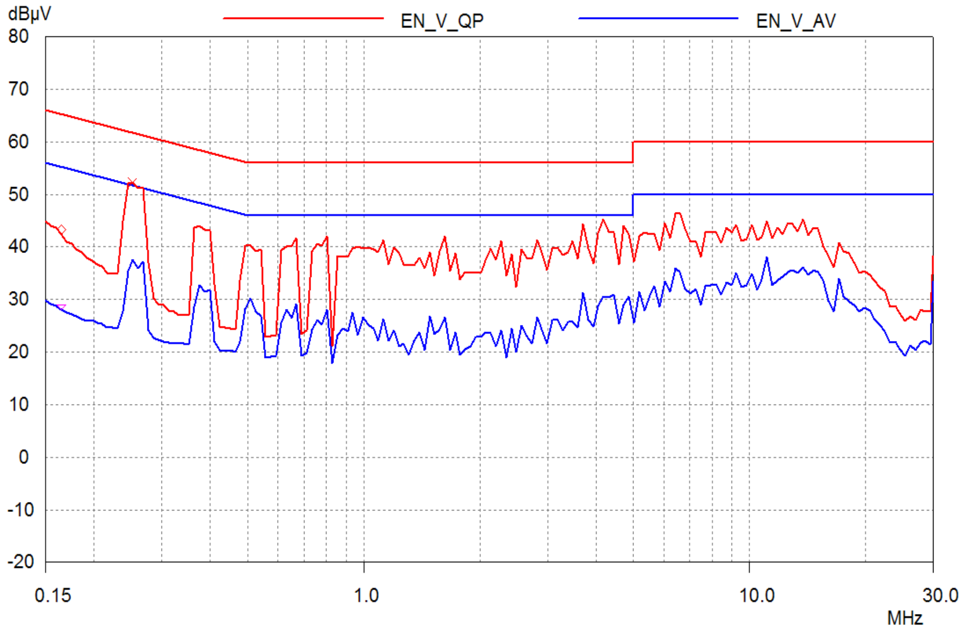

Figure 45 – Conducted EMI at 230 VAC 60 Hz, Full Load, and Output Return Connected to Ground.

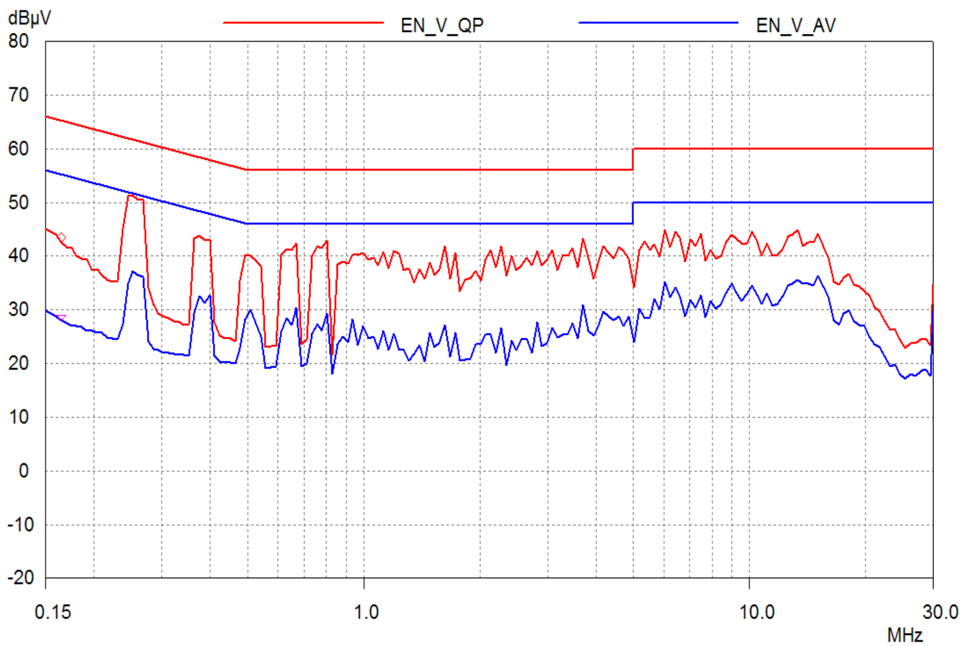

Figure 46 – Conducted EMI at 230 VAC 60 Hz, Full Load, and Output Return Connected to Artificial Hand.

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17 修訂記錄

Date	Author	Revision	Description & changes	Reviewed
24-Jul-12	SS	1.0	Initial Release	Apps & Mktg
01-Aug-12	SS	1.1	Changed D8 to thru-hole. Improved heat sink for PI device and output diode.Changed BR2 and VR1 to SMD.	
14-Sep-12	KM	1.2	Updated schematic and format.	

如需最新更新，請造訪我們的網站： **www.powerint.com**

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本處所述的產品和應用 (包括 PI 裝置 IC 之外的變壓器結構和電路) 可能包含 Power Integrations 的一項或多項美國及國外專利，或是正在申請的美國及國外專利。www.powerint.com 上提供了 Power Integrations 專利的完整清單。Power Integrations 授予其客戶某些特定專利權的授權，詳情請參閱 <http://www.powerint.com/ip.htm>。

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