Design Example Report

Title	***150 W AIO Power Supply Using HiperPFS™-3 PFS7526H and LinkSwitch™-HP LNK6779EG without Standby Converter***
Specification	90 VAC – 264 VAC Input; 150 W (20 V at 7.5 A) Output
Application	AIO 80 Plus Bronze Power Supply
Author	Applications Engineering Department
Document Number	DER-437
Date	September 21, 2016
Revision	3.2

Summary and Features

- Integrated PFC stage using
  - PFS7526H from HiperPFS-3 family of ICs
- Integrated flyback stage using
  - LNK6779EG from LinkSwitch-HP family of ICs
  - Secondary side regulated isolated flyback converter
- Metting light load consumption requirement without using CAPZero
- <175 mW noload consumption
- P_{IN} = 450 mW at 250 mW P_{OUT} with 230 VAC
- Non standy solution
- Excellent output regulation and transient response
- Meeting 80 PLUS bronze with 1% margin
- Can deliver 180 W of peak power during transients

Power Integrations
5245 Hellyer Avenue, San Jose, CA 95138 USA.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This engineering report describes a 20 V, 7.5 A power supply for 90 VAC to 264 VAC AIO power supplies which can also serve as a general purpose evaluation board for the combination of a HiperPFS-3 power factor stage with LinkSwitch-HP output stage using devices from the Power Integration's HiperPFS-3 and LinkSwitch-HP device families.

The design is based on the PFS7526H IC for the PFC front end, with a LNK6779E utilized in an isolated flyback output stage. Due to low power sunsumption of LinkSwitch-HP device, no standby stage is needed to meet the no-load and light load consumption requirements.

Note:

- LNK6779E (4mS) was used for better no-load power and regulation in conjunction with a secondary optocoupler circuit.
- Secondary side regulation circuit was used in order to improve the output regulation, transient response and no-load consumption. Compensation network components were altered from standard values used in existing designs to improve the transient performance.
- Forced air-cooling is required when operating the power supply.

Figure 1 – Photograph, Top View.

Figure 2 – Photograph, Bottom View.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		264	VAC	2 Wire Input
Frequency	f_{LINE}	47	50/60	63	Hz	
Output 1						
Output Voltage	V_M	19.5	20	21	V	20 VDC ± 5%
Output Ripple	$V_{RIPPLE(M)}$			200	mV P-P	20 MHz Bandwidth
Output Current	I_M	0.00	7.5	9	A	
Total Output Power						
Continuous Output Power	P_{OUT}		150	180	W	

Note: The power supply can only start-up with 7.5 A of load current. The power supply can deliver 9 A load only during transient conditions.

3 Schematic

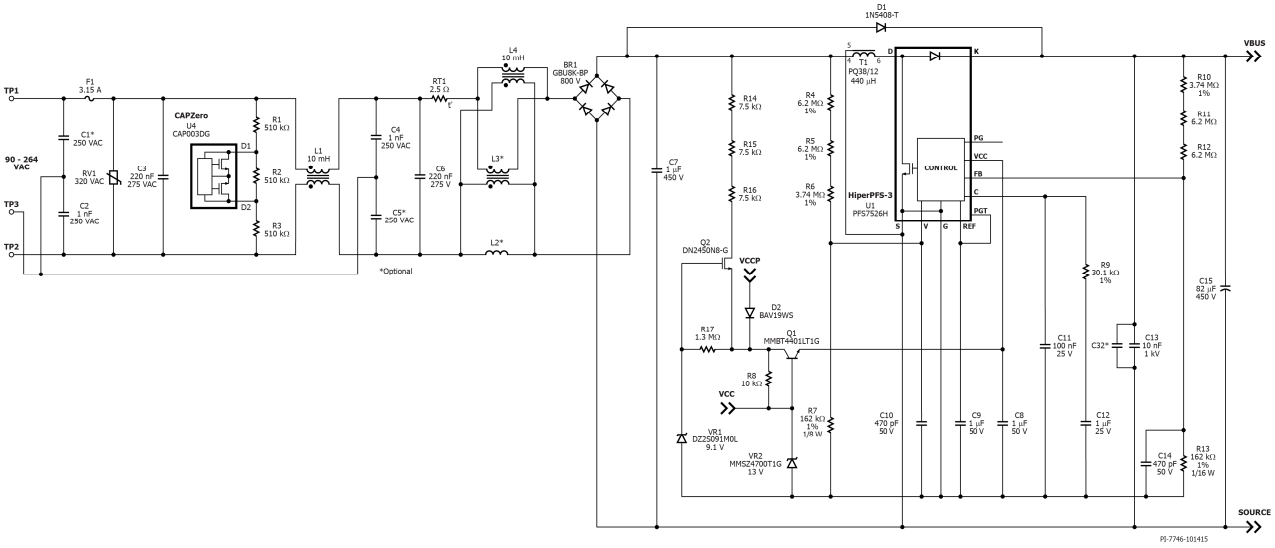

Figure 3 – Schematic DER-437 AIO Power Supply Application Circuit - Input Filter, Bridge Rectifier and PFC Section.

Note: * Marked components are optional. Capzero was not populated on the board.

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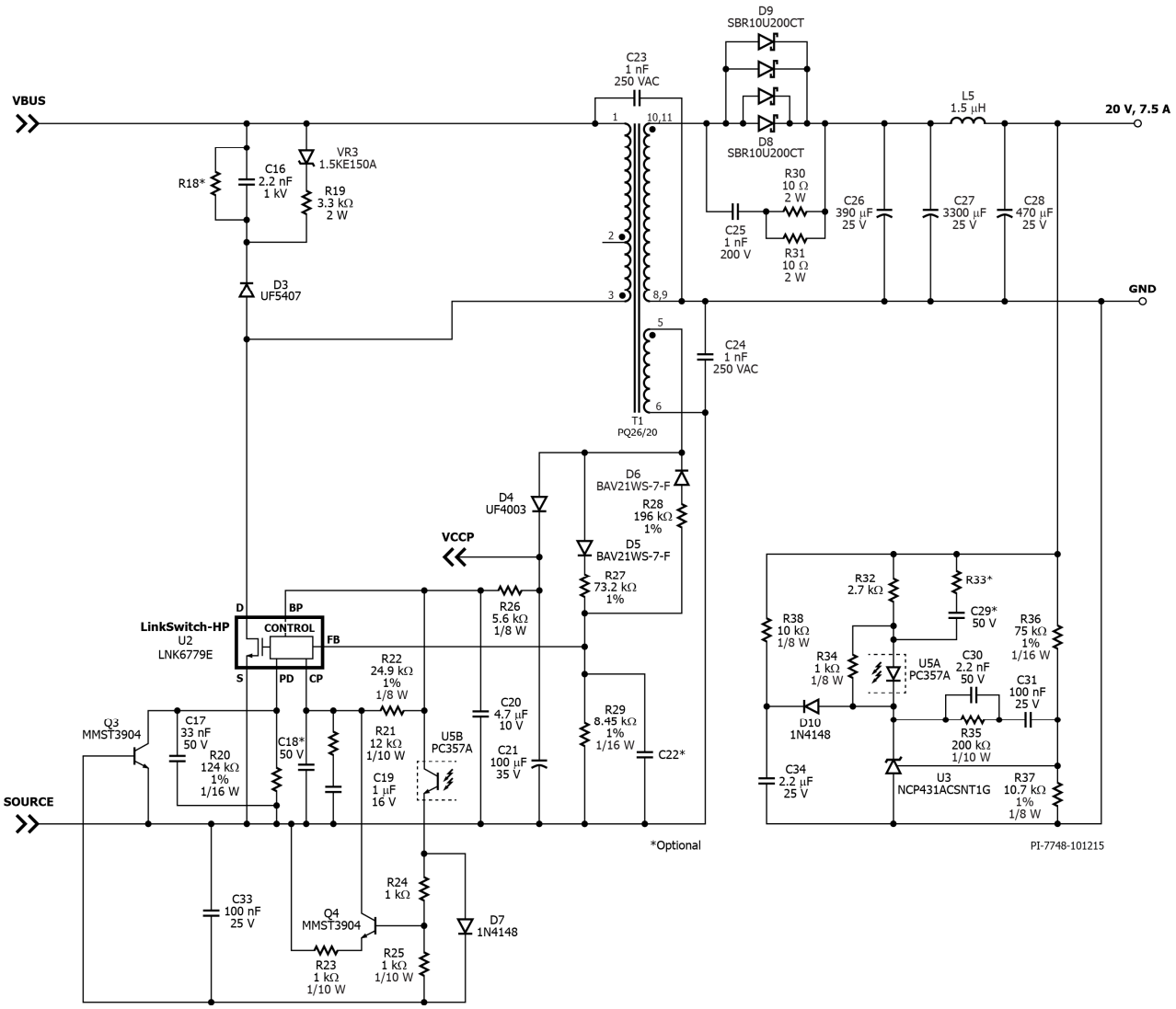

Figure 4 – Schematic DER-437 AIO Power Supply Application Circuit – DC/DC Section.

Note: * Marked components are optional.

4 Circuit Description

The circuit shown in Figures 3 and 4 utilizes the PFS7526H, the LNK6779E devices from Power Integrations in a 20 V, 150 W power factor corrected isolated flyback power supply intended to power an AIO power supply.

4.1 Input EMI Filter and Rectifier

Fuse F1 provides overcurrent protection to the circuit and isolates it from the AC supply in the event of a fault. Diode bridge BR1 rectifies the AC input. Capacitors C2, C3, C4 and C6, in conjunction with inductors L1 and L4, constitute the EMI filter for attenuating both common mode and differential mode conducted noise. Film capacitor C7 provides input decoupling charge storage to reduce input ripple current at the switching frequencies and harmonics. Common mode choke LW has high leakage inductance used to minimize the resonance in the input current waveform.

Resistors R1, R2 and R3 are provided to discharge the EMI filter capacitors after line voltage has been removed from the circuit.

NTC thermistor RT1 limits inrush current of the supply when line voltage is first applied.

Metal oxide varistor (MOV) RV1 protects the circuit during line surge events by effectively clamping the input voltage seen by the power supply.

4.2 PFS7526H Boost Converter

The boost converter stage consists of the boost inductor T1 and the PFS7526H IC U1. This converter stage operates as a PFC boost converter, thereby maintaining a sinusoidal input current to the power supply while regulating the output DC voltage.

During start-up, diode D1 provides an inrush current path to the output capacitor C15, bypassing the switching inductor T1 and switch U1 in order to prevent a resonant interaction between the switching inductor and output capacitor.

Capacitor C13 provide a short, high-frequency return path to RTN for improved EMI results and to reduce U1 MOSFET drain voltage overshoot during turn-off. Capacitor C8 decouples and bypasses the U1 VCC pin.

Capacitor C9 on the REF pin of U1 is a noise decoupler for the internal reference and also programs the output power for either full mode, 100% of rated power [C9 = 1 μF] or efficiency mode, 80% [C9 = 0.1 μF] of rated power.

Since this design requires no standby solution, a high-voltage start-up circuit was used in order to power the PFC stage at start-up. Once the LinkSwitchHP stage is running, the bias winding will supply the V_{CC} to PFC stage by taking over the high-voltage start-up

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circuit. Ressitor R14, R15, R16, Q2, R17 and VR1 form the high-voltage start-up circuit. Depletion mode MOSFET was used for Q2 inorder to reduce no-load or light load consumption.

4.3 PFC Input Feed Forward Sense Circuit

The input voltage of the power supply is sensed by the IC U1 using resistors R4, R5, R6 and R7. The capacitor C10 bypasses the V pin on IC U1.

4.4 PFC Output Feedback

An output voltage resistive divider network consisting of resistors R10, R11, R12, and R13 provide a scaled voltage proportional to the output voltage as feedback to the controller IC U1 setting the PFC output at 385 V. Capacitor C14 decouples the U1 FB pin.

Resistor R9 and capacitor C12 provide the control loop dominant pole. Capactior C11, attenuates high-frequency noise.

4.5 LinkSwitch-HP Primary

The schematic in Figure 4 depicts a 20 V, 150 W LinkSwitch-HP based flyback DC-DC converter implemented using the LNK6779E. The LNK6779E device (U2) integrates an oscillator, an error amplifier and multi-mode control circuit, start-up and protection circuitry and a high-voltage power MOSFET all in one monolithic IC.

One side of the power transformer is connected to the high-voltage bus and the other side is connected to the DRAIN (D) pin of U2. At the start of a switching cycle, the controller turns the power MOSFET on and current ramps up in the primary winding, which stores energy in the core of the transformer. When that current reaches the limit threshold which is set by the output of internal error amplifier (COMPENSATION (CP) pin voltage), the controller turns the power MOSFET off. Due to the phasing of the transformer windings and the orientation of the output diode, the stored energy then induces a voltage across the secondary winding, which forward biases the output diode, and the stored energy is delivered to the output capacitor.

Capacitor C20 (4.7 μF) connected to the BYPASS (BP) pin sets overvoltage protection (OVP) and over-temperature protection (OTP) to latching and lost regulation protection to automatic restart attempts (auto-restart) after a given off-period (typ. 1500 ms).

4.6 Primary RZCD Clamp

Diode D3, VR3, C16 and R19 form a RZCD snubber that is used to limit the voltage stress across the LinkSwitch-HP. Peak drain voltage is therefore limited to typically less than 610 V providing significant margin to the 700 V drain voltage (BVDSS).

Zener diode VR3 prevents the capacitor C16 from fully discharging every switching cycle to reduce power consumption during standby operation.

4.7 Output Rectification

Output rectification of 20 V output is provided by diode D8, D9 and filtering is provided by capacitor C26, C27 and inductor L5 and C28. The snubber formed by R30, R31 and C25 provides high frequency filtering for improved EMI.

4.8 External Current Limit Setting

The maximum cycle-by-cycle current limit is set by the resistor R20 connected to the PROGRAM (PD) pin. A 124 kΩ resistor in the design sets the maximum current limit to 100% of the LNK6779E's default current limit.

4.9 Feedback and Compensation Network

Secondary side regulation was used for this design instead of primary side regulation because of its no-load consumption (<200 mW) and transient response requirements (±2.5%).

4.10 Primary Side Regulation

The output voltage is sensed through bias winding and resistor divider (R27 and R29) during the flyback period. The sensed output voltage is compared to the FEEDBACK (FB) pin threshold to regulate the output or to stop switching in case an overvoltage condition is detected (OVP). Voltage divider R28 and R29 is used to indirectly monitor the bus voltage during the integrated power MOSFET on-time.

The voltage sensed at the FB pin produces a control voltage at the CP pin. Resistor R21 and capacitors C18 and C19 are used for control loop compensation. The operating peak primary current and the operating switching frequency are determined by the CP pin voltage.

4.11 Secondary Side Regulation

The output voltage is controlled using shunt regulator U3. Resistors R36 and R37 sense the output voltage, forming a resistor divider connected to the reference input of IC U2. Changes in the output voltage and hence the voltage at the reference input of U2 results in changes in the cathode voltage of IC U2 and therefore optocoupler U5 LED current. This changes the voltage on CP pin of U2 and acts to maintain output voltage regulation.

The voltage sensed at the output was used to produce a control voltage at the CP pin. Resistor R21, R22, R32, R35 and capacitors C19, C30, C31 are used for control loop compensation. The operating peak primary current and the operating switching frequency are determined by the CP pin voltage.

SSR control circuit (primary side of optocoupler feedback circuit) consist of Q4, R23, U5, R24, R25, D7, C33 and Q3. The PSR feedback (consist of R27, D5 and R29) should be in place even though SSR control circuit is available. However, the FB pin divider network (PSR feedback R27 and R29) ratio should be set to deliver higher output voltage than the

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targeted regulation V_{OUT}, that set by the SSR feedback circuit. PSR feedback circuit will drive the transconductance amplifier to deliver a higher output voltage set by PSR feedback circuit and the SSR feedback circuit will override the transconductance amplifier output and regulate the output voltage at set V_{OUT} regulation level.

Since the FB pin divider network is set to deliver higher output voltage than the actual regulated output (set by SSR), a lost regulation fault is detected by the IC. The LinkSwitch-HP IC reacts under a lost regulation fault, by the PROGRAM pin voltage cycling 128 times between VPD (DL) (typ. 0.5 V) and VPD(DU) (typ. 1.2 V). Then the power supply will stop switching after this 128 cycle times because of the lost regulation fault.

Diode D7 is used to clamp the voltage from optocoupler emitter to ground in order to avoid overdriving of Q4 (maximum voltage on the optocoupler emitter will be the voltage drop of D7 plus the V_{BE} of Q3).

If D7 is not used, during a load transient from full load to no-load the U5B transistor will get saturated and voltage at the U5B can exceed 6 V. When the voltage exceeds 6 V at U5B emitter w.r.t. ground, it will over drive the Q4 and it will raise the voltage at Q4 emitter w.r.t. ground to a higher level and causes CP pin voltage to rise to a higher level and output voltage will go out of regulation. Once it over drives it will latch on to that condition for ever.

Resistor R23 and R25 sets a gain of 1 along with Q3 and Q4 and voltage across R23 will be approximately 300 mV at no-load. This is well below the minimum voltage on the CP pin at no-load.

5 PCB Layout

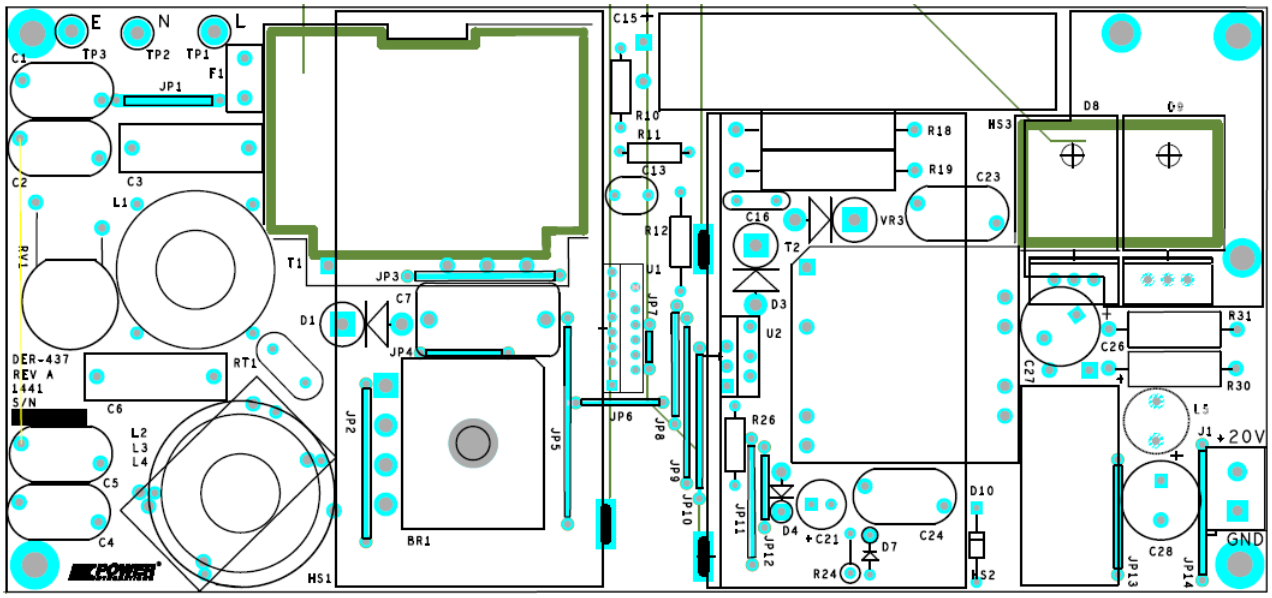

Figure 5 – Printed Circuit Layout – Top Side.

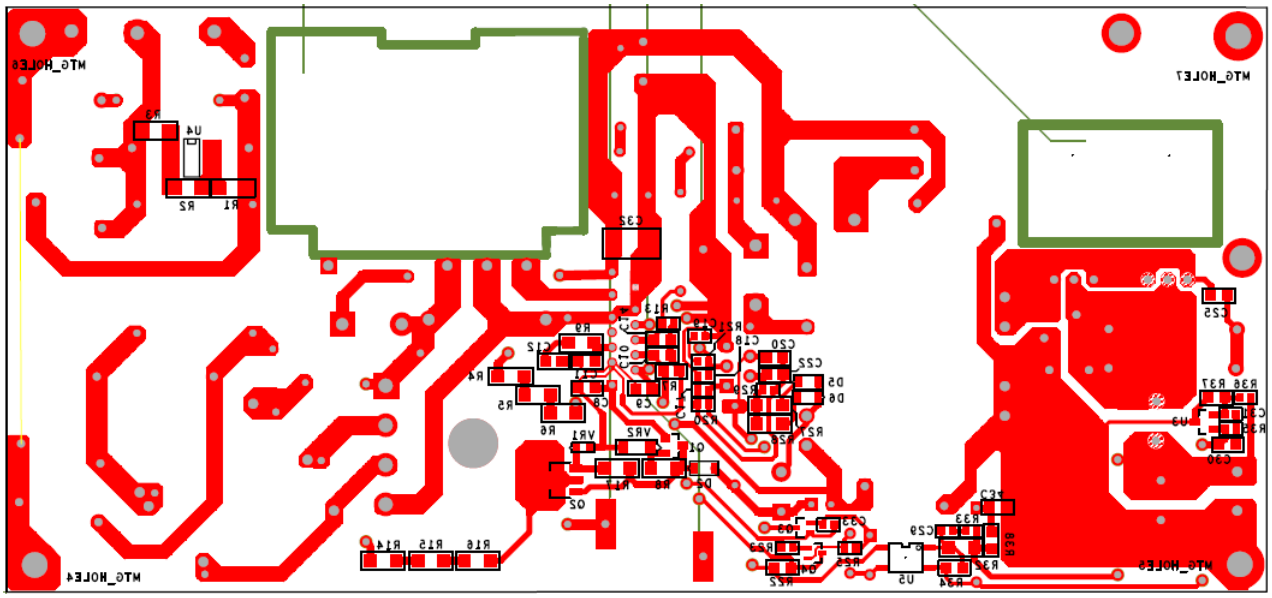

Figure 6 – Printed Circuit Layout – Bottom Side.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	800 V, 8 A, Bridge Rectifier, GBU Case	GBU8K-BP	Micro Commercial
2	5	C2 C4 C23	1 nF, Ceramic, Y1	440LD10-R	Vishay
3	2	C3 C6	220 nF, 275VAC, Film, X2	R46KI322050M2K	Kemet
4	1	C7	1.0 µF, 450 V, METALPOLYPRO	ECW-F2W105JA	Panasonic
5	2	C8 C9	1 µF,50 V, Ceramic, X7R, 0805	C2012X7R1H105M	TDK
6	2	C10 C14	470 pF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB471	Yageo
7	1	C11	100 nF, 25 V, Ceramic, X7R, 0805	08053C104KAT2A	AVX
8	1	C12	1 µF, 25 V, Ceramic, X5R, 0805	C2012X5R1E105K	TDK
9	1	C13	10 nF, 1 kV, Disc Ceramic, X7R	SV01AC103KAR	AVX
10	1	C15	82 µF, 450 V, Electrolytic, (12.5 x 52)	UPZ2W820MNY9	Nichicon
11	1	C16	2.2 nF, 1 kV, Disc Ceramic	NCD222K1KVY5FF	NIC
12	1	C17	33 nF 50 V, Ceramic, X7R, 0603	GRM188R71H333KA61D	Murata
13	1	C19	1 µF 16 V, Ceramic, X7R, 0603	C1608X7R1C105M	TDK
14	1	C20	4.7 µF, 10 V, Ceramic, X7R, 0805	C0805C475K8PACTU	Kemet
15	1	C21	100 µF, 35 V, Electrolytic, Gen. Purpose, (6.3 x 11)	EKMG350ELL101MF11D	Nippon Chemi-Con
16	1	C25	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
17	1	C26	390 µF, 25 V, Al Organic Polymer, Gen. Purpose, 20% 10 x 11.5	APSG250ELL391MJB5S	United Chemi-Con
18	1	C27	3300 µF, 25 V, Electrolytic, Gen Purpose, (12.5 x 27)	EEU-HD1E332B	Panasonic
19	1	C28	470 µF, 25 V, Electrolytic, Gen. Purpose, (10 x 12.5)	EKMG250ELL471MJC5S	Nippon Chemi-Con
20	1	C29	2.2 nF 50 V, Ceramic, X7R, 0603	C0603C222K5RACTU	Yageo
21	1	C30	2.2 nF, 50 V, Ceramic, X7R, 0805	08055C222KAT2A	AVX
22	1	C32	10 nF, 1k V, Ceramic, X7R, 1812	VJ1812Y103KXGAT	Vishay
23	2	C31 C33	100 nF, 25 V, Ceramic, X7R, 0603	VJ0603Y104KNXAO	Vishay
24	1	C34	2.2 µF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
25	1	CLIP_LCS_PFS1	Heat Sink Hardware, Clip LCS/PFS	EM-285V0	Kang Yang Hardware
26	1	D1	1000 V, 3 A, Recitifier, DO-201AD	1N5408-T	Diodes, Inc.
27	1	D2	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
28	1	D3	800 V, 3 A, Ultrafast Recovery, 50 ns, DO-201AD	UF5407-E3/1	Vishay
29	1	D4	200 V, 1 A, Ultrafast Recovery, 50 ns, DO-41	UF4003-E3	Vishay
30	2	D5 D6	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
31	2	D7 D10	75 V, 300 mA, Fast Switching, DO-35	1N4148TR	Vishay
32	2	D8 D9	200 V, 5 A, Dual Schotkky, TO-220AB	SBR10U200CT	ST Micro
33	1	ESIP CLIP1	Heat Sink Hardware, Edge Clip, 14.33 mm L x 6.35 mm W	TRK-24	Kang Yang Hardware
34	1	F1	3.15 A, 250V, Slow, RST	507-1181	Belfuse
35	1	HS1	FAB, Heat Sink, Diodes, DER437		
36	1	HS2	FAB, Heat Sink, Diodes, DER437		
37	1	HS3	FAB, Heat Sink, Diodes, DER437		Custom
38	1	J1	CONN TERM BLOCK, 2 POS, 5 mm, PCB	ED500/2DS	On Shore Tech
39	3	JP1 JP8 JP11	Wire Jumper, Insulated, TFE, #22 AWG, 0.6 in	C2004-12-02	Alpha
40	2	JP2 JP3	Wire Jumper, Insulated, TFE, #22 AWG, 0.8 in	C2004-12-02	Alpha
41	4	JP4 JP6 JP12 JP13	Wire Jumper, Insulated, TFE, #22 AWG, 0.5 in	C2004-12-02	Alpha
42	1	JP5	Wire Jumper, Insulated, TFE, #22 AWG, 1.0 in	C2004-12-02	Alpha
43	1	JP7	Wire Jumper, Insulated, TFE, #22 AWG, 0.3 in	C2004-12-02	Alpha
44	2	JP9 JP10	Wire Jumper, Insulated, TFE, #22 AWG, 0.9 in	C2004-12-02	Alpha
45	1	JP14	Wire Jumper, Insulated, TFE, #22 AWG, 0.7 in	C2004-12-02	Alpha
46	2	L1	10 mH, Common Mode Choke		Custom
47	1	L4	10 mH, 1.6 A, Common Mode Choke	B82732F2162B001	Epcos
48	1	L5	1.5 µH, 8.5 A, 9 x 12 mm	RL622-1R5K-RC	JW MIller
49	1	Q1	NPN, Small Signal BJT, GP SS, 40 V, 0.6 A, SOT-23	MMBT4401LT1G	Diodes, Inc.

50	1	Q2	MOSFET N-CH 500 V 230 mA 3SOT-89	DN2450N8-G	Microchip Tech
51	2	Q3 Q4	NPN, Small Signal BJT, 40 V, 0.2 A, SOT-323	MMST3904-7-F	Diodes, Inc.
52	3	R1-R3	510 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ514V	Panasonic
53	2	R4 R5	6.2 MΩ, 1%, 1/4 W, Thick Film, 1206	KTR18EZPF6204	Rohm
54	1	R6	3.74 MΩ, 1%, 1/4 W, Thick Film, 1206	CRCW12063M74FKEA	Vishay
55	1	R7	162 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1623V	Panasonic
56	1	R8	10 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ103V	Panasonic
57	1	R9	30.1 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF3012V	Panasonic
58	1	R10	3.74 MΩ, 1%, 1/4 W, Metal Film	MFR-25FBF52-3M74	Yageo
59	2	R11 R12	6.2 MΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-6M2	Yageo
60	1	R13	162 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1623V	Panasonic
61	3	R14-R16	7.5 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ752V	Panasonic
62	1	R17	1.3 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ135V	Panasonic
63	1	R19	3.3 kΩ, 5%, 2 W, Metal Oxide	RSF200JB-3K3	Yageo
64	1	R20	124 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1243V	Panasonic
65	1	R21	12 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ123V	Panasonic
66	1	R22	24.9 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2492V	Panasonic
67	2	R23 R25	1 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
68	1	R24	1 kΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-1K0	Yageo
69	1	R26	5.6 kΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-5K6	Yageo
70	1	R27	73.2 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF7322V	Panasonic
71	1	R28	196 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1963V	Panasonic
72	1	R29	8.45 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF8451V	Panasonic
73	2	R30 R31	10 Ω, 5%, 2 W, Metal Oxide	RSF200JB-10R	Yageo
74	1	R32	2.7 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ272V	Panasonic
75	1	R34	1 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ102V	Panasonic
76	1	R35	200 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ204V	Panasonic
77	1	R36	75.0 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF7502V	Panasonic
78	1	R37	10.7 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1072V	Panasonic
79	1	R38	10 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ103V	Panasonic
80	1	RT1	NTC Thermistor, 2.5 Ω, 5 A	SL10 2R505	Ametherm
81	2	RTV1 RTV3	Thermally conductive Silicone Grease	120-SA	Wakefield
82	1	RV1	320 V, 23 J, 10 mm, RADIAL	V320LA10P	Littlefuse
83	8	SCREW2 SCREW3 SCREW5 SCREW7-SCREW10 SCREW12	SCREW MACHINE PHIL 4-40 X 1/4 SS	PMSSS 440 0025 PH	Building Fasteners
84	1	SCREW11	SCREW MACHINE PHIL 4-40X 3/16 SS	67413609	MSC Industrial
85	4	STDOFF1-STDOFF4	Standoff Hex, 4-40, 0.375" L, Al, F/F	1892	Keystone
86	1	T1	Bobbin, Vertical, 10pins		
87	1	T2	Bobbin, PQ26/20, Vertical, 12 pins	BPQ26/20-1112CPFR	TDK
88	2	TO-220 PAD1 TO-220 PAD2	THERMAL PAD TO-220 .009" SP1000	1009-58	Bergquist
89	1	TP1	Test Point, BLK,THRU-HOLE MOUNT	5011	Keystone
90	1	TP2	Test Point, WHT,THRU-HOLE MOUNT	5012	Keystone
91	1	TP3	Test Point, YEL,THRU-HOLE MOUNT	5014	Keystone
92	1	U1	HiperPFS-3, eSIP16/13	PFS7526H	Power Integrations
93	1	U2	LinkSwitch-HP, eSIP-7F	LNK6779E	Power Integrations
94	1	U3	2.4 V Shunt Regulator IC, 1%, 0 to 70C, SOT-23-3	NCP431ACSNT1G	ON Semi
95	1	U5	Optocoupler, 80 V, CTR 80-160%, 4-Mini Flat	PC357N1TJ00F	Sharp
96	1	VR1	9.1 V, 5%, 150 mW, SSMINI-2	DZ2S091M0L	Panasonic
97	1	VR2	13 V, 5%, 500 Mw, SOD-123	MMSZ4700T1G	ON Semi
98	1	VR3	150 V, 1500W, TVS, 1500W 5% UNI AXL	1.5KE150A	LittleFuse

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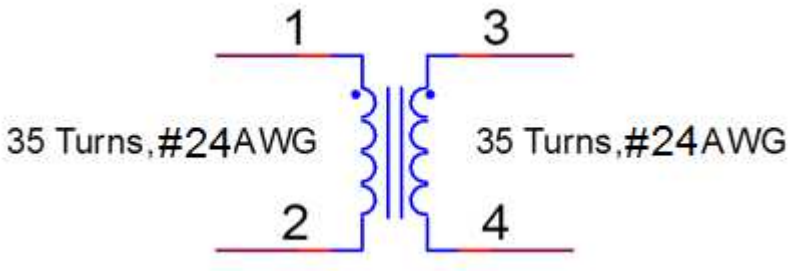
99	3	WASHER1 WASHER2 WASHER9	WASHER FLAT #4 Zinc, OD 0.219, ID 0.125, Thk 0.032,Yellow Chromate Finish	5205820-2	Tyco
100	2	WASHER8 WASHER10	Washer Nylon Shoulder #4	3049	Keystone

7 Magnetics

7.1 Common Mode Choke Specification (L1)

7.1.1 Electrical Diagram



7.1.2 Electrical Specifications

Inductance	Pins 1-2, 3-4 measured at 10 kHz	10 mH ±25%

7.1.3 Material List

Item	Description
[1]	Core: JL15 (JLW ELECTRONICS (HONG KONG) LIMITED). AL = 9000 nH/N2. Mfg P/N: T18x10x7C-JL15*. PI P/N: 30-00398-00.
[2]	Divider -- Fish paper, insulating cotton rag, 0.010” thick, PI #: 66-00042-00. Cut to size 0.383”x0.293”.
[3]	Magnetic Wire: #24 AWG.
[4]	Number of Turns: 35 each section.

*T18x10x7C is the physical size, JL15 is the core type
Note: Leakage inductance is about 30 µH.

7.1.4 Winding Instruction

1. Insert the divider (see details below) in the core to divide into 2 sections equally.

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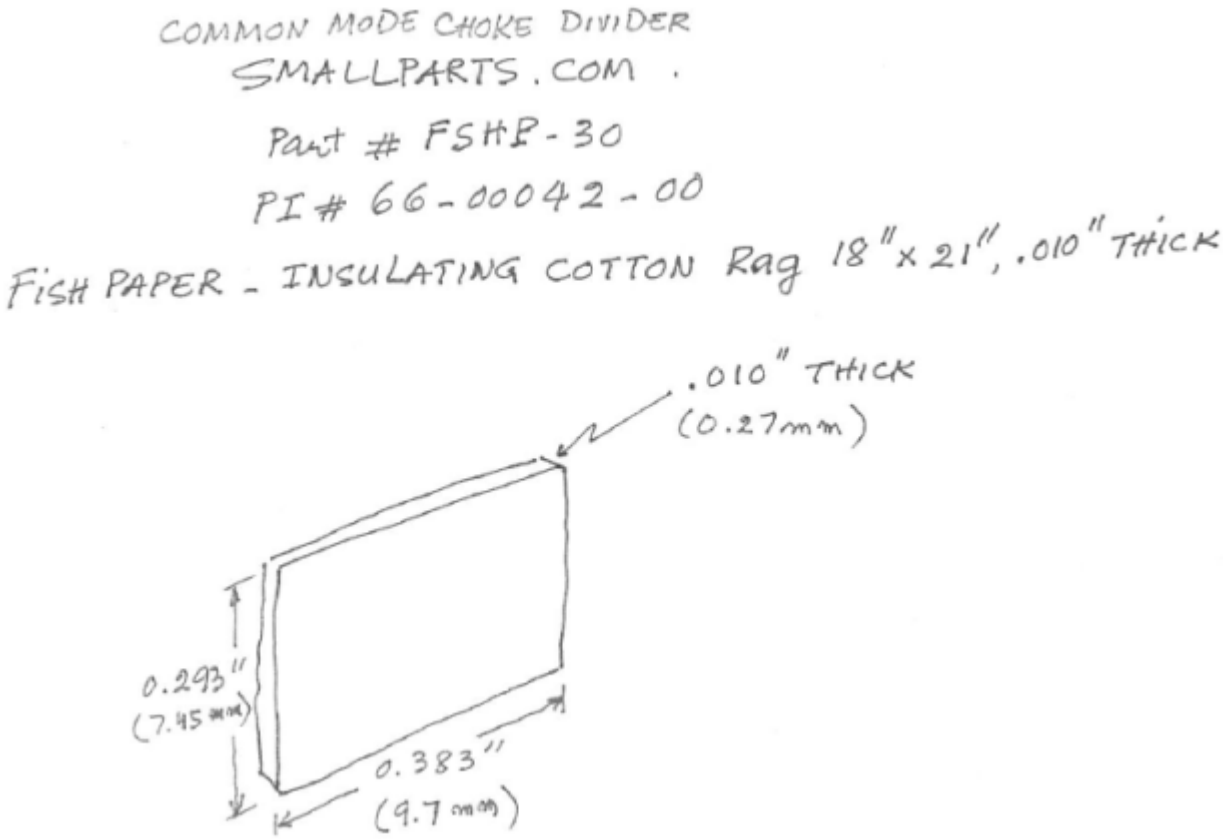
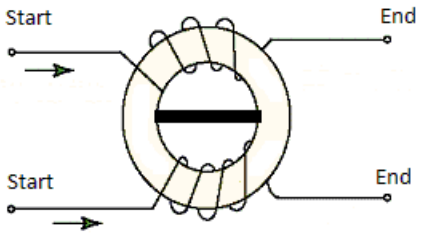


2. Start winding on one section with 28 turns or completely fill up the section for the 1st layer, then equally spread the remaining turns for the 2nd layer.

3. Repeat step 2 for the other section winding. Make sure it starts from the SAME side and winding direction as step 2. See picture below.



7.2 PFC Choke Specification (T1)

7.2.1 Electrical Diagram

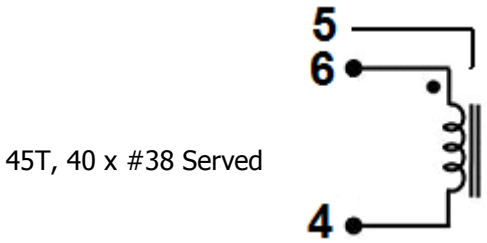


Figure 7 – PFC Choke Electrical Diagram.

7.2.2 Electrical Specifications

Inductance	Pins 1-2 measured at 100 kHz, 0.4 RMS.	440 µH +5%

7.2.3 Material List

Item	Description
[1]	Core: TDG Core, PC40 ±25%.
[2]	Bobbin: PQ38/12, from TDG. P/N: PQ38/12.
[3]	Wire: Served Litz 40/#38.
[4]	Tape, Polyester Web 3M, 4.5 mm wide, 5 mil Thick.
[5]	Bus wire, #24 AWG (connect to pin 5).

7.2.4 Inductor Construction

Winding Preparation	Place the bobbin on the mandrel with the pin side is on the left side. Winding direction is clockwise direction.
Winding #1	Starting at pin 6, wind 45 turns of served Litz wire item [3], finish at pin 4.
Insulation	Apply 3 layers of tape item [4].
Assembly	Grind both cores to specified inductance.
Final Assembly	Solder a wire of item [5] at pin 5, and then attach the other end of the wire to the bottom side of the core. Secure the wire and the core halves.

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7.3 Transformer Specification (T2)

7.3.1 Electrical Diagram

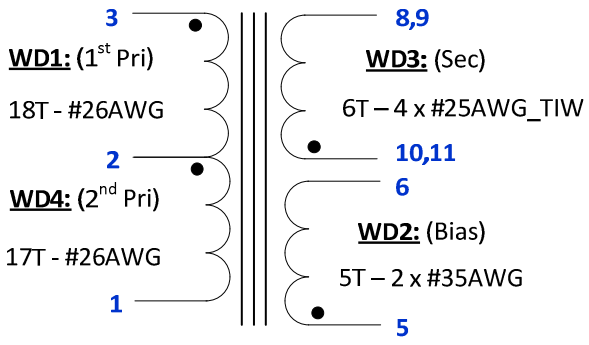

Figure 8 – Transformer Electrical Diagram.

7.3.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1-6 to pins 8-11.	3000 VAC
Primary Inductance	Pins 1-3, all other open, measured at 100 kHz, 0.4 V_{RMS}.	480 µH ±5%
Resonant Frequency	Pins 1-3, all other open	2400 kHz (Min.)
Primary Leakage	Pins 1-3, with pins 8-11 shorted, measured at 100 kHz, 0.4V_{RMS}.	3.5 µH (Max.)

7.3.3 Material List

Item	Description
[1]	Core: PQ26/20, TDK-PC95, gapped for ALG of 390nH/T².
[2]	Bobbin: PQ26/20, Vertical, 12 pins (6/6), TDK; or equivalent.
[3]	Magnet wire: #26 AWG Double Coated, Solderable.
[4]	Magnet wire: #35 AWG Double Coated, Solderable.
[5]	Magnet wire: #25 AWG Triple Insulated Wire.
[6]	Tape: 3M 1298 Polyester Film, 2 mil Thick, 9.0 mm Wide.
[7]	Varnish.

7.3.4 Transformer Build Diagram

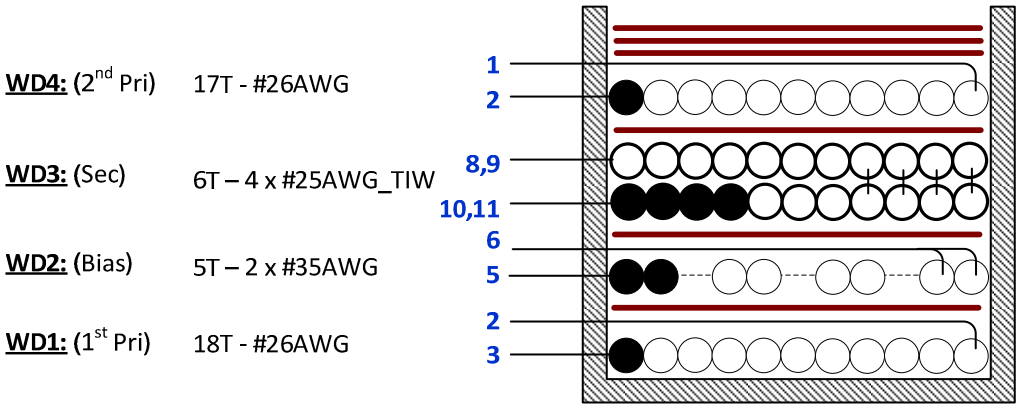

Figure 9 – Transformer Build Diagram.

7.3.5 Transformer Build Instructions

Winding preparation	Position the bobbin item [2] on the mandrel such that the pin side is on the left. Winding direction is clock-wise direction.
WD1 1st Half Primary	Start at pin 3, wind 18 turns of wire item [3] in 1 layer with tight tension, and finish at pin 2.
Insulation	Place 1 layer of tape item [6].
WD2 Bias	Start at pin 5, wind 5 bifilar turns of wire item [4] in 1 layer, spread wire evenly on the bobbin, and finish at pin 6.
Insulation	Place 1 layer of tape item [6].
WD3 Secondary	Start at pin 10,11, wind 6 quadfilar turns of wire item [5] in 2 layers with tight tension, and finish at pin 8,9 (note: terminate 2 wires per pin).
Insulation	Place 1 layer of tape item [6].
WD4 2nd Half Primary	Start at pin 2, wind 17 turns of wire item [3] in 1 layer with tight tension, and finish at pin 1.
Insulation	Place 3 layers of tape item [6].

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8 Magnetics Design Spreadsheets

8.1 HiperPFS-3 Design Spreadsheet

Hiper_PFS-3_Boost_012815; Rev.0.6; Copyright Power Integrations 2015	**INPUT**	**INFO**	**OUTPUT**	**UNITS**	**Hiper_PFS-3_Boost_012815_Rev0-6.xls; Continuous Mode Boost Converter Design Spreadsheet**
Enter Application Variables					
Input Voltage Range	**Universal**		**Universal**		**Input voltage range**
VACMIN	90		90	VAC	Minimum AC input voltage. Spreadsheet simulation is performed at this voltage. To examine operation at other votlages, enter here, but enter fixed value for LPFC_ACTUAL.
VACMAX	264		264	VAC	Maximum AC input voltage
VBROWNIN			76	VAC	Expected Minimum Brown-in Voltage
VBROWNOUT			72	VAC	Specify brownout voltage.
VO			385	VDC	Nominal load voltage
PO	168		168	W	Nominal Output power
fL			50	Hz	Line frequency
TA Max			40	°C	Maximum ambient temperature
n			0.93		Enter the efficiency estimate for the boost converter at VACMIN. Should approximately match calculated efficiency in Loss Budget section
VO_MIN			366	VDC	Minimum Output voltage
VO_RIPPLE_MAX			20	VDC	Maximum Output voltage ripple
tHOLDUP	17		17	ms	Holdup time
VHOLDUP_MIN	280		280	VDC	Minimum Voltage Output can drop to during holdup
I_INRUSH			40	A	Maximum allowable inrush current
Forced Air Cooling	**No**		**No**		Enter "Yes" for Forced air cooling. Otherwise enter "No". Forced air reduces acceptable choke current density and core autopick core size
KP and INDUCTANCE					
KP_TARGET	0.628		0.628		Target ripple to peak inductor current ratio at the peak of VACMIN. Affects inductance value
LPFC_TARGET (0 bias)			440	uH	PFC inductance required to hit KP_TARGET at peak of VACMIN and full load
LPFC_DESIRED (0 bias)			440	uH	LPFC value used for calculations. Leave blank to use LPFC_TARGET. Enter value to hold constant (also enter core selection) while changing VACMIN to examine brownout operation. Calculated inductance with rounded (integral) turns for powder core.
KP_ACTUAL			0.606		Actual KP calculated from LPFC_ACTUAL
LPFC_PEAK			440	uH	Inductance at VACMIN, 90°. For Ferrite, same as LPFC_DESIRED (0 bias)
Basic current parameters					
IAC_RMS			2.01	A	AC input RMS current at VACMIN and Full Power load
IO_DC			0.44	A	Output average current/Average diode current
PFS Parameters					
PFS Part Number	**PFS7526H**		**PFS7526H**		If examining brownout operation, over-ride autopick with desired device size
Operating Mode	**Full Power**		**Full Power**		Mode of operation of PFS. For Full Power mode enter "Full Power" otherwise enter "EFFICIENCY" to indicate efficiency mode
IOCP min			6.8	A	Minimum Current limit
IOCP typ			7.2	A	Typical current limit

IOCP max			7.5	A	Maximum current limit
IP			3.91	A	MOSFET peak current
IRMS			1.72	A	PFS MOSFET RMS current
RDSON			0.62	Ohms	Typical RDSon at 100 'C
FS_PK			74	kHz	Estimated frequency of operation at crest of input voltage (at VACMIN)
FS_AVG			55	kHz	Estimated average frequency of operation over line cycle (at VACMIN)
PCOND_LOSS_PFS			1.8	W	Estimated PFS conduction losses
PSW_LOSS_PFS			1.6	W	Estimated PFS switching losses
PFS_TOTAL			3.5	W	Total Estimated PFS losses
TJ Max			100	deg C	Maximum steady-state junction temperature
Rth-JS			2.80	°C/W	Maximum thermal resistance (Junction to heatsink)
HEATSINK Theta-CA			11.25	°C/W	Maximum thermal resistance of heatsink
INDUCTOR DESIGN					
Basic Inductor Parameters					
LPFC (0 Bias)			440	uH	Value of PFC inductor at zero current. This is the value measured with LCR meter. For powder, it will be different than LPFC.
LP_TOL	5.0		5.0	%	Tolerance of PFC Inductor Value (ferrite only)
IL_RMS			2.00	A	Inductor RMS current (calculated at VACMIN and Full Power Load)
Material and Dimensions					
Core Type	**Ferrite**		**Ferrite**		Enter "Sendust", "Pow Iron" or "Ferrite"
Core Material	**PC44/PC95**		**PC44/PC95**		Select from 60u, 75u, 90u or 125 u for Sendust cores. Fixed at PC44/PC95 for Ferrite cores. Fixed at -52 material for Pow Iron cores.
Core Geometry	**PQ**		**PQ**		Toroid only for Sendust and Powdered Iron; EE or PQ for Ferrite cores.
Core	**Auto**		**PQ32/20**		Core part number
Ae	129.70		129.70	mm^2	Core cross sectional area
Le	43.50		43.50	mm	Core mean path length
AL	4000.00		4000.00	nH/t^2	Core AL value
Ve	5.64		5.64	cm^3	Core volume
HT (EE/PQ) / ID (toroid)	7.50		7.50	mm	Core height/Height of window; ID if toroid
MLT	7.3		7.3	mm	Mean length per turn
BW	4.70		4.70	mm	Bobbin width
LG			0.67	mm	Gap length (Ferrite cores only)
Flux and MMF calculations					
BP_TARGET (ferrite only)	6000	Info	6000	Gauss	Info: Peak flux density is too high. Check for Inductor saturation during line transient operation
B_OCP (or BP)		Warning	5942	Gauss	Warning: Peak flux density is too high. Check for Inductor saturation during load steps
B_MAX			3122	Gauss	peak flux density at AC peak, VACMIN and Full Power Load, nominal inductance
µ_TARGET (powder only)			N/A	%	target µ at peak current divided by µ at zero current, at VACMIN, full load (powder only) - drives auto core selection
µ_MAX (powder only)			N/A	%	mu_max greater than 75% indicates a very large core. Please verify
µ_OCP (powder only)			N/A	%	µ at IOCPtyp divided by µ at zero current
I_TEST	4.9		4.9	A	Current at which B_TEST and H_TEST are calculated, for checking flux at a current other than IOCP or IP; if blank IOCP_typ is used.
B_TEST			3882	Gauss	Flux density at I_TEST and maximum tolerance inductance

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μ_TEST (powder only)			N/A	%	μ at IOCP divided by μ at zero current, at IOCPtyp
Wire					
TURNS			45		Inductor turns. To adjust turns, change BP_TARGET (ferrite) or μ_TARGET (powder)
ILRMS			2.00	A	Inductor RMS current
Wire type	**Litz**		**Litz**		Select between "Litz" or "Magnet" for double coated magnet wire
AWG	38	Info	38	AWG	!!! Info. Selected wire gauge is too thick and may caused increased losses due to skin effect. Consider using multiple strands of thinner wires or Litz wire
Filar	40		40		Inductor wire number of parallel strands. Leave blank to auto-calc for Litz
OD (per strand)			0.102	mm	Outer diameter of single strand of wire
OD bundle (Litz only)			0.90	mm	Will be different than OD if Litz
DCR			0.23	ohm	Choke DC Resistance
P AC Resistance Ratio		Info	2.06		AC resistance is high. Check copper loss, use Litz or thinner wire and fewer layers, or reduce Kp
J		Warning	6.19	A/mm^2	Current density is high, if copper loss is high use thicker wire, more strands, or larger core
FIT		Warning	103%	%	!!! Warning. Windings may not fit on this inductor. Use bigger core or reduce KP or reduce wire gauge if possible
Layers			7.75		Estimated layers in winding
Loss calculations					
BAC-p-p			1961	Gauss	Core AC peak-peak flux excursion at VACMIN, peak of sine wave
LPFC_CORE_LOSS			0.64	W	Estimated Inductor core Loss
LPFC_COPPER_LOSS			1.93	W	Estimated Inductor copper losses
LPFC_TOTAL_LOSS			2.57	W	Total estimated Inductor Losses
Built-in PFC Diode					
PFC Diode Part Number			INTERNAL1		PFC Diode Part Number
Type			SPECIAL		PFD Diode Type
Manufacturer			PI		Diode Manufacturer
VRRM			530	V	Diode rated reverse voltage
IF			3	A	Diode rated forward current
Qrr			57		high temperature
VF			1.47	V	Diode rated forward voltage drop
PCOND_DIODE			0.64	W	Estimated Diode conduction losses
PSW_DIODE			0.15	W	Estimated Diode switching losses
P_DIODE			0.79	W	Total estimated Diode losses
TJ Max			100	deg C	Maximum steady-state operating temperature
Rth-JS			3.00	degC/W	Maximum thermal resistance (Junction to heatsink)
HEATSINK Theta-CA			11.25	degC/W	Maximum thermal resistance of heatsink
Output Capacitor					
Output Capacitor	**82**		82	uF	Minimum value of Output capacitance
VO_RIPPLE_EXPECTED			18.2	V	Expected ripple voltage on Output with selected Output capacitor
T_HOLDUP_EXPECTED			17.0	ms	Expected holdup time with selected Output capacitor
ESR_LF			2.02	ohms	Low Frequency Capacitor ESR
ESR_HF			0.81	ohms	High Frequency Capacitor ESR
IC_RMS_LF			0.30	A	Low Frequency Capacitor RMS current
IC_RMS_HF			0.77	A	High Frequency Capacitor RMS current
CO_LF_LOSS			0.18	W	Estimated Low Frequency ESR loss in Output capacitor
CO_HF_LOSS			0.49	W	Estimated High frequency ESR loss in Output capacitor
Total CO LOSS			0.66	W	Total estimated losses in Output Capacitor
Input Bridge (BR1) and Fuse (F1)					

I^2t Rating			5.72	A^2*s	Minimum I^2t rating for fuse
Fuse Current rating			2.98	A	Minimum Current rating of fuse
VF			0.90	V	Input bridge Diode forward Diode drop
IAVG			1.85	A	Input average current at 70 VAC.
PIV_INPUT BRIDGE			373	V	Peak inverse voltage of input bridge
PCOND_LOSS_BRIDGE			3.25	W	Estimated Bridge Diode conduction loss
CIN			0.5	uF	Input capacitor. Use metallized polypropylene or film foil type with high ripple current rating
RT			9.33	ohms	Input Thermistor value
D_Precharge			1N5407		Recommended precharge Diode
PFS3 small signal components					
C_REF			1.0	uF	REF pin capacitor value
RV1			4.0	MOhms	Line sense resistor 1
RV2			6.0	MOhms	Line sense resistor 2
RV3			6.0	MOhms	Typical value of the lower resistor connected to the V-PIN. Use 1% resistor only!
RV4			161.6	kOhms	Description pending, could be modified based on feedback chain R1-R4
C_V			0.495	nF	V pin decoupling capacitor (RV4 and C_V should have a time constant of 80us) Pick the closest available capacitance.
C_VCC			1.0	uF	Supply decoupling capacitor
C_C			100	nF	Feedback C pin decoupling capacitor
Power good Vo lower threshold VPG(L)			333	V	Vo lower threshold voltage at which power good signal will trigger
PGT set resistor			333.0	kohm	Power good threshold setting resistor
Feedback Components					
R1			4.0	Mohms	Feedback network, first high voltage divider resistor
R2			6.0	Mohms	Feedback network, second high voltage divider resistor
R3			6.0	Mohms	Feedback network, third high voltage divider resistor
R4			161.6	kohms	Feedback network, lower divider resistor
C1			0.495	nF	Feedback network, loop speedup capacitor. (R4 and C1 should have a time constant of 80us) Pick the closest available capacitance.
R5			19.1	kohms	Feedback network: zero setting resistor
C2			1000	nF	Feedback component- noise suppression capacitor
Loss Budget (Estimated at VACMIN)					
PFS Losses			3.48	W	Total estimated losses in PFS
Boost diode Losses			0.79	W	Total estimated losses in Output Diode
Input Bridge losses			3.25	W	Total estimated losses in input bridge module
Inductor losses			2.57	W	Total estimated losses in PFC choke
Output Capacitor Loss			0.66	W	Total estimated losses in Output capacitor
EMI choke copper loss			0.50	W	Total estimated losses in EMI choke copper
Total losses			10.76	W	Overall loss estimate
Efficiency			0.94		Estimated efficiency at VACMIN, full load.
CAPZero component selection recommendation					
CAPZero Device			CAP002DG		(Optional) Recommended CAPZero device to discharge X-Capacitor with time constant of 1 second
Total Series Resistance (R1+R2)			1.5	k-ohms	Maximum Total Series resistor value to discharge X-Capacitors
EMI filter components recommendation					
CIN_RECOMMENDED	1000		1000	nF	Metallized polyester film capacitor after bridge, ratio with Po
CX2	220		220	nF	X capacitor after differencial mode choke and before bridge, ratio with Po
LDM_calc			208	uH	estimated minimum differencial inductance to avoid <10kHz resonance in input current
CX1	220		220	nF	X capacitor before common mode choke, ratio with Po

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LCM			10	mH	typical common mode choke value
LCM_leakage			30	uH	estimated leakage inductance of CM choke, typical from 30~60uH
CY1 (and CY2)			220	pF	typical Y capacitance for common mode noise suppression
LDM_Actual			178	uH	cal_LDM minus LCM_leakage, utilizing CM leakage inductance as DM choke.
DCR_LCM	0.10		0.10	Ohms	total DCR of CM choke for estimating copper loss
DCR_LDM	0.10		0.10	Ohms	total DCR of DM choke(or CM #2) for estimating copper loss

Note: Peak flux density was calculated using device max current limit, but actual peak current at full load is much less than the device maximum current limit.

8.2 LinkSwitch-HP Design Spreadsheet

ACDC_LinkSwitchHP89_081814; Rev.0.2; Copyright Power Integrations 2014	INPUT	INFO	OUTPUT	UNIT	ACDC_LinkSwitchHP89_081814 Rev 0-2.xls: LinkSwitch-HP Flyback Continuous/Discontinuous Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	264		264	V	Minimum AC Input Voltage
VACMAX	264		264	V	Maximum AC Input Voltage
fL			50	Hz	AC Mains Frequency
VO	20		20	V	Output Voltage (main)
PO	150		150	W	Load Power
n	0.90		0.90		Efficiency Estimate
Z			0.50		Loss Allocation Factor
VB	15		15	V	Bias Voltage
tC			3	ms	Bridge Rectifier Conduction Time Estimate
CIN			150	uF	Input Filter Capacitor
Package	E/V		E/V		E and V Package Selected
Enclosure	Open Frame		Open Frame		Open Frame type enclosure
Heatsink	Metal		Metal		Metallic heatsink thermally connected to the exposed metal on the E-package
ENTER LinkSwitch-HP VARIABLES					
LinkSwitch-HP	LNK6779E		LNK6779E		Manual Device Selection
ILIMITMIN			3.162	A	Minimum Current limit
ILIMITMAX			3.638	A	Maximum current limit
ILIMITMIN_EXT			3.162	A	External Minimum Current limit
ILIMITMAX_EXT			3.638	A	External Maximum current limit
KI	Auto		1		Current limit reduction factor
Rpd			124.00	k-ohm	Program delay Resistor
Cpd			33.00	nF	Program delay Capacitor
Total programmed delay			0.86	sec	Total program delay
fS			132	kHz	LinkSwitch-HP Switching Frequency
fSmin			120	kHz	LinkSwitch-HP Minimum Switching Frequency
fSmax			136	kHz	LinkSwitch-HP Maximum Switching Frequency
KP	0.56		0.56		Ripple to Peak Current Ratio (0.4 < KP < 6.0)
VOR	121.00		121.00	V	Reflected Output Voltage
Voltage Sense					
VUVON			308.00	V	Undervoltage turn on
VUVOFF			124.37	V	Undervoltage turn off
VOV			1402.96	V	Overvoltage threshold
FMAX_FULL_LOAD			136.00	kHz	Maximum switching frequency at full load
FMIN_FULL_LOAD			120.00	kHz	Minimum switching frequency at full load
TSAMPLE_FULL_LOAD			5.12	us	Minimum available Diode conduction time at full load. This should be greater than 2.5 us
TSAMPLE_LIGHT_LOAD			2.89	us	Minimum available Diode conduction time at light load. This should be greater than 1.4 us
VDS		Info	2.60	V	For LNK6XX8/9, RDSON is extrapolated due to lack of real data from Production Engineering.
VD			0.50	V	Output Winding Diode Forward Voltage Drop
VDB	0.70		0.70	V	Bias Winding Diode Forward Voltage Drop
FEEDBACK SENSING SECTION					
RFB1			158.00	k-ohms	Feedback divider upper resistor

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RFB2			23.20	k-ohms	Feedback divider lowerr resistor
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Select Core Size	Auto		Auto		Auto Core Selection
Core			EE40		Selected Core
Custom Core	PQ26/20				Enter name of custom core is applicable
AE	1.19		1.19	cm^2	Core Effective Cross Sectional Area
LE	4.63		4.63	cm	Core Effective Path Length
AL	5490		5490	nH/T^2	Ungapped Core Effective Inductance
BW	9.2		9.2	mm	Bobbin Physical Winding Width
M			0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L			2		Number of Primary Layers
NS	6		6		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN	280		280	V	Minimum DC Input Voltage
VMAX	385		385	V	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.30		Maximum Duty Cycle
IAVG			0.60	A	Average Primary Current
IP			2.72	A	Peak Primary Current
IR			1.52	A	Primary Ripple Current
IRMS			1.11	A	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP_TYP			480	uH	Typical Primary Inductance
LP_TOL	8		8	%	Primary inductance Tolerance
NP			35		Primary Winding Number of Turns
NB			5		Bias Winding Number of Turns
ALG			383	nH/T^2	Gapped Core Effective Inductance
BM		Warning	3101	Gauss	!!! Warning. Maximum flux density is too high. Increase NS or use larger core
BP		Warning	4476	Gauss	!!! REDUCE BP<3700 (increase NS,smaller LinkSwitch-HP, larger Core,increase KP)
BAC			868	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1700		Relative Permeability of Ungapped Core
LG			0.36	mm	Gap Length (Lg > 0.1 mm)
BWE			18.4	mm	Effective Bobbin Width
OD			0.52	mm	Maximum Primary Wire Diameter including insulation
INS			0.07	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.45	mm	Bare conductor diameter
AWG			26	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			256	Cmils	Bare conductor effective area in circular mils
CMA			231	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE OUTPUT EQUIVALENT)					
Lumped parameters					
ISP			16.07	A	Peak Secondary Current
ISRMS			9.89	A	Secondary RMS Current
IO			7.50	A	Power Supply Output Current
IRIPPLE			6.45	A	Output Capacitor RMS Ripple Current
CMS			1979	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			17	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			1.15	mm	Secondary Minimum Bare Conductor Diameter
ODS			1.53	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS			0.19	mm	Maximum Secondary Insulation Wall Thickness

VOLTAGE STRESS PARAMETERS					
VDRAIN			659	V	Peak voltage acoss drain to source of Linkswitch-HP
PIVS			85	V	Output Rectifier Maximum Peak Inverse Voltage
PIVB			65	V	Bias Rectifier Maximum Peak Inverse Voltage
TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)					
1st output					
VO1			20.00	V	Output Voltage
IO1			7.50	A	Output DC Current
PO1			150	W	Output Power
VD1			0.5	V	Output Diode Forward Voltage Drop
NS1			6.00		Output Winding Number of Turns
ISRMS1			9.893	A	Output Winding RMS Current
IRIPPLE1			6.45	A	Output Capacitor RMS Ripple Current
PIVS1			85	V	Output Rectifier Maximum Peak Inverse Voltage
CMS1			1979	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			17	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			1.15	mm	Minimum Bare Conductor Diameter
ODS1			1.53	mm	Maximum Outside Diameter for Triple Insulated Wire
2nd output					
VO2			0.00	V	Output Voltage
IO2			0.00	A	Output DC Current
PO2			0	W	Output Power
VD2			0.7	V	Output Diode Forward Voltage Drop
NS2			0.20		Output Winding Number of Turns
ISRMS2			0	A	Output Winding RMS Current
IRIPPLE2			0.00	A	Output Capacitor RMS Ripple Current
PIVS2			2	V	Output Rectifier Maximum Peak Inverse Voltage
CMS2			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS2			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS2			N/A	mm	Minimum Bare Conductor Diameter
ODS2			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
3rd output					
VO3			0.00	V	Output Voltage
IO3			0.00	A	Output DC Current
PO3			0	W	Output Power
VD3			0.7	V	Output Diode Forward Voltage Drop
NS3			0.20		Output Winding Number of Turns
ISRMS3			0	A	Output Winding RMS Current
IRIPPLE3			0.00	A	Output Capacitor RMS Ripple Current
PIVS3			2	V	Output Rectifier Maximum Peak Inverse Voltage
CMS3			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS3			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS3			N/A	mm	Minimum Bare Conductor Diameter
ODS3			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
Total power			150	W	Total Power for Multi-output section
Negative Output	N/A		N/A		If negative output exists enter Output number; eg: If VO2 is negative output, enter 2

Note: Peak flux density was calculated using device max current limit, but actual peak current at full load is much less than the device maximum current limit.

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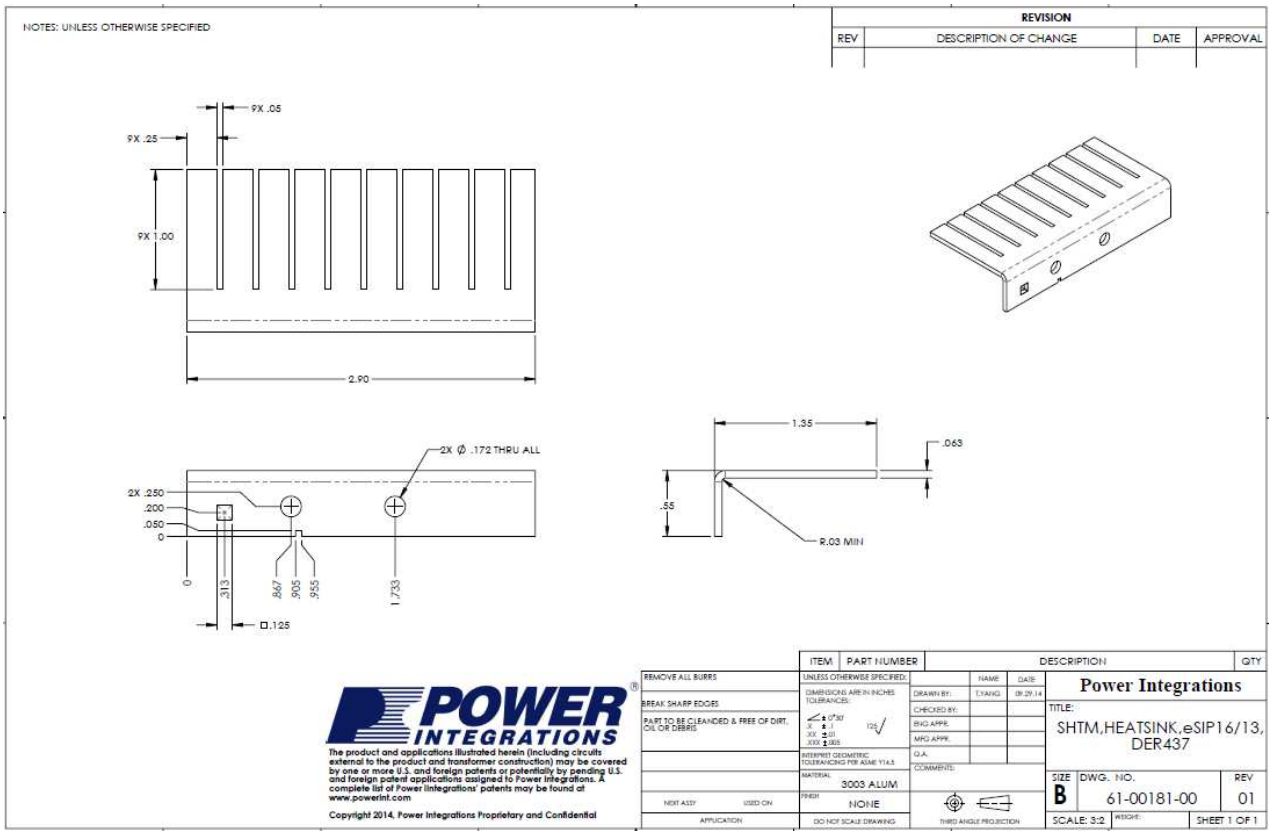
9 Heat Sink Assemblies

9.1 HiperPFS-3 Heat Sink

9.1.1 HiperPFS-3 Heat Sink Fabrication Drawing

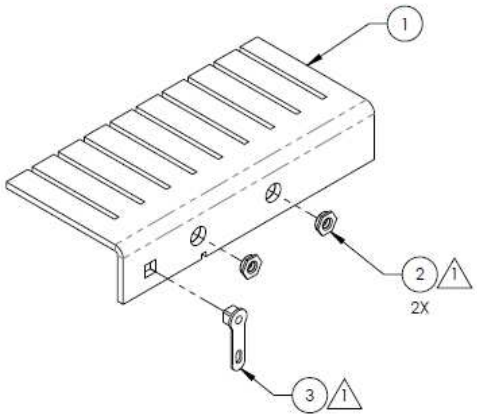


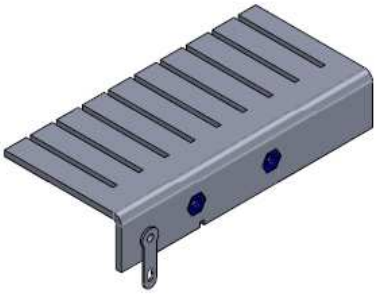
9.1.2 HiperPFS-3 Heat Sink Assembly Drawing

NOTES: UNLESS OTHERWISE SPECIFIED

1. SUPPLIER TO INSTALL FLUSH NUT, ITEM 2 AND EYELET, ITEM 3 TO HEAT SINK, ITEM 1.

REVISION			
REV	DESCRIPTION OF CHANGE	DATE	APPROVAL





ITEM	PART NUMBER	DESCRIPTION	QTY
03	60-00016-00	TERM,EYELET,TIN PLD BRASS,ZIERICK PN 190	1
02	77-00005-00	CAPTIVE NUT,FLUSH,SS,4-40,PNL THK .061 "	2
01	61-00181-00	SHTM,HEATSINK,eSIP16/13,DER427	1

POWER INTEGRATIONS

REMOVE ALL BURRS	
BREAK SHARP EDGES	
PART TO BE CLEANED & FREE OF DIRT, OIL OR DEBRIS	
NEXT ASSY	
USED ON	
APPLICATION	

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES:
± 0°30'
X ±.1
.XX ±.01
.XXX ±.005
125
ASME Y14.5
MATERIAL: SEE BOM
FINISH: NONE
DO NOT SCALE DRAWING

	NAME	DATE
DRAWN BY:	T.YANG	09.30.14
CHECKED BY:		
ENG APPR.		
MFG APPR.		
Q.A.		

COMMENTS:

THIRD ANGLE PROJECTION

Power Integrations

TITLE: FAB,HEATSINK, eSIP16/13,DER437

SIZE	DWG. NO.	REV
A	61-00181-01	01
SCALE: 1:1	WEIGHT:	SHEET 1 OF 1

Power Integrations
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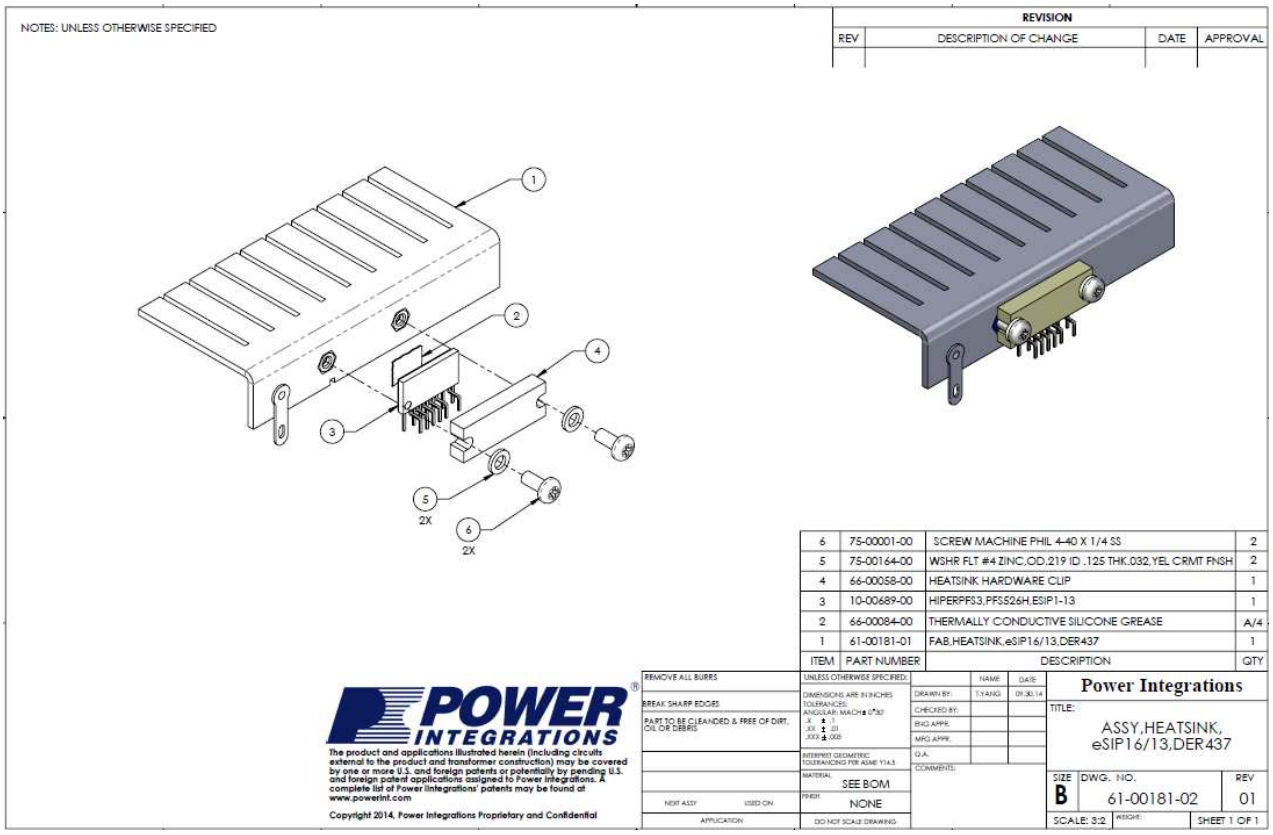
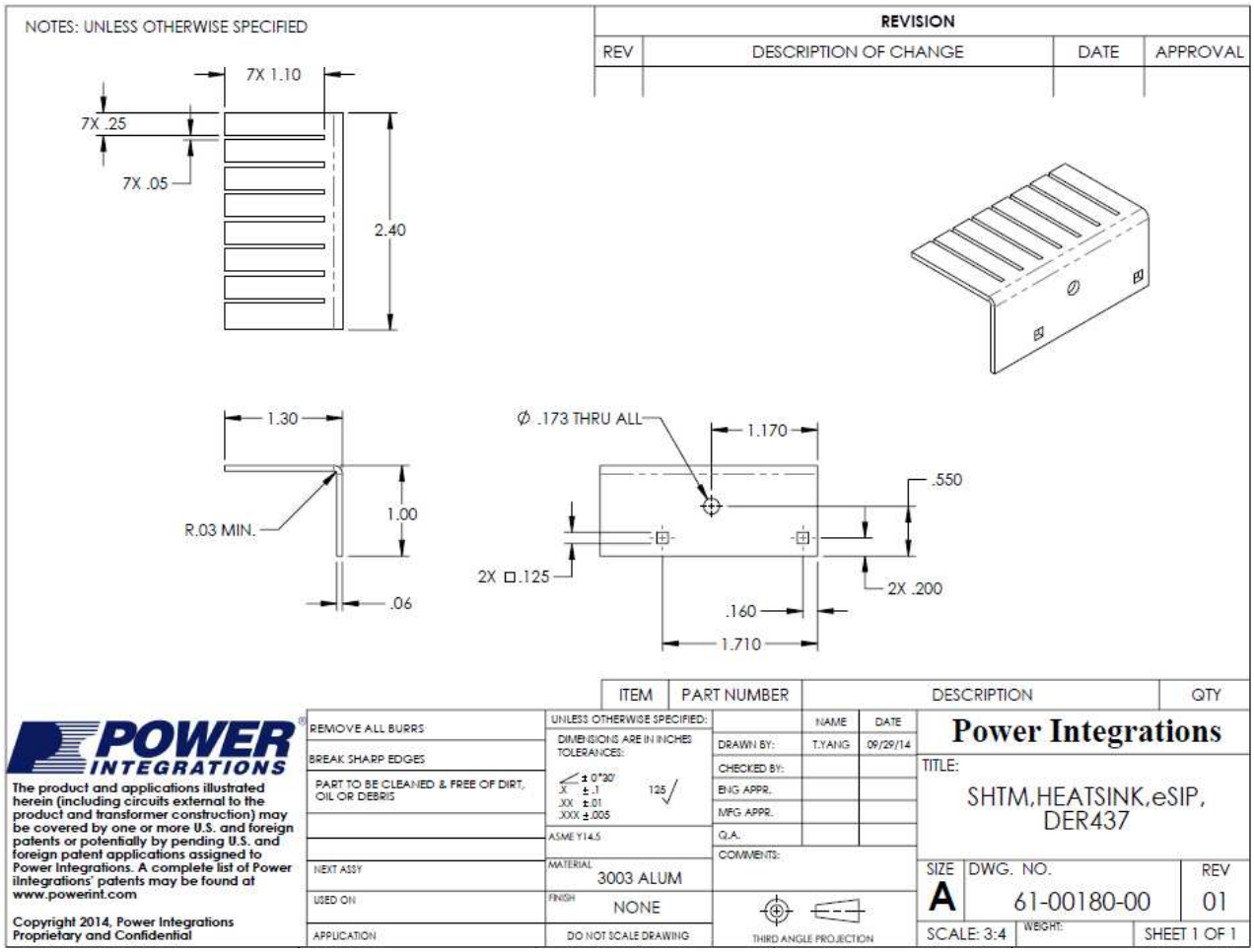
9.1.3 HiperPFS-3 and Heat Sink Assembly Drawing



9.2 LinkSwitch-HP Heat Sink

9.2.1 LinkSwitch-HP Heat Sink Fabrication Drawing



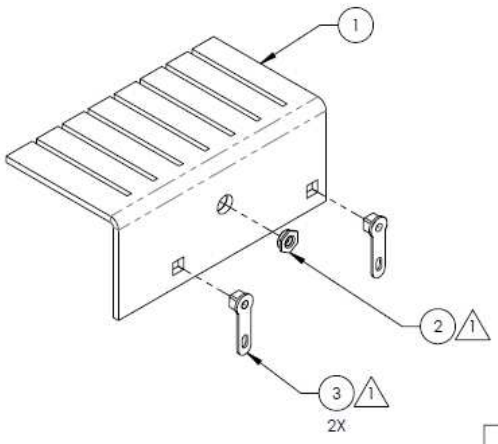
Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201

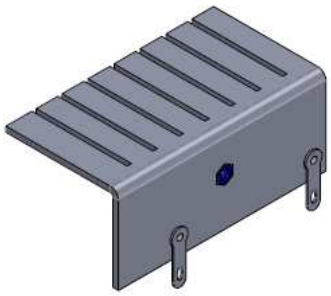
9.2.2 LinkSwitch-HP Heat Sink Assembly Drawing

NOTES: UNLESS OTHERWISE SPECIFIED

1. SUPPLIER TO INSTALL FLUSH NUT, ITEM 2 AND EYELET, ITEM 3 TO HEAT SINK, ITEM 1.

REVISION			
REV	DESCRIPTION OF CHANGE	DATE	APPROVAL





ITEM	PART NUMBER	DESCRIPTION	QTY
03	60-00016-00	TERM,EYELET,TIN PLD BRASS,ZIERICK PN 190	2
02	77-00005-00	CAPTIVE NUT,FLUSH,SS,4-40,PNL THK .061 "	1
01	61-00180-00	SHTM,HEATSINK,eSIP,DER427	1

POWER INTEGRATIONS

REMOVE ALL BURRS
BREAK SHARP EDGES
PART TO BE CLEANED & FREE OF DIRT, OIL OR DEBRIS
NEXT ASSY
USED ON
APPLICATION

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES:
∠ ± 0°30'
X ± .1
.XX ± .01
.XXX ± .005
125
ASME Y14.5
MATERIAL: SEE BOM
FINISH: NONE
DO NOT SCALE DRAWING

	NAME	DATE
DRAWN BY:	T.YANG	09.30.14
CHECKED BY:		
ENG APPR.		
MFG APPR.		
Q.A.		

COMMENTS:

THIRD ANGLE PROJECTION

Power Integrations

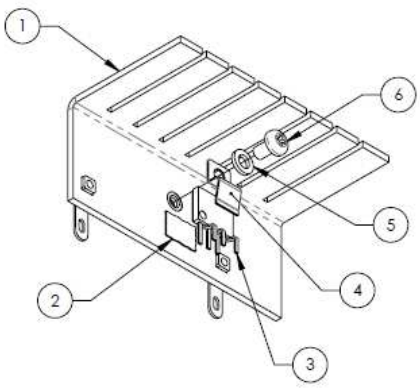
TITLE: FAB,HEATSINK, eSIP,DER437

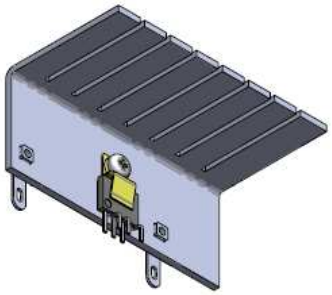
SIZE	DWG. NO.	REV
A	61-00180-01	01
SCALE: 1:1	WEIGHT:	SHEET 1 OF 1

9.2.3 LinkSwitch-HP and Heat Sink Assembly Drawing

NOTES: UNLESS OTHERWISE SPECIFIED

REVISION			
REV	DESCRIPTION OF CHANGE	DATE	APPROVAL





ITEM	PART NUMBER	DESCRIPTION	QTY
6	75-00089-00	SCREW MACHINE PHIL 4-40 X 3/16 SS	1
5	75-00164-00	WSHR,FLT #4 ZNC,OD.219,ID.125,THK.032	1
4	60-00037-00	EDGE-CLIP-14.33mmL x 6.35mmW	1
3	10-00826-00	LINKSWITCH-HP,LNK6779E,eSIP-7C	1
2	66-00084-00	THERMAL CONDUCTIVE SILICONE GREASE	A/R
1	61-00180-01	FAB,HEATSINK,eSIP,DER437	1

POWER INTEGRATIONS

REMOVE ALL BURRS
BREAK SHARP EDGES
PART TO BE CLEANED & FREE OF DIRT, OIL OR DEBRIS
NEXT ASSY
USED ON
APPLICATION

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES:
± 0°30'
X ± .1
.XX ± .01
.XXX ± .005
125
ASME Y14.5
MATERIAL: SEE BOM
FINISH: NONE
DO NOT SCALE DRAWING

	NAME	DATE
DRAWN BY:	T.YANG	09.30.14
CHECKED BY:		
ENG APPR.		
MFG APPR.		
Q.A.		

COMMENTS:

THIRD ANGLE PROJECTION

Power Integrations

TITLE: ASSY,HEATSINK,eSIP, DER437

SIZE	DWG. NO.	REV
A	61-00180-02	01
SCALE: 1:1	WEIGHT:	SHEET 1 OF 1

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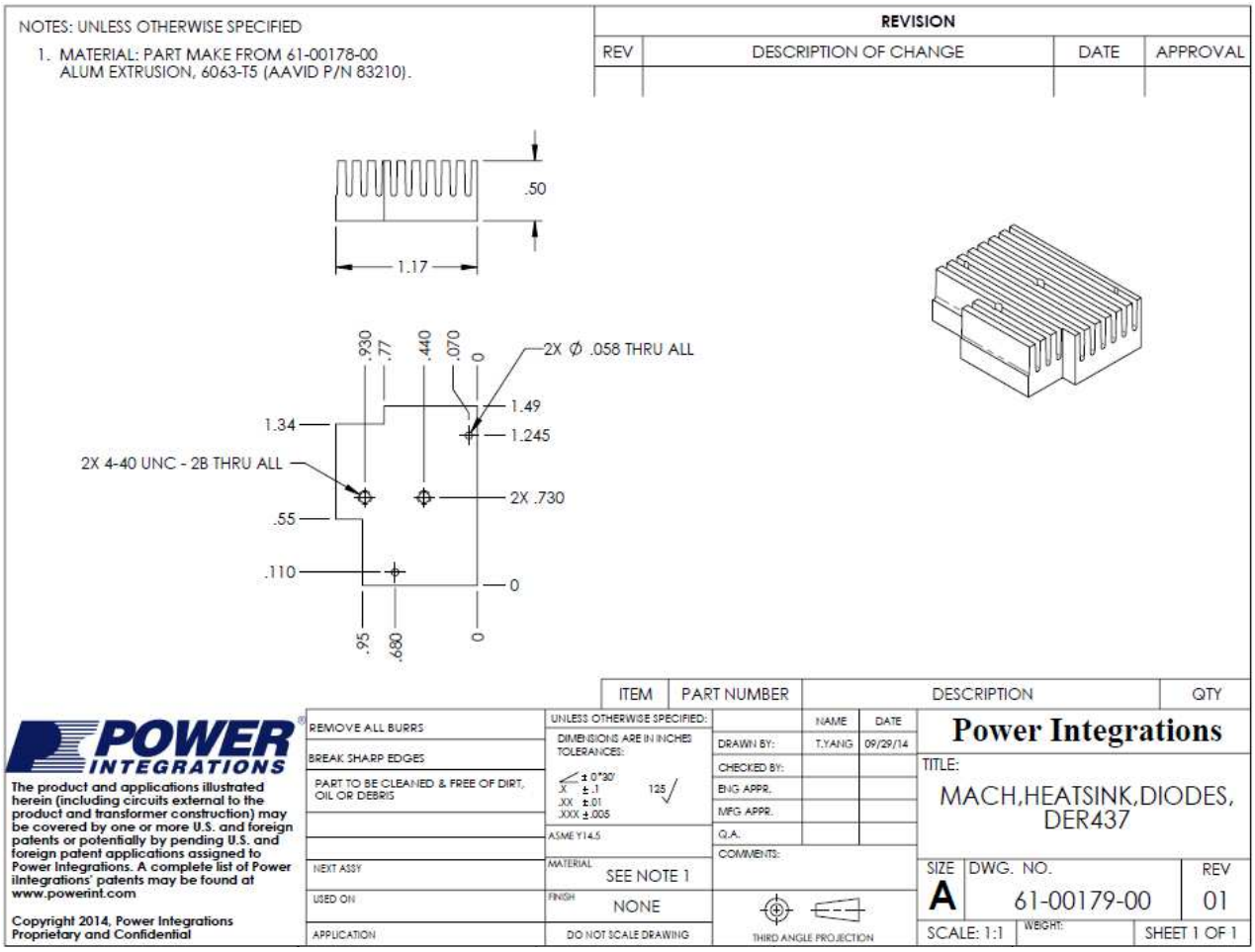
9.3 Diode Heat Sink

9.3.1 Diode Heat Sink Fabrication Drawing

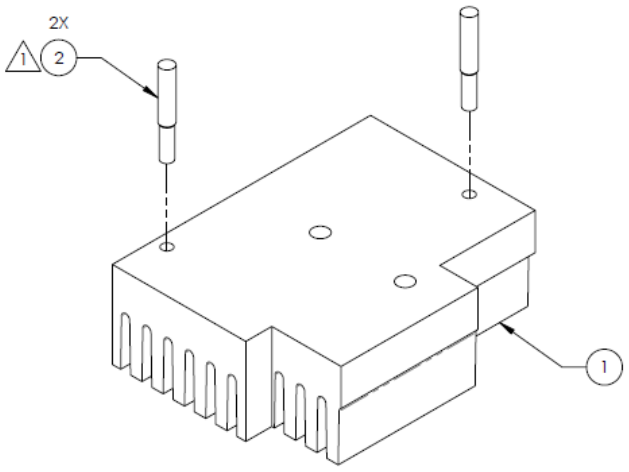


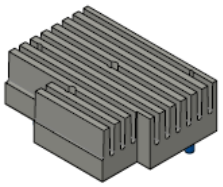
9.3.2 Heat Sink Assembly Drawing

NOTES: UNLESS OTHERWISE SPECIFIED

1. PIN, ITEM 2, TO BE PRESSED FIT INTO HEAT SINK, ITEM 1 BY SUPPLIER.

REVISION			
REV	DESCRIPTION OF CHANGE	DATE	APPROVAL





ITEM	PART NUMBER	DESCRIPTION	QTY
02	60-00052-00	PIN,NKL PLT STL,12mmLX1.9mm TO 1.6mm STP	2
01	61-00179-00	MACH,HEATSINK,DIODES,DER437	1

POWER INTEGRATIONS

REMOVE ALL BURRS

BREAK SHARP EDGES

PART TO BE CLEANED & FREE OF DIRT, OIL OR DEBRIS

NEXT ASSY

USED ON

APPLICATION

UNLESS OTHERWISE SPECIFIED:

DIMENSIONS ARE IN INCHES

TOLERANCES:

∠ ± 0°30'
X ± .1
XX ± .01
XXX ± .005

125

ASME Y14.5

MATERIAL: SEE BOM

FINISH: NONE

DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

	NAME	DATE
DRAWN BY:	T.YANG	09.30.14
CHECKED BY:		
ENG APPR.		
MFG APPR.		
Q.A.		

COMMENTS:

Power Integrations

TITLE: FAB,HEATSINK, DIODES,DER437

SIZE	DWG. NO.	REV
A	61-00179-01	01

SCALE: 2:1 WEIGHT: SHEET 1 OF 1

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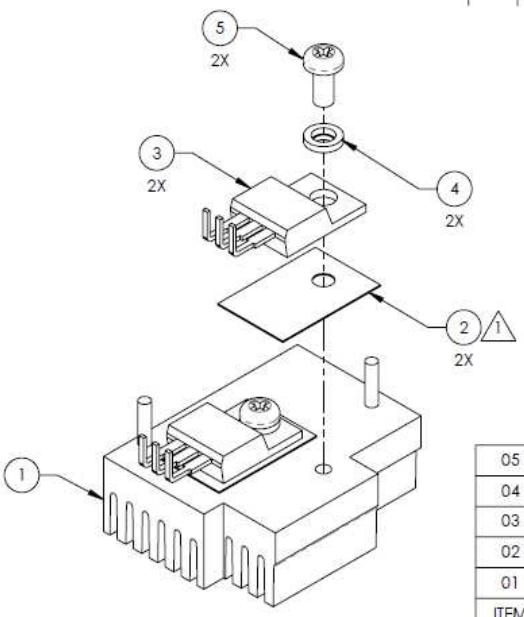
Tel: +1 408 414 9200 Fax: +1 408 414 9201

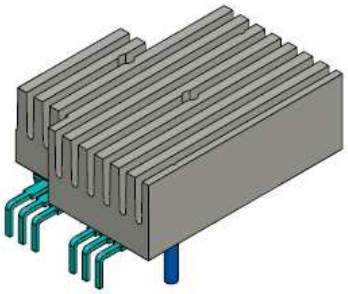
9.3.3 Diode and Heat Sink Assembly Drawing

NOTES: UNLESS OTHEWISE SPECIFIED

1. TRIM OVERLAP/EXCESS THERMAL PAD, ITEM 2, AS REQUIRED WHEN ASSEMBLE.

REVISION			
REV	DESCRIPTION OF CHANGE	DATE	APPROVAL





ITEM	PART NUMBER	DESCRIPTION	QTY
05	75-00001-00	SCREW MACHINE PHIL 4-40 X 1/4 SS	2
04	75-00071-00	WASHER NYLON SHOULDER #4	2
03	15-01079-00	200V,10A,DUAL SCHOTTKY,TO-220AB	2
02	66-00079-00	THERMAL PAD TO-220 9MIL SP1000	2
01	61-00179-01	FAB,HEATSINK,DIODES,DER437	1

POWER INTEGRATIONS

REMOVE ALL BURRS
BREAK SHARP EDGES
PART TO BE CLEANED & FREE OF DIRT, OIL OR DEBRIS
NEXT ASSY
USED ON
APPLICATION

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES:
± 0°30'
X ±.1
XX ±.01
XXX ±.005
125
ASME Y14.5
MATERIAL: SEE BOM
FINISH: NONE
DO NOT SCALE DRAWING

	NAME	DATE
DRAWN BY:	T.YANG	09.30.14
CHECKED BY:		
ENG APPR.		
MFG APPR.		
Q.A.		

COMMENTS:

THIRD ANGLE PROJECTION

Power Integrations

TITLE: ASSY,HEATSINK, DIODES,DER437

SIZE	DWG. NO.	REV
A	61-00179-02	01
SCALE: 2:1	WEIGHT:	SHEET 1 OF 1

10 Performance Data

All measurements were taken at room temperature and 50/60 Hz input frequency unless otherwise specified, Output voltage measurements were taken at the output connectors.

10.1 System Efficiency

Figures below show the total supply efficiency (PFC and LinkSwitch-HP stages). AC input was supplied using a sine wave source.

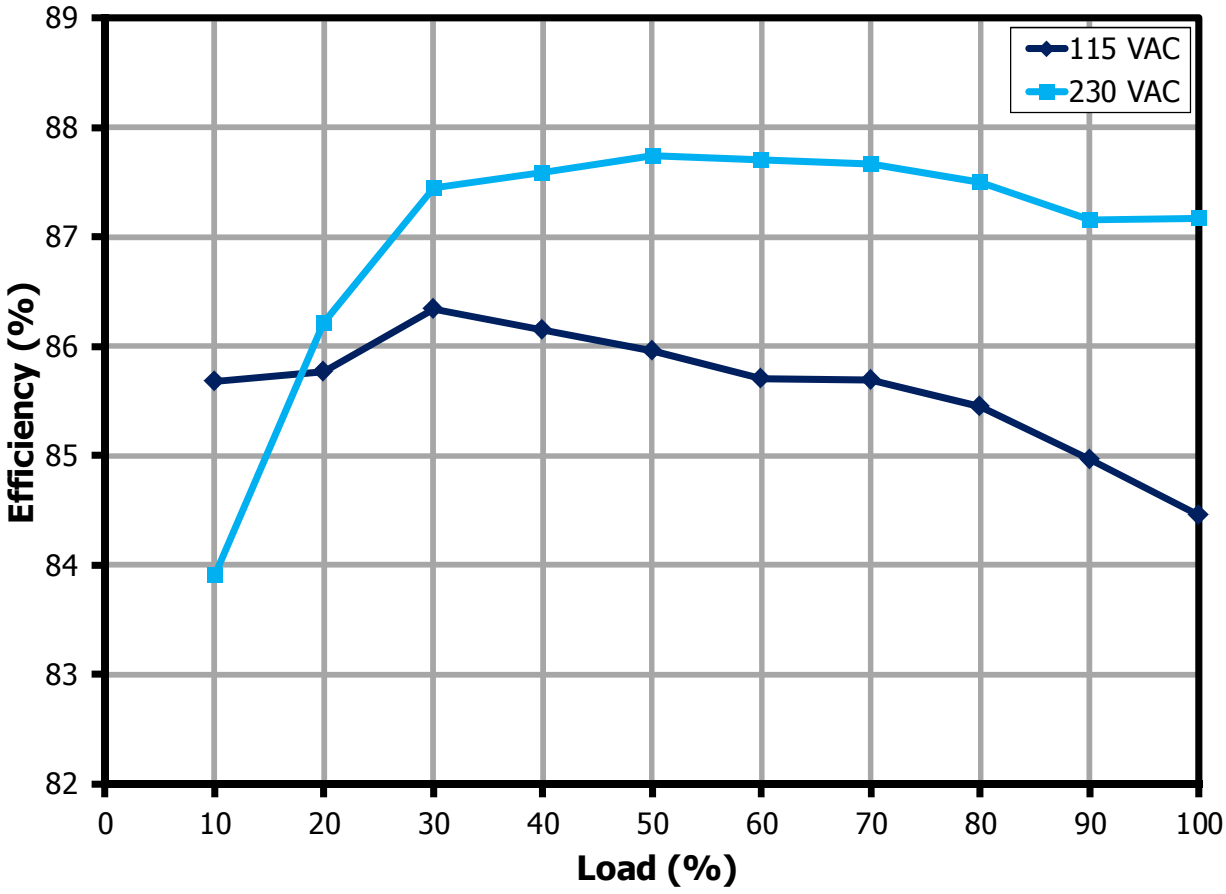


Figure 10 – System Efficiency vs. Load.

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10.2 Power Factor

Power factor measurements were made using a sine wave AC source.

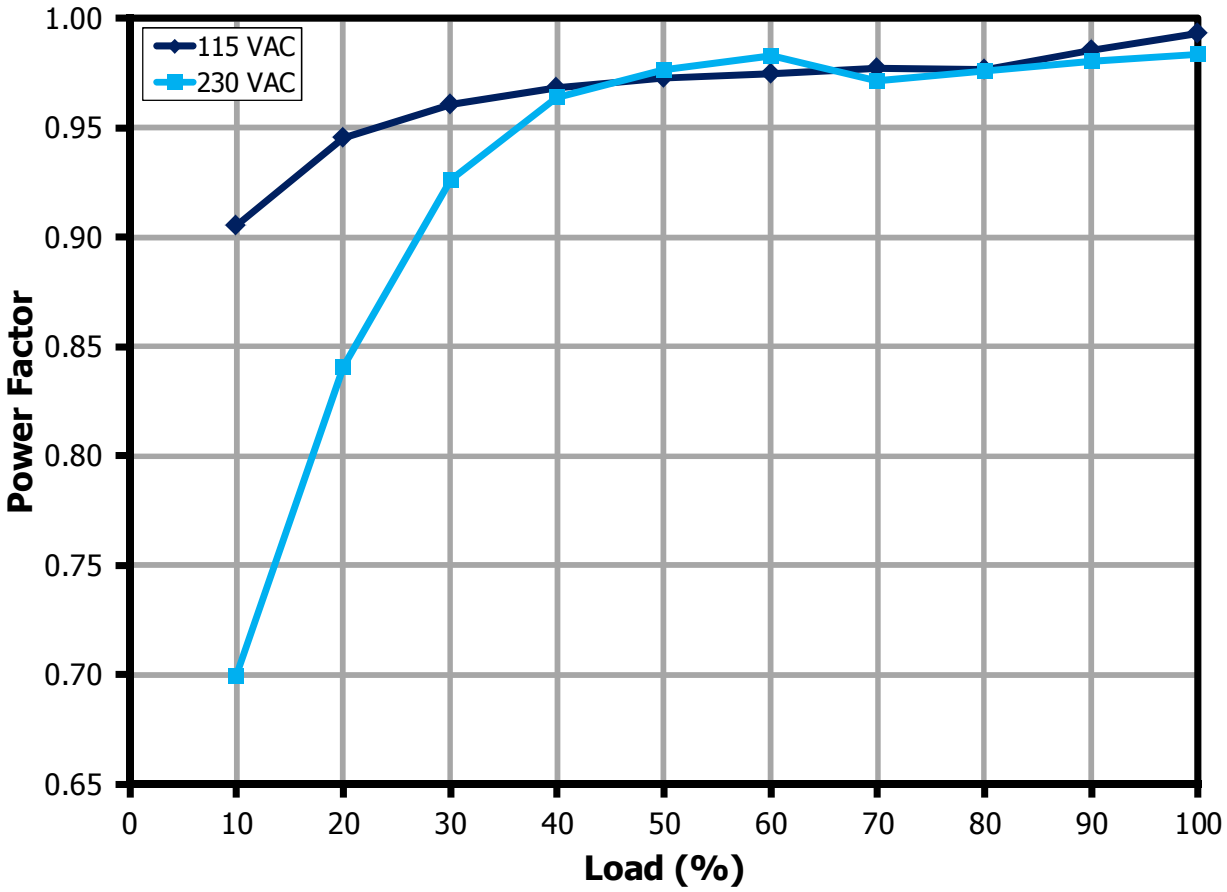

Figure 11 – Power Factor vs. Load.

10.3 THD

THD measurements were made using a sine wave AC source.

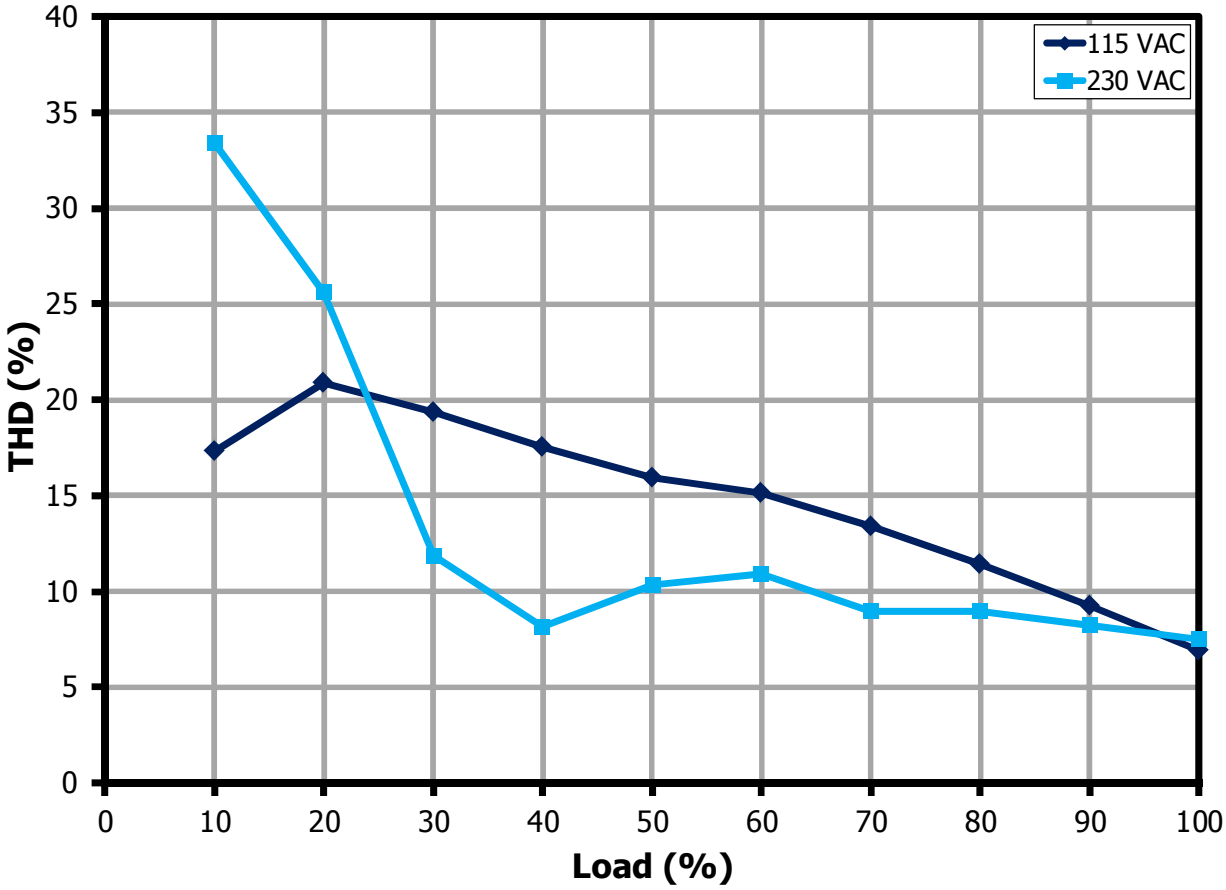

Figure 12 – THD vs. Load.

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10.4 Load Regulation

Load regulation measurements were made by sweeping the load from 10% to full load.

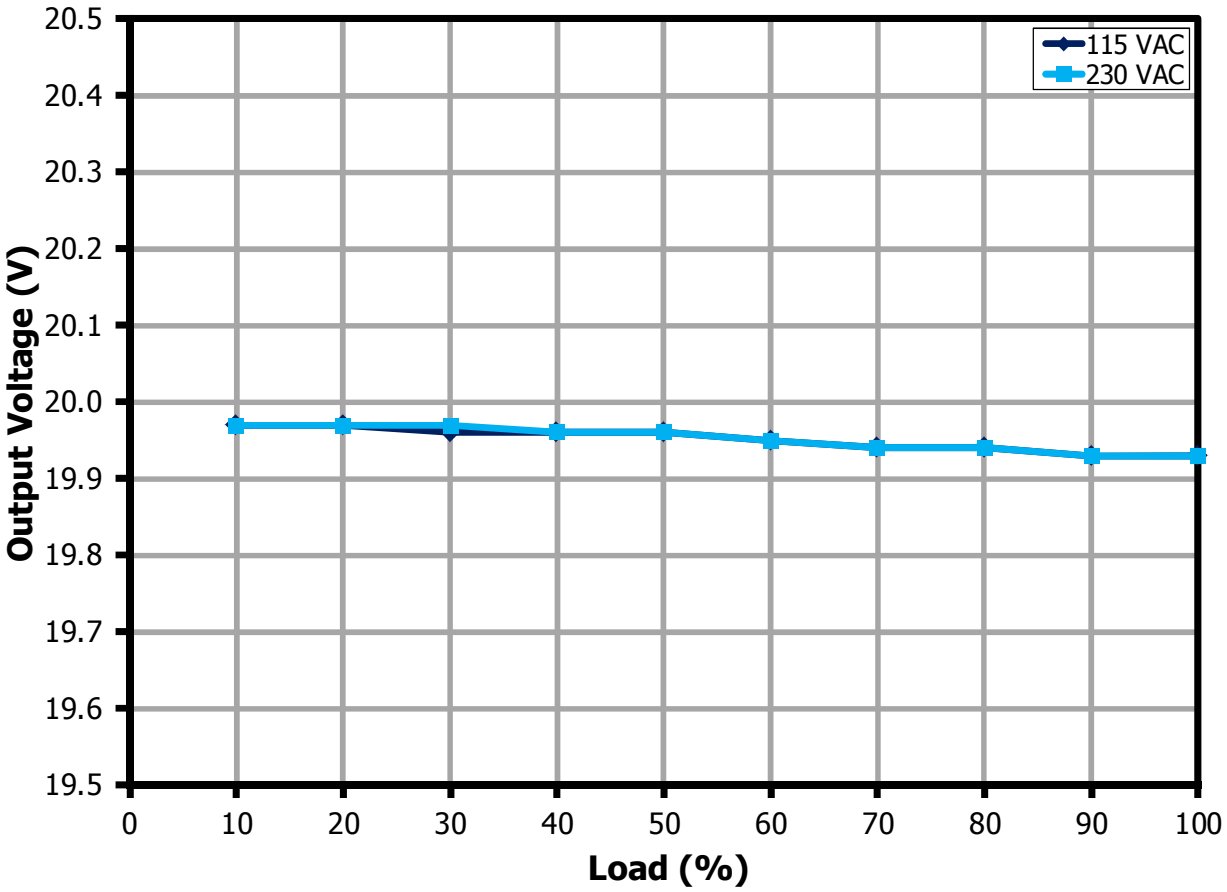

Figure 13 – Output Voltage vs. Load.

10.5 Light Load Consumption

Light Load consumption data is measured by loading 20V ouput.

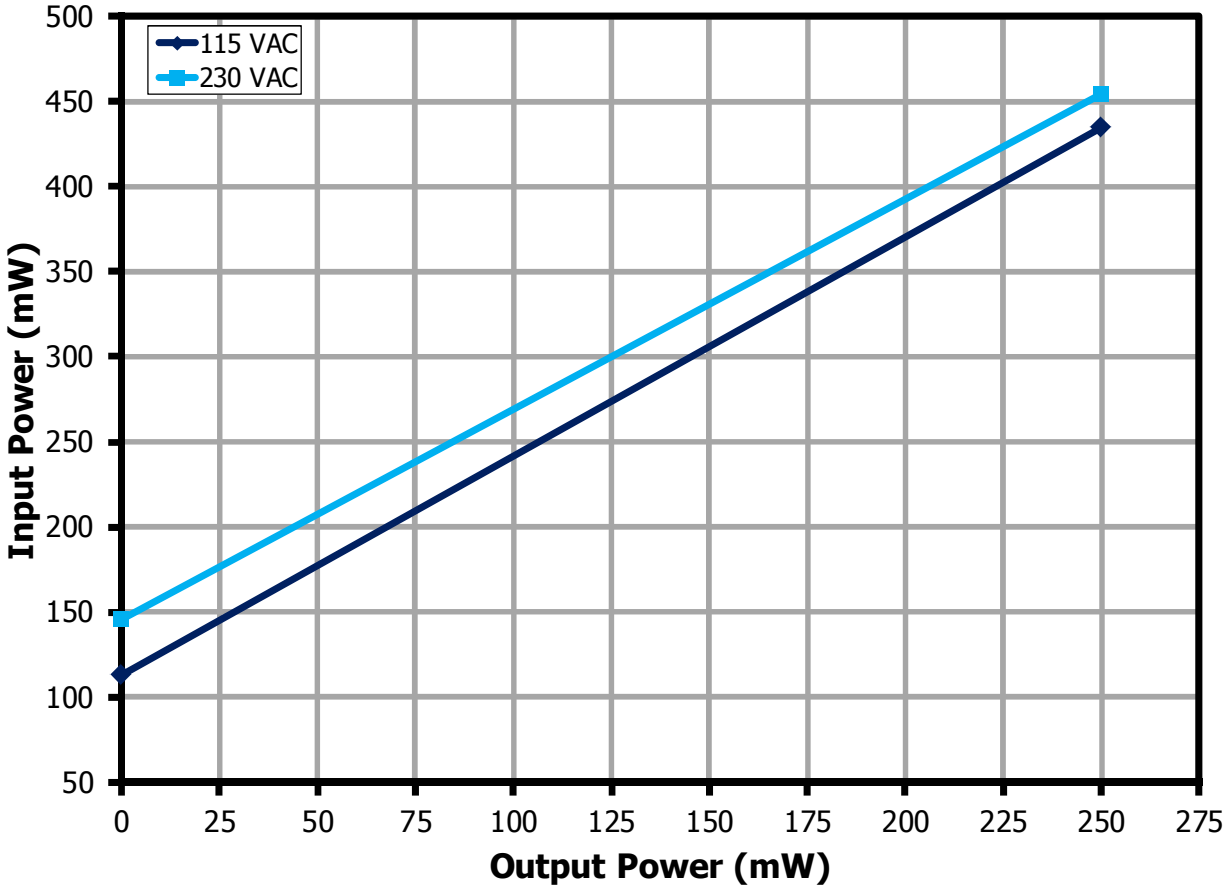

Figure 14 – Input power vs. Load.

Note: By using optocoupler feedback, No-load or light load requirement is reduced greately by eliminating pre-load requirement.

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10.6 Thermal Set-up and Performance

Thermal test was carried out at 25 ºC, 90 VAC and full load. Forced air cooling is required to operate the power supply at full load.

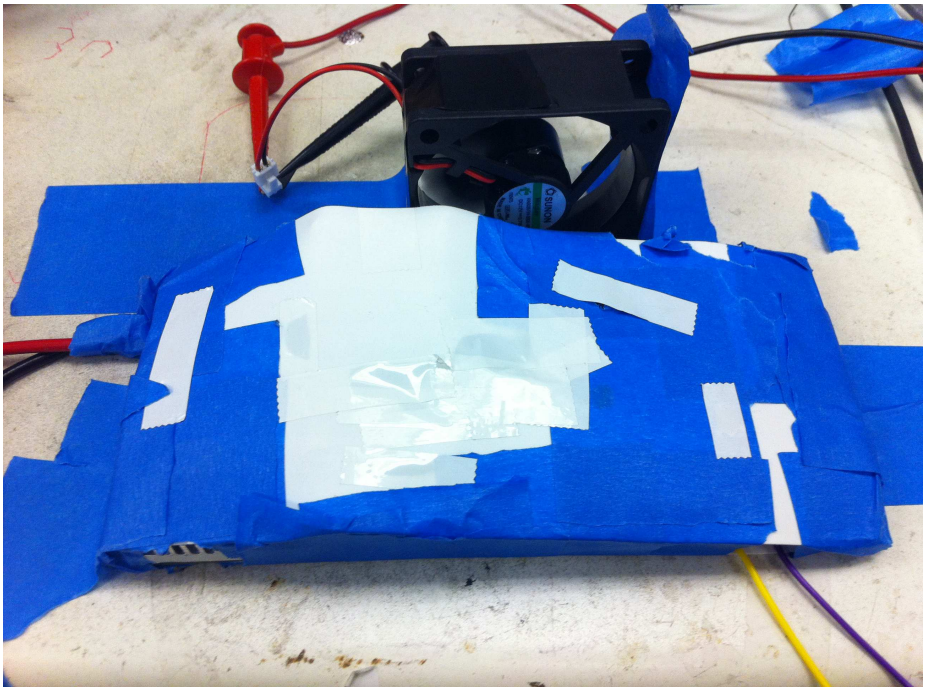

Figure 15 – Thermal Set-up.

Device	ºC
Tamb	23
PFC Inductor	53.8
Common Mode Choke (L4)	80.3
PFC MOSFET	61
Bridge Rectifier	62.1
LinkSwitch-HP Heat Sink	73.5
LinkSwitch-HP MOSFET	68.3
Primary Clamp Diode	78.8
Primary Clamp Zener	68.9
Primary Clamp Resistor	65.5
Transformer Winding	84.5
Secondary Freewheel Diode	75
Secondary Freewheel Diode Heat Sink	68.3
Secondary Snubber Resistor	81.2

Note: SUNON Fan (HA60251V4-0000-999) was used to cool the power supply. This Fan is rated for 12 V, 0.7 W and 13.8 CFM airflow.

11 Waveforms

11.1 Input Voltage and Current

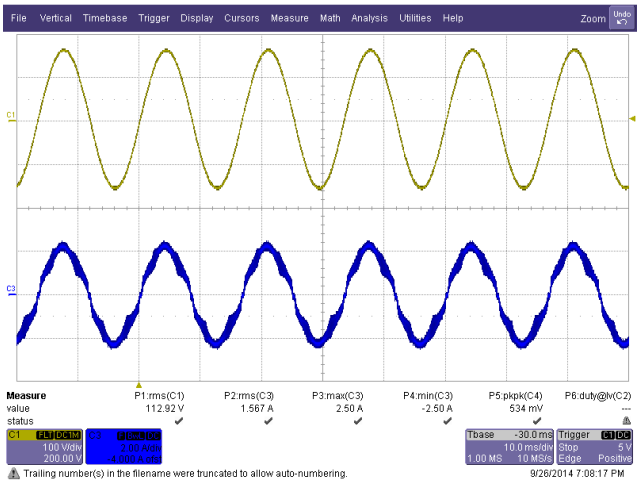

Figure 16 – 115 VAC, 150 W Load.
Upper: V_{IN}, 100 V, 10 ms / div.
Lower: I_{IN}, 2 A / div.

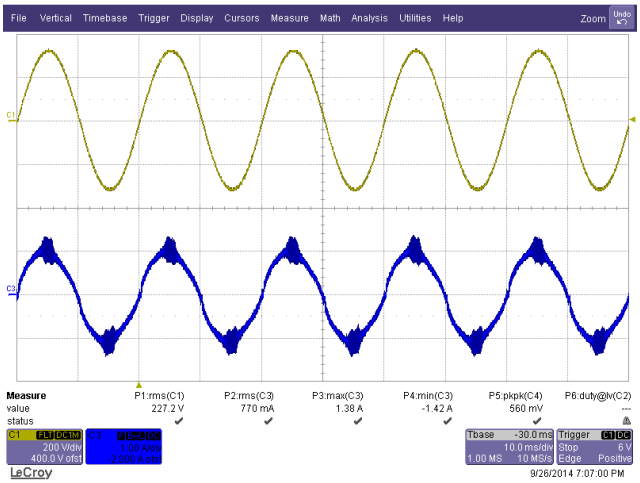

Figure 17 – 230 VAC, 150 W Load.
Upper: V_{IN}, 200 V, 10 ms / div.
Lower: I_{IN}, 1 A / div.

11.2 LinkSwitch-HP Primary Drain Voltage and Current

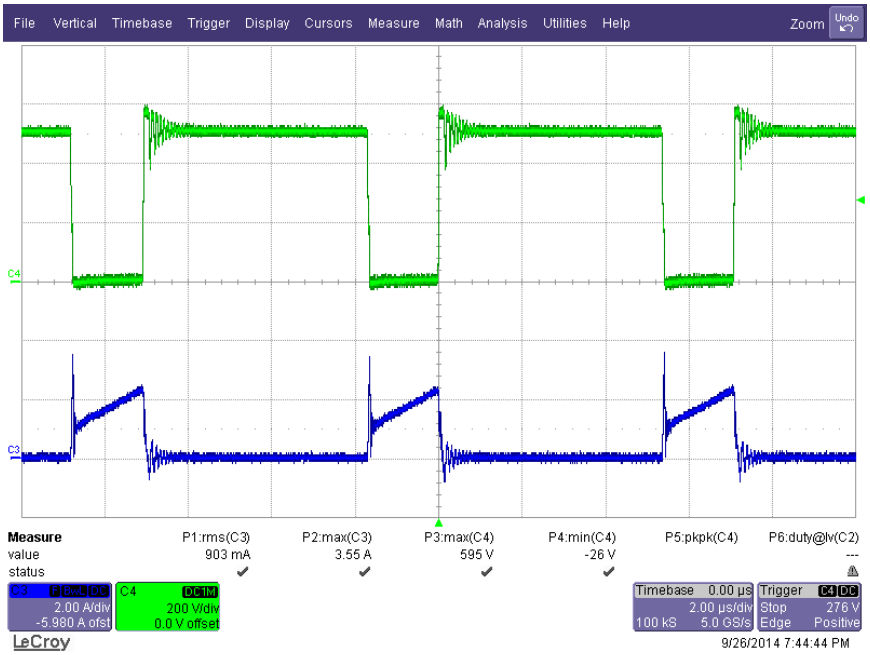

Figure 18 – LinkSwitch-HP Primary Drain Voltage and Current.
Upper: Voltage, 200 V, 2 µs / div.
Lower: Current, 2 A / div.

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11.3 PFC Switch Voltage and Current - Normal Operation

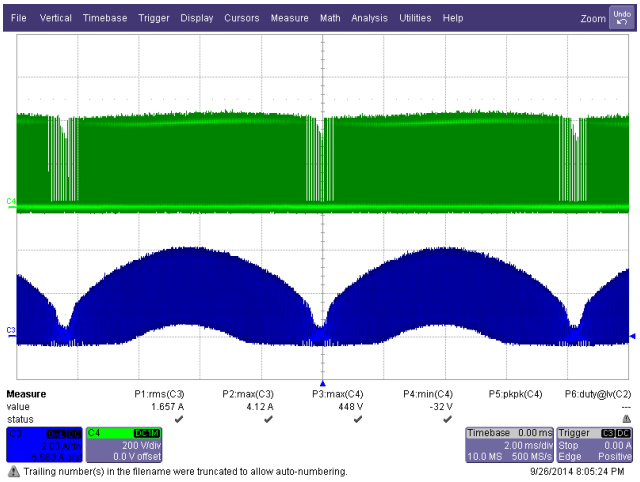

Figure 19 – PFC Stage Drain Voltage and Inductor Current, Full Load, 115 VAC.
Upper: V_{DRAIN}, 200 V, 2 ms / div.
Lower: $I_{INDUCTOR}$, 2 A / div.

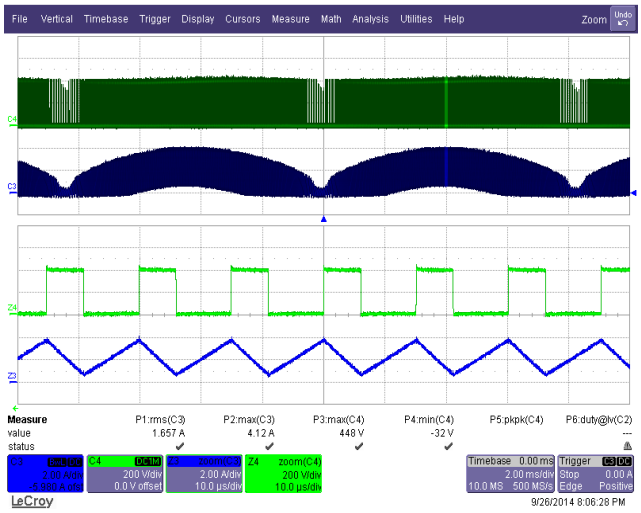

Figure 20 – PFC Stage Drain Voltage and Inductor Current, Full Load, 115 VAC.
Upper: V_{DRAIN}, 200 V, 10 µs / div. (Zoom in on Top of Sine Wave)
Lower: $I_{INDUCTOR}$, 2 A / div.

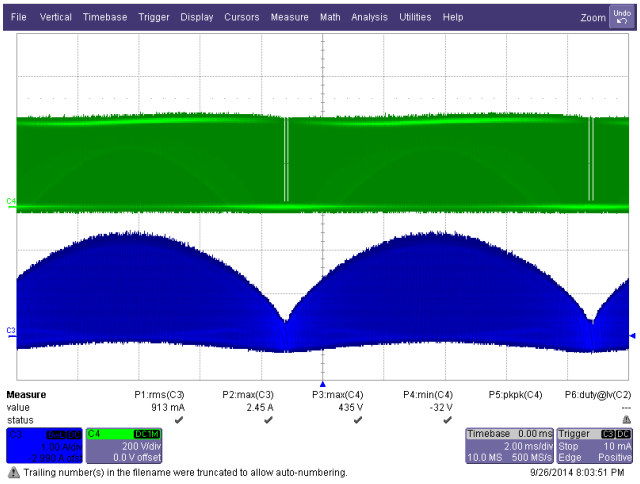

Figure 21 – PFC Stage Drain Voltage and Inductor Current, Full Load, 230 VAC.
Upper: V_{DRAIN}, 200 V, 2 ms / div.
Lower: $I_{INDUCTOR}$, 1 A / div.

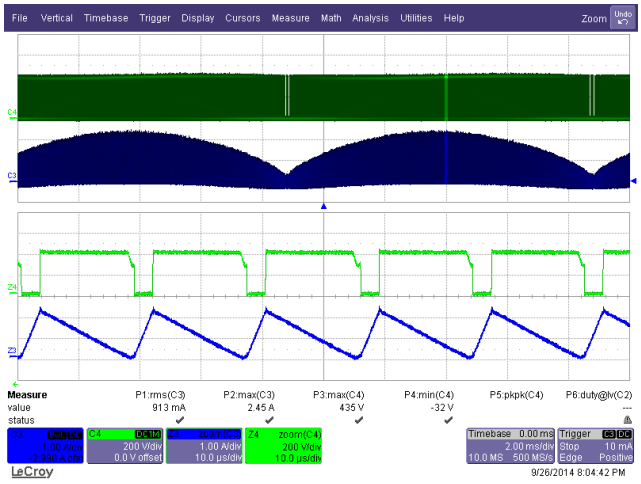

Figure 22 – PFC Stage Drain Voltage and Inductor Current, Full Load, 230 VAC.
Upper: $I_{INDUCTOR}$, 1 A / div.
Lower: V_{DRAIN}, 200 V, 10 µs / div.
(Zoom in on Top of Sine Wave)

11.4 AC Input Current and PFC Output Voltage during Start-up

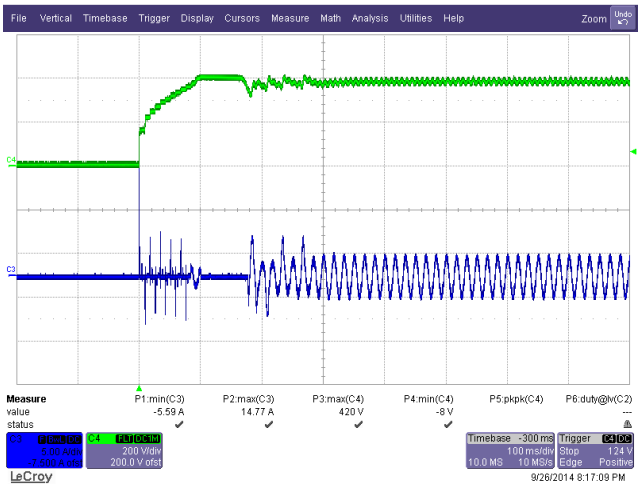

Figure 23 – AC Input Current vs. PFC Output Voltage at Start-up, Full Load, 115 VAC.
Upper: PFC V_{OUT}, 200 V, 100 ms / div.
Lower: AC I_{IN}, 5 A / div.

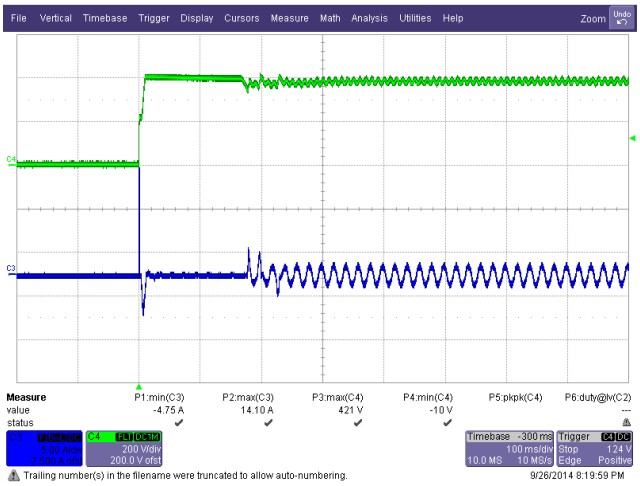

Figure 24 – AC Input Current vs. PFC Output Voltage at Start-up, Full Load, 230 VAC.
Upper: AC I_{IN}, 5 A / div.
Lower: PFC V_{OUT}, 200 V, 100 ms / div.

11.5 LinkSwitch-HP Drain Voltage and Current during Start-up

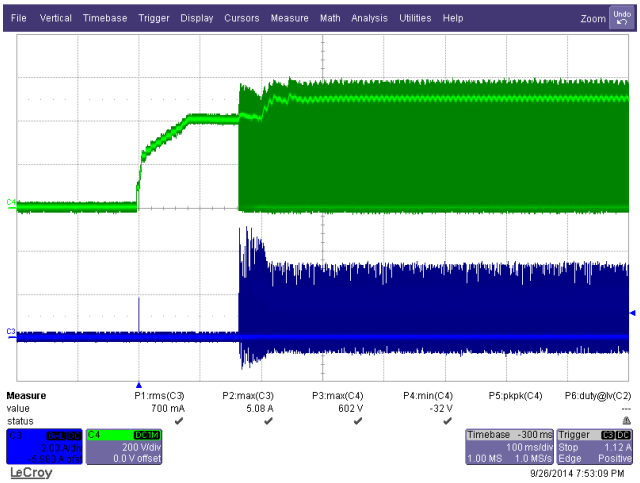

Figure 25 – LinkSwitch-HP Start-up. 115 VAC, Full Load.
Upper: V_{DRAIN}, 200 V.
Lower: I_{DRAIN}, 2 A / div., 50 ms / div.

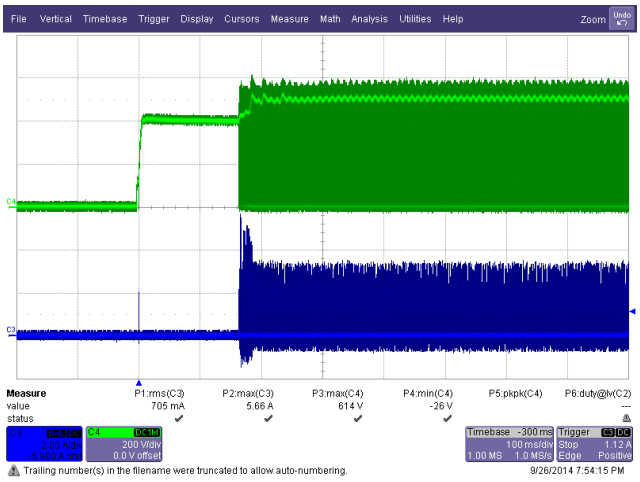

Figure 26 – LinkSwitch-HP Start-up. 230 VAC, Full Load.
Upper: V_{DRAIN}, 200 V.
Lower: I_{DRAIN}, 1 A / div., 50 ms / div.

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11.6 Output Voltage Start-up

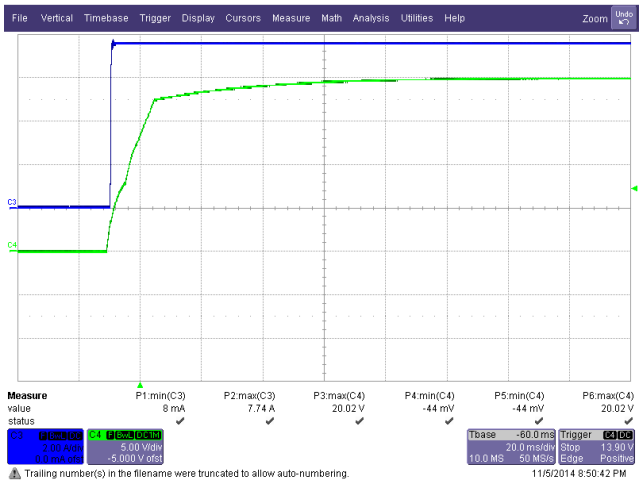

Figure 27 – Output Start-up. 230 VAC, Full Load.
Upper: 7.5 A I_{OUT}, 2 A / div.
Lower: 20 V V_{OUT}, 5 V, 50 ms / div.

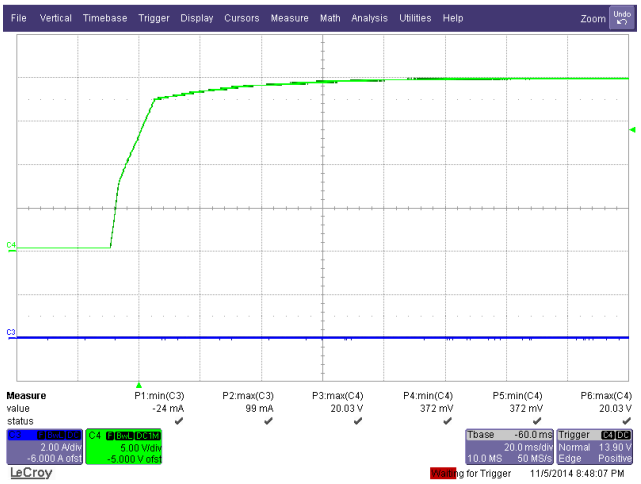

Figure 28 – Output Start-up. 230 VAC, No-load.
Upper: 20 V V_{OUT}, 5 V
Lower: 0 A I_{OUT}, 2 A / div., 50 ms / div.

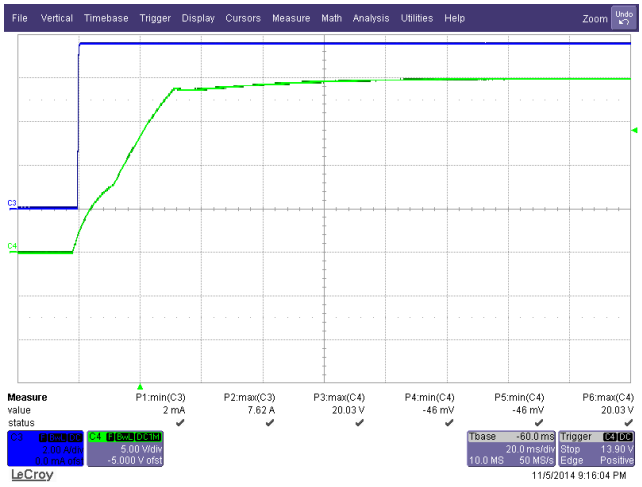

Figure 29 – Output Start-up with 5000 µF. 230 VAC, Full Load.
Upper: 7.5 A I_{OUT}, 2 A / div.
Lower: 20 V V_{OUT}, 5 V, 50 ms / div.

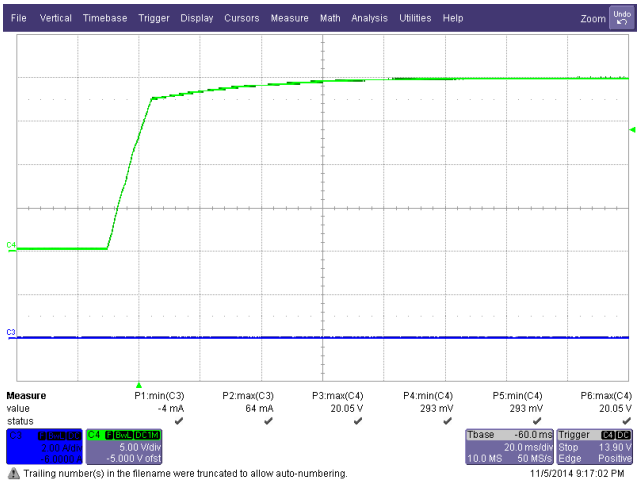

Figure 30 – Output Start-up with 5000 µF. 230 VAC, No-load.
Upper: 20 V V_{OUT}, 5 V
Lower: 0 A I_{OUT}, 2 A / div., 50 ms / div.

11.7 Output Rectifier Diode Voltage Waveforms

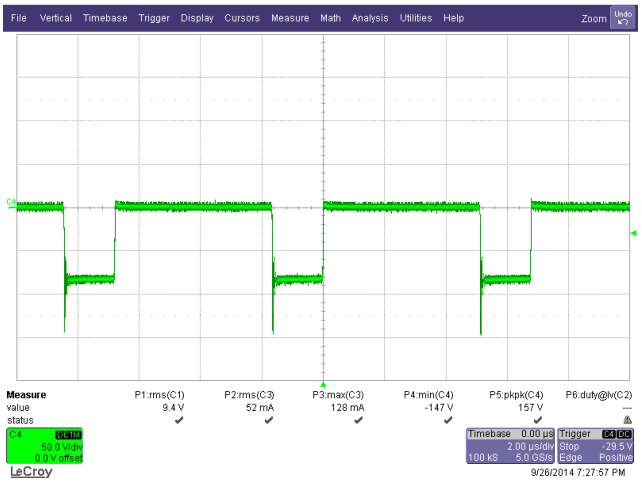

Figure 31 – 20 V Output Rectifier Diode Voltage, 100% Load.
Upper: 20 V Output Diode PIV, 50 V / div.
2 µs / div.

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12 Output Ripple Measurements

12.1 Ripple Measurement Technique

For DC output ripple measurements, use a modified oscilloscope test probe to reduce spurious signals. Details of the probe modification are provided in figures below.

Tie two capacitors in parallel across the probe tip of the 4987BA probe adapter. Use a 0.1 µF / 50 V ceramic capacitor and 1.0 µF / 100 V aluminum electrolytic capacitor. The aluminum-electrolytic capacitor is polarized, so always maintain proper polarity across DC outputs.

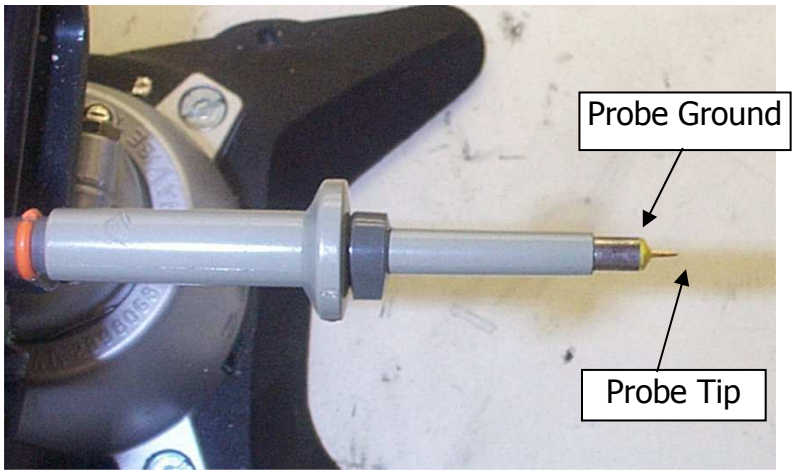

Figure 32 – Oscilloscope Probe Prepared for Ripple Measurement (End Cap and Ground Lead Removed).

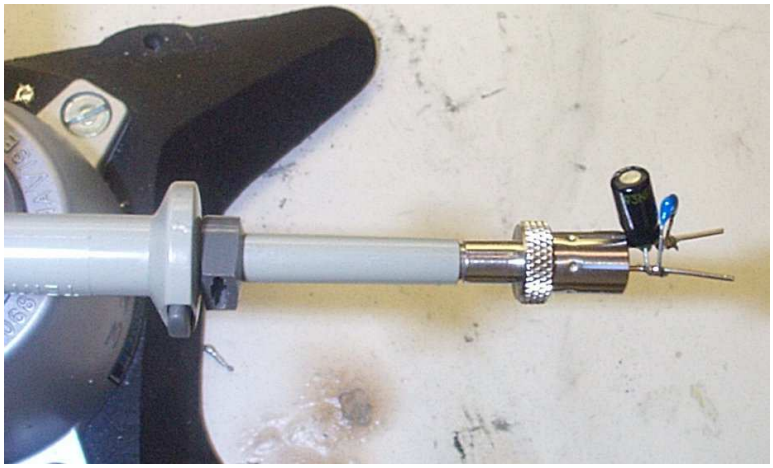

Figure 33 – Oscilloscope Probe with Probe Master 4987BA BNC Adapter (Modified with Wires for Probe Ground for Ripple measurement and Two Parallel Decoupling Capacitors Added).

12.1.1 Full Load Output Ripple Results

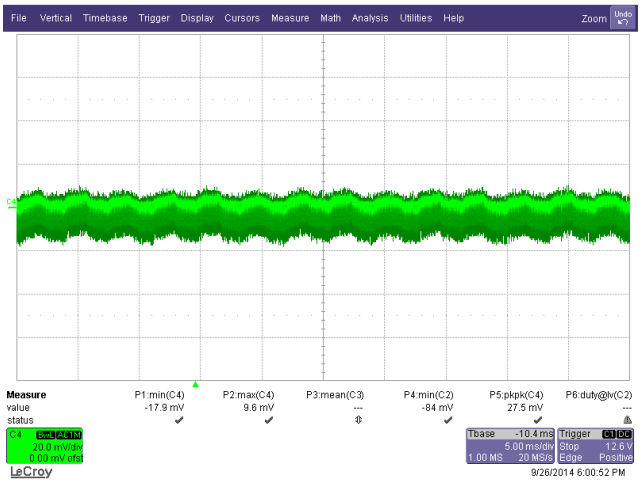

Figure 34 – Output Ripple, 100% Load.
Upper: 20 V V_{RIPPLE}, 20 mV / div.,
5 ms / div.

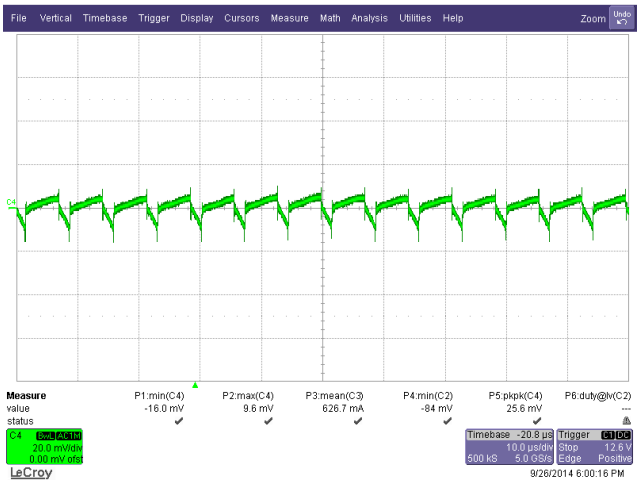

Figure 35 – Output Ripple, 100% Load.
Upper: 20 V V_{RIPPLE}, 20 mV / div.,
10 µs / div.

12.1.1 Full Load Output Ripple Results

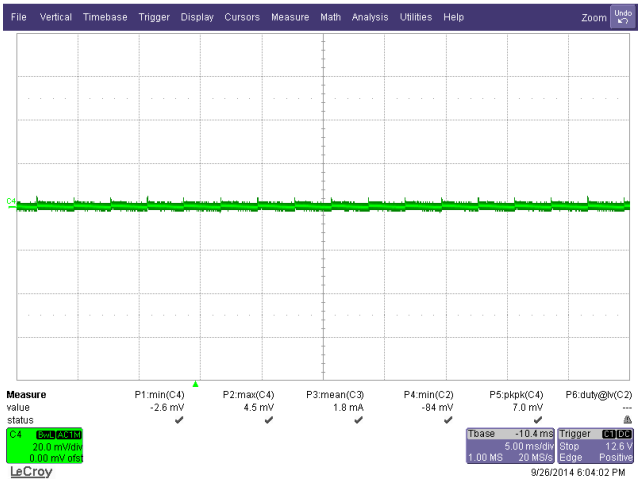

Figure 36 – Output Ripple, 0% Load.
Upper: 20 V V_{RIPPLE}, 20 mV / div.,
5 ms / div.

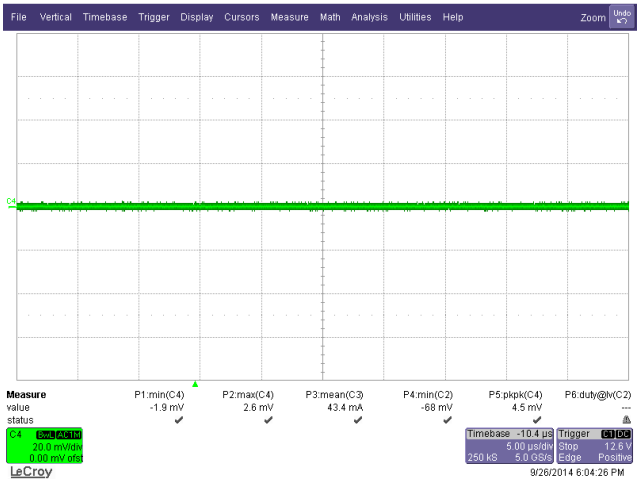

Figure 37 – Output Ripple, 0% Load.
Upper: 20 V V_{RIPPLE}, 20 mV / div.,
10 µs / div.

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12.2 Output Load Step Response

The figures below show transient response with a 0%-60%-0%, 0%-60%, 40%-100%-40%, and 50%-9A-50% load steps for the 20 V output. The oscilloscope was triggered using the rising edge of the load step, and averaging was used to cancel out ripple components asynchronous to the load step in order to better ascertain the load step response.

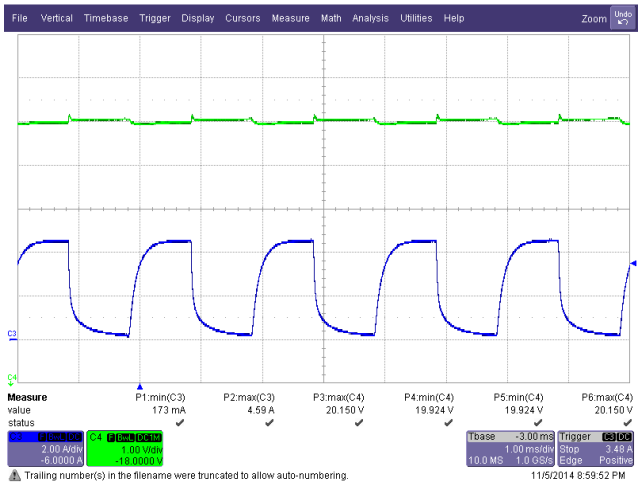

Figure 38 – Output Transient Response 0%-60%-0% Load Step on 20 V.
Upper: 20 V V_{OUT}, 1 V / div.
Lower: I_{LOAD}, 2 A / div., 1 ms / div.

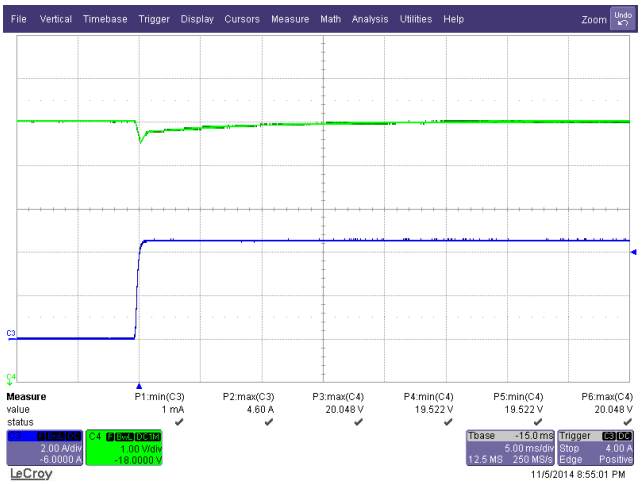

Figure 39 – Output Transient Response 0%-60% Load Step on 20 V.
Upper: 20 V V_{OUT}, 1 V / div.
Lower: I_{LOAD}, 2 A / div., 10 ms / div.

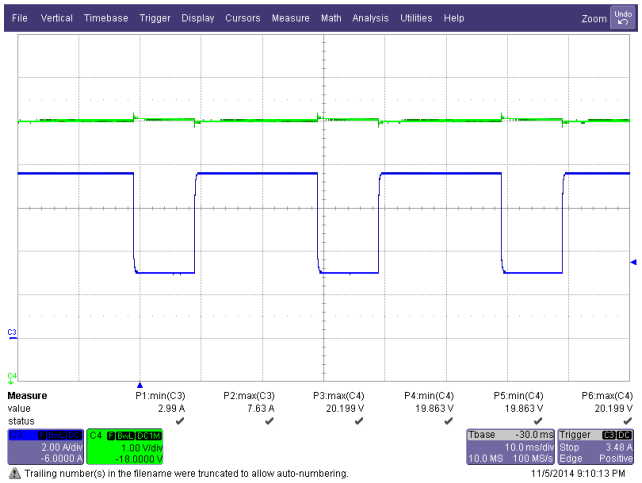

Figure 40 – Output Transient Response 40%-100%-40% Load Step on 20 V.
Upper: 20 V V_{OUT}, 1 V / div.
Lower: I_{LOAD}, 2 A / div., 10 ms / div.

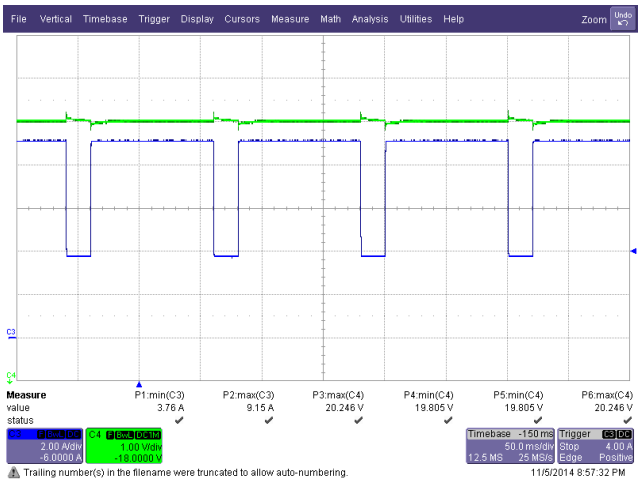

Figure 41 – Output Transient Response 50%-9A-50% Load Step on 20 V.
Upper: 20 V V_{OUT}, 1 V / div.
Lower: I_{LOAD}, 2 A / div., 50 ms / div.

13 Conducted EMI

13.1 EMI Set-up

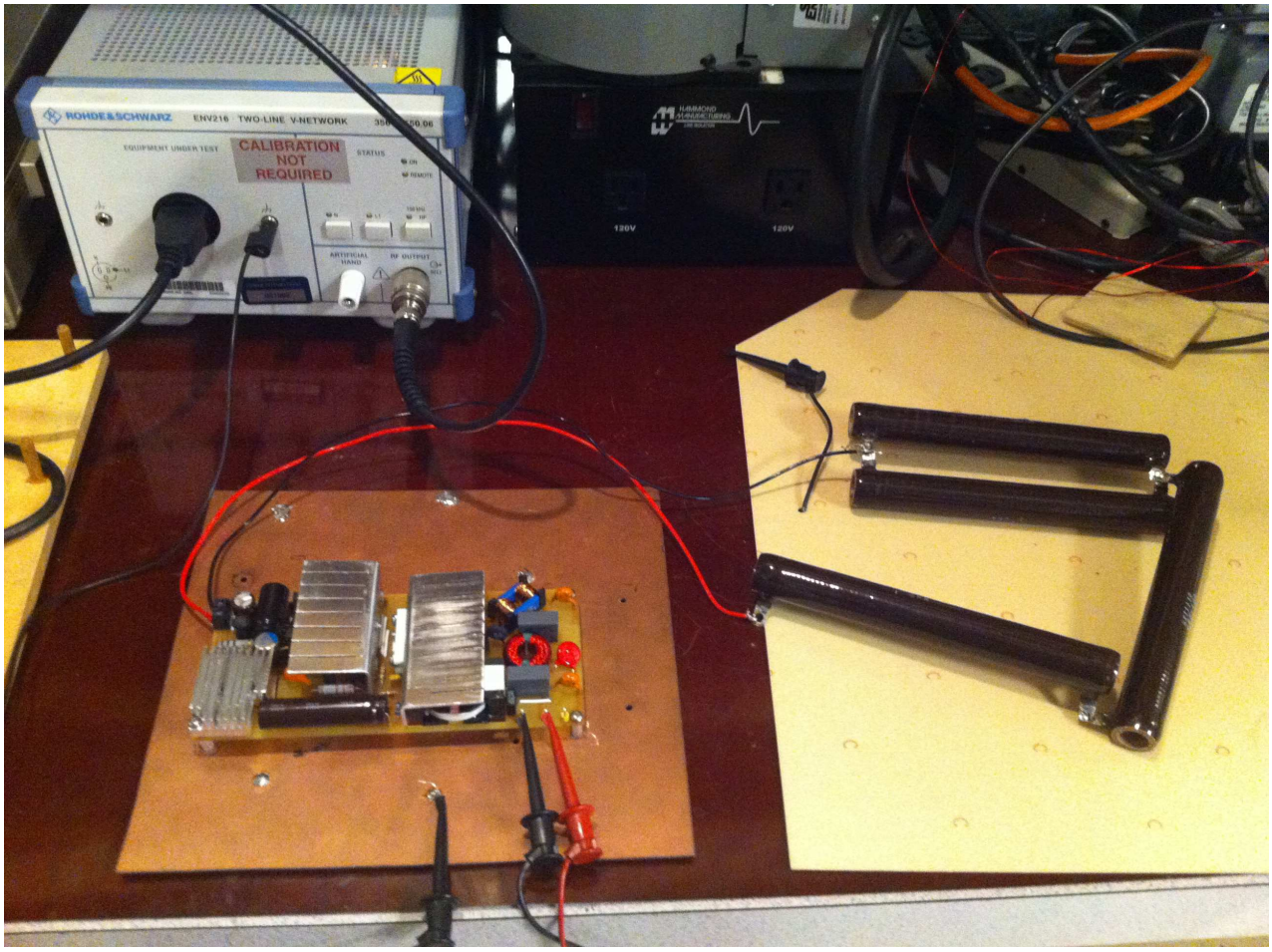

Figure 42 – EMI Test Set-up.

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13.2 EMI Scans

Conducted EMI tests were performed with a resistive load on the 20 V output. The secondary ground of the unit was connected to the metallic copper plane with the help of a screw, which in turn was hard wired to the AC cord ground. The resistive load was left floating.

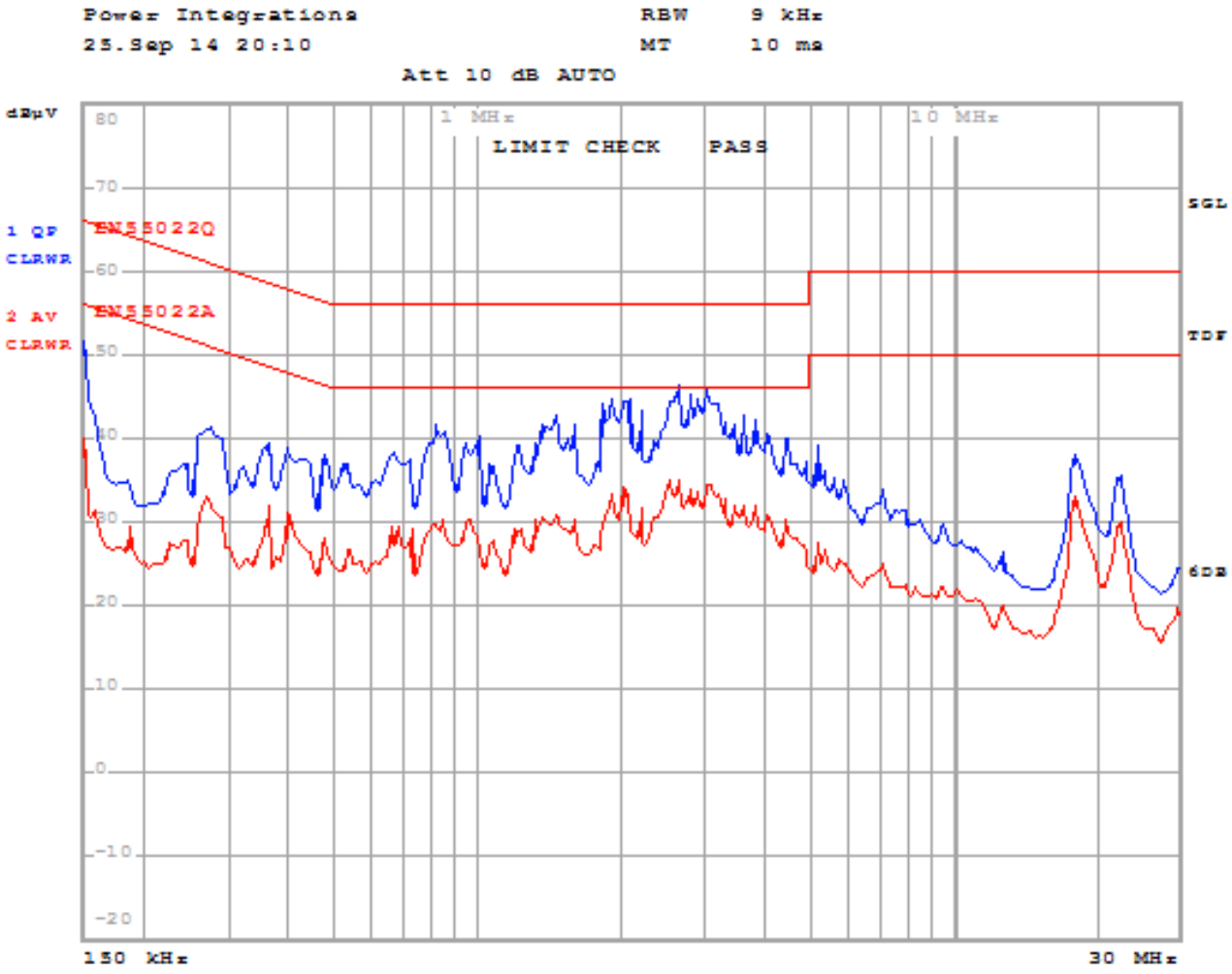

Figure 43 – Conducted EMI, 115 VAC.

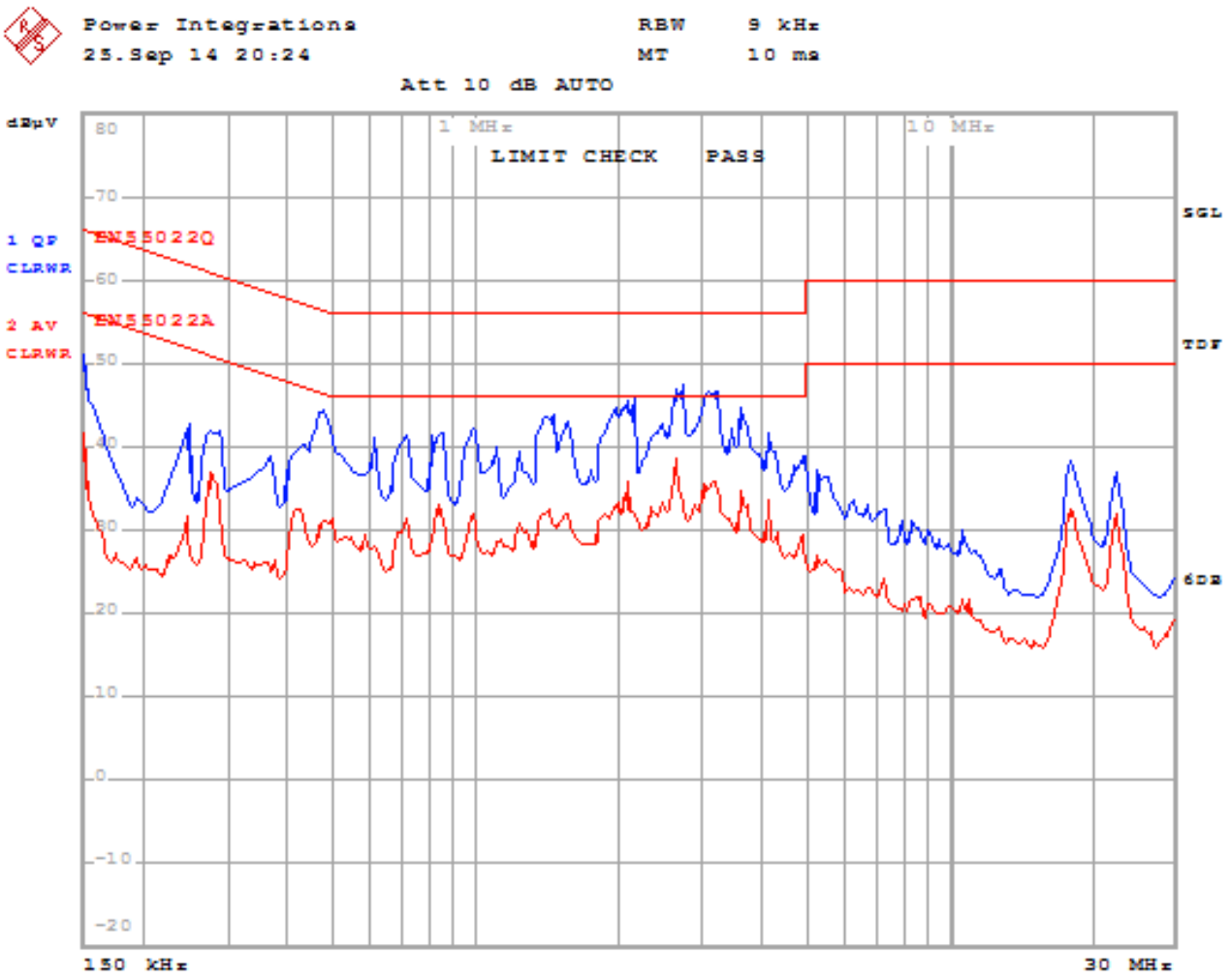

Figure 44 – Conducted EMI, 230 VAC.

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14 Gain-Phase Measurement

14.1 Gain-Phase Measurement Circuit

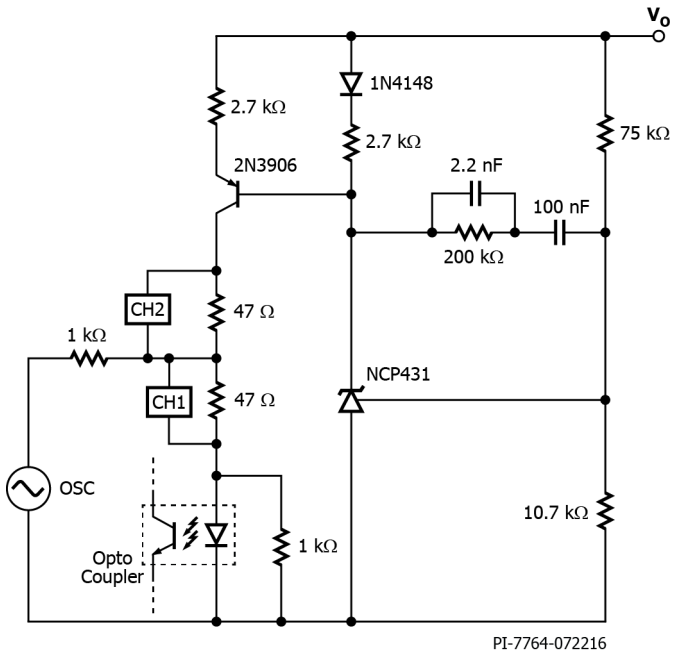

Figure 83 – LinkSwitch-HP Gain-Phase Measurement Schematic.

Note: Current mirror circuit was used inorder to get the clean loop gain plots.

14.2 Gain-Phase Plot

Gain-phase measurements were carried out on DER-437 at 20%, 50% and 100% loads.

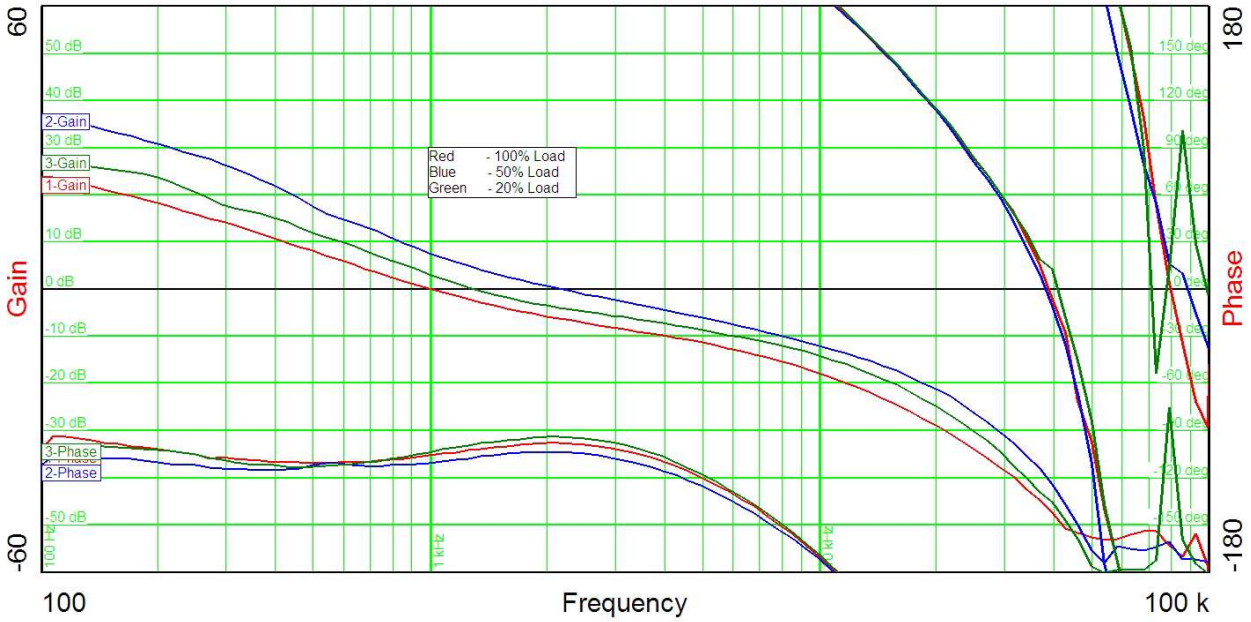

Figure 83 – LINKSwitch-HP Gain-Phase Measurement.

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15 Surge Test

Following common mode and differential mode surge tests were performed on DER-437 power supply. 5 strikes have been applied on each condition.

Combination Wave Surge Test (IEC 61000-4-5)							
S.No	**Polarity**	**Voltage (kV)**	**Time Interval (Sec)**	**Impedance (Ω)**	**Angle (º)**	**Common Mode**	**Test Result**
1	Positive	3	10	12	0, 90, 180, 270	L, N-PE	Pass
2	Negative	3	10	12	0, 90, 180, 270	L, N-PE	Pass
3	Positive	3	10	12	0, 90, 180, 270	L-PE	Pass
4	Negative	3	10	12	0, 90, 180, 270	L-PE	Pass
5	Positive	3	10	12	0, 90, 180, 270	N-PE	Pass
6	Negative	3	10	12	0, 90, 180, 270	N-PE	Pass

Combination Wave Surge Test (IEC 61000-4-5)							
S.No	**Polarity**	**Voltage (kV)**	**Time Interval (Sec)**	**Impedance (Ω)**	**Angle (º)**	**Differential Mode**	**Test Result**
1	Positive	2	10	2	0, 90, 180, 270	L-N	Pass
2	Negative	2	10	2	0, 90, 180, 270	L-N	Pass

16 ESD Test

Power supply has been tested for 16.5 kV air discharge and 8.8 kV contact discharge.

ESD Test						
S.No	**Polarity**	**Voltage (kV)**	**Type of Discharge**	**Applied On**	**No. of Strikes**	**Test Result**
1	Positive	16.5	Air	V_{OUT} (20 V)	10	Pass
2	Negative	16.5	Air	Gnd	10	Pass
3	Positive	8.8	Contact	V_{OUT} (20 V)	10	Pass
4	Negative	8.8	Contact	Gnd	10	Pass

17 Revision History

Date	Author	Revision	Description and Changes	Reviewed
23-Oct-15	SS	3.1	Initial Release.	Apps & Mktg
21-Sept-16	KM	3.2	Updated Figure 83.	

Power Integrations
Tel: +1 408 414 9200 Fax: +1 408 414 9201

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Power Integrations Worldwide Sales Support Locations

WORLD HEADQUARTERS
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Phone: +1-408-414-9665
Fax: +1-408-414-9765
e-mail: usasales@power.com

GERMANY
Lindwurmstrasse 114
80337, Munich
Germany
Phone: +49-895-527-39110
Fax: +49-895-527-39200
e-mail: eurosales@power.com

JAPAN
Kosei Dai-3 Building
2-12-11, Shin-Yokohama,
Kohoku-ku, Yokohama-shi,
Kanagawa 222-0033
Japan
Phone: +81-45-471-1021
Fax: +81-45-471-3717
e-mail: japansales@power.com

TAIWAN
5F, No. 318, Nei Hu Rd.,
Sec. 1
Nei Hu District
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
Fax: +886-2-2659-4550
e-mail:
taiwansales@power.com

CHINA (SHANGHAI)
Rm 2410, Charity Plaza, No. 88,
North Caoxi Road,
Shanghai, PRC 200030
Phone: +86-21-6354-6323
Fax: +86-21-6354-6325
e-mail: chinasales@power.com

INDIA
#1, 14th Main Road
Vasanthanagar
Bangalore-560052
India
Phone: +91-80-4113-8020
Fax: +91-80-4113-8023
e-mail: indiasales@power.com

KOREA
RM 602, 6FL
Korea City Air Terminal B/D,
159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728 Korea
Phone: +82-2-2016-6610
Fax: +82-2-2016-6630
e-mail: koreasales@power.com

UK
Cambridge Semiconductor,
a Power Integrations company
Westbrook Centre, Block 5,
2nd Floor
Milton Road
Cambridge CB4 1YG
Phone: +44 (0) 1223-446483
e-mail: eurosales@power.com

CHINA (SHENZHEN)
17/F, Hivac Building, No. 2, Keji
Nan 8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
Fax: +86-755-8672-8690
e-mail: chinasales@power.com

ITALY
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni (MI)
Italy
Phone: +39-024-550-8701
Fax: +39-028-928-6009
e-mail: eurosales@power.com

SINGAPORE
51 Newton Road,
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
Fax: +65-6358-2015
e-mail: singaporesales@power.com