Design Example Report

Title	*500 W PFC Front End Using 2 x Parallel HiperPFS™-5 PFS5178F PFC Stages*
Specification	90 VAC – 264 VAC Input; 400 VDC Output
Application	PFC Front-End
Author	Applications Engineering Department
Document Number	DER-977
Date	May 22, 2023
Revision	1.0

Summary and Features

- Highly integrated, low component count, low-cost PFC using 2 PFS5178F ICs in parallel
- Low-cost standard output rectifier (MUR460)
- Power Integrations INSOP-28 Low profile SM package
- EN61000-3-2 Class-D compliant
- High PFC efficiency
- Enhanced light load power factor (PF)
  - PF >0.9 at 20% load and 230 VAC, 50 Hz input
  - PF >0.95 at 50% load
- Frequency sliding maintains high efficiency across load range
  - >95% from 10 to 100% load (115 VAC and 230 VAC input)
- Feed forward line sense gain – maintains relatively constant loop gain over entire operating voltage range
- Excellent transient load response
- Frequency adjusted over input line voltage and load
  - Spread-spectrum across >60 kHz window simplifies EMI filtering requirements

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Important Note:
All testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This report describes a PFC power supply utilizing a 2 instances of HiperPFS-5 PFS5178F PFC controller operating as two 250 W paralleled PFC stages, with a total output of 500 W This power supply is intended as a general purpose platform that operates from universal input line voltage and provides a regulated 400 V DC output voltage and continuous output power of 500 W.

The DER-977 power supply is designed to operate with convection cooling for all input and load conditions up to the rated maximum ambient temperature of 50 °C.

This document contains the power supply specification, schematic, bill of materials, inductor documentation, printed circuit layout, and performance data.

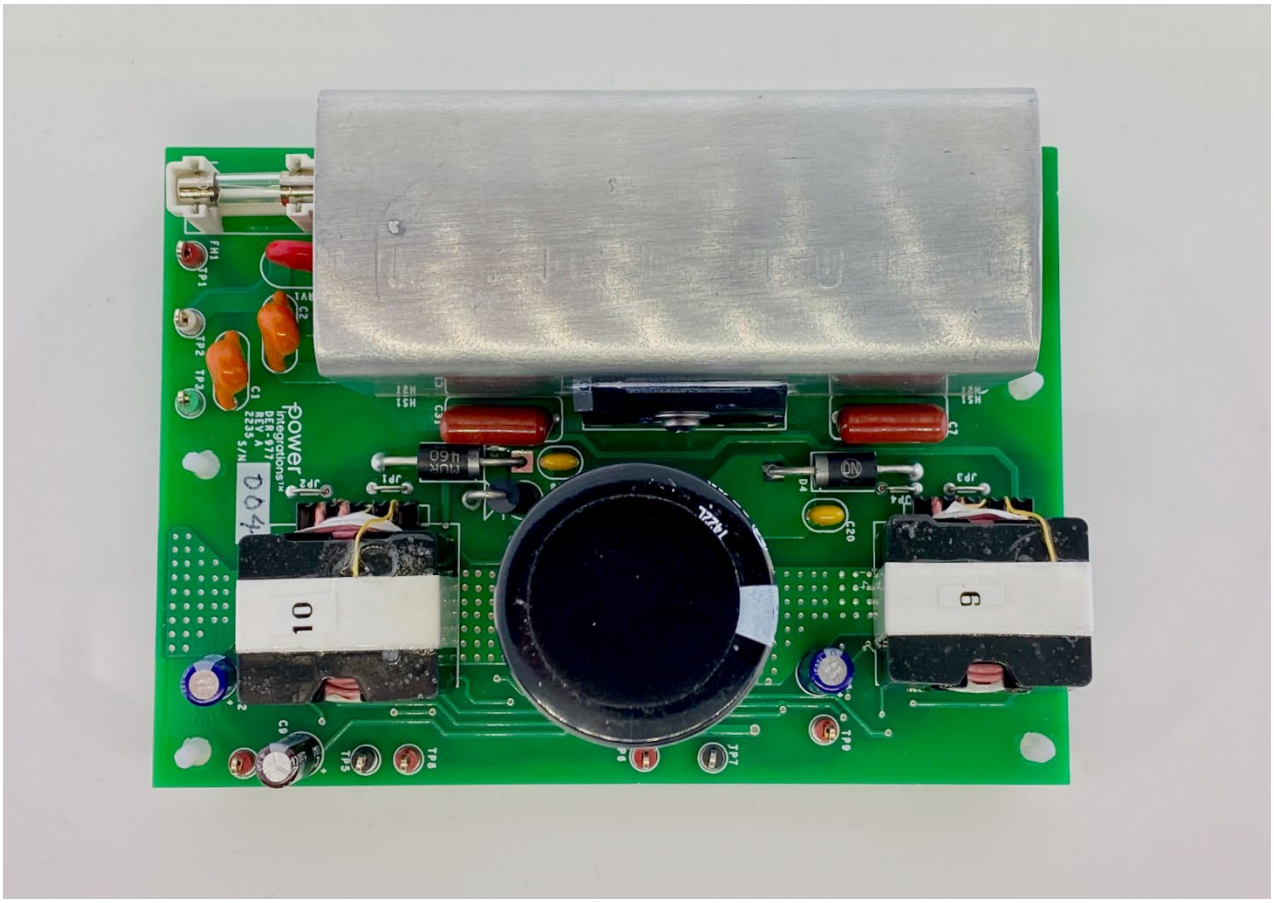


Figure 1 – Populated Circuit Board Photograph (Top View).

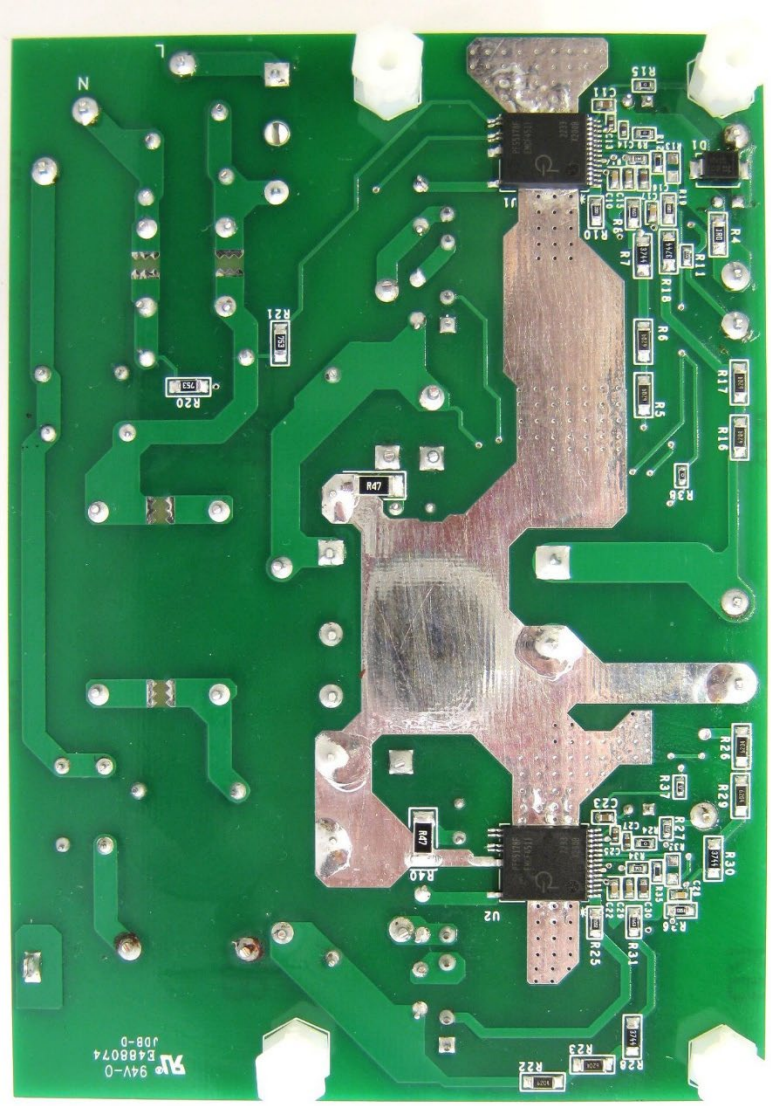


Figure 2 – Populated Circuit Board Photograph (Bottom View).

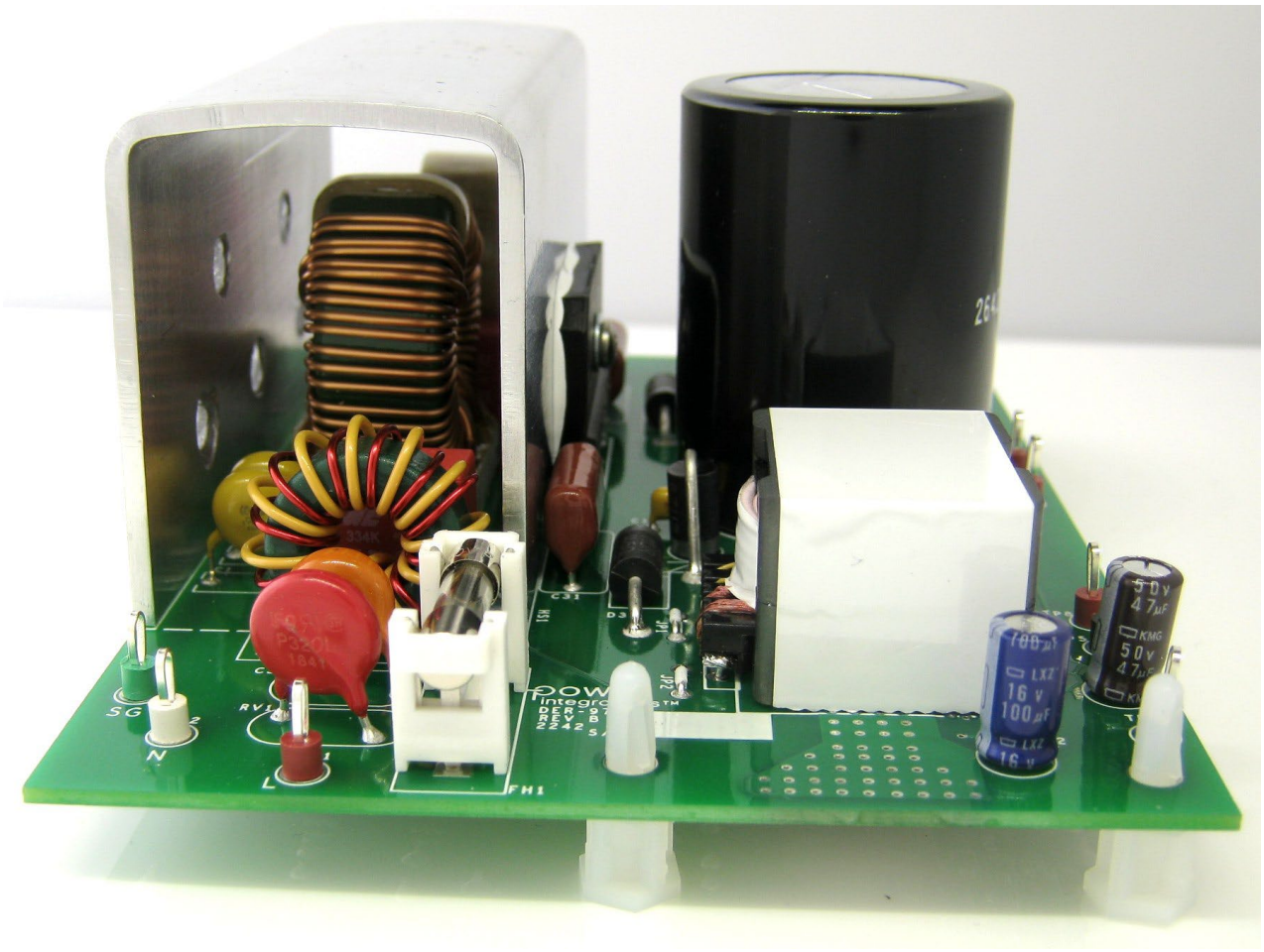


Figure 3 – Populated Circuit Board Photograph (Side View).

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		264	VAC	3 Wire.
Frequency	f_{LINE}	47	50/60	64	Hz	
Output						
Output Voltage	V_{OUT}	395	400	405	V	
Output Ripple Voltage p-p	V_{RIPPLE}			30	V	20 MHz Bandwidth.
Output Current	I_{OUT}		1.25		A	
Total Output Power						
Continuous Output Power	P_{OUT}		500		W	Forced air cooling
Efficiency						
Full Load	η	95			%	Measured at P_{OUT} 25 °C.
Minimum efficiency at 20, 50 and 100 % of P_{OUT}	η_{80+}	94			%	Measured at 115 VAC Input.
Environmental						1.2/50 μs surge, IEC1000-4-5, Series Impedance: Differential Mode: 2 Ω. Common Mode: 12 Ω.
Line Surge						
Differential Mode (L1-L2)			2		kV	
Common mode (L1/L2-PE)			3		kV	
Ambient Temperature	T_{AMB}	0		50	°C	Forced convection required. 300 LFM Min.
Auxiliary Supply Input						
Auxiliary Supply	V_{aux}	8		30	V	DC Supply.

3 Schematic

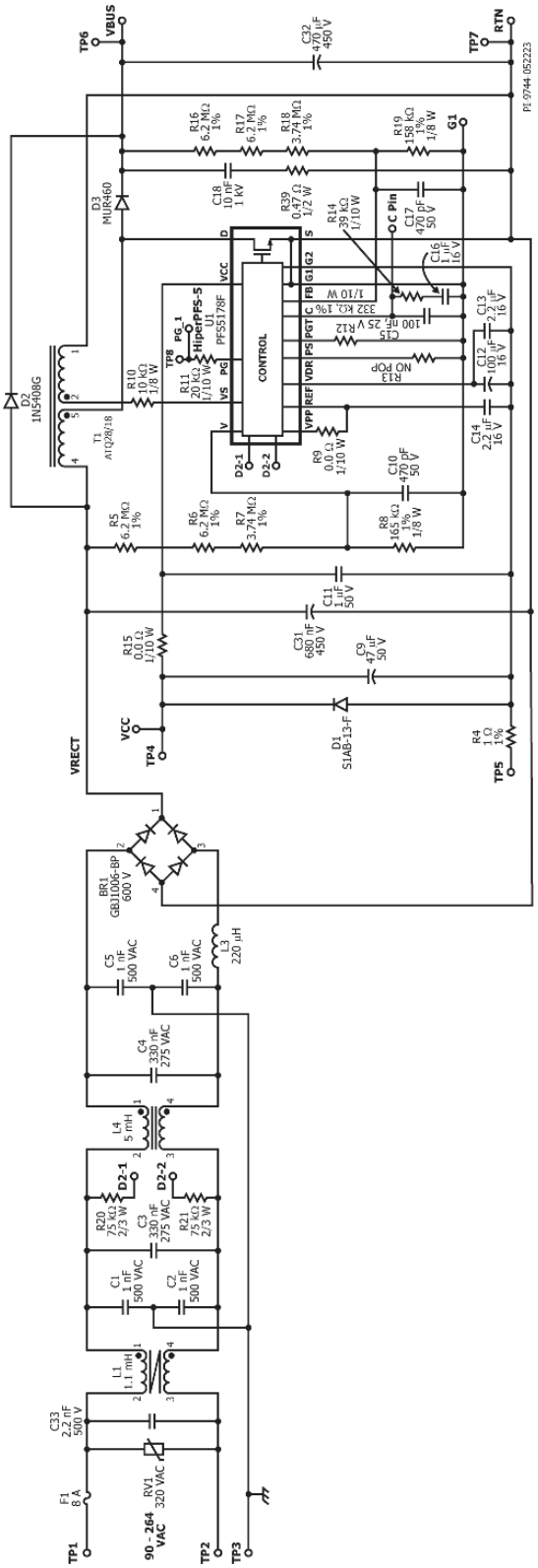


Figure 4 – Schematic, Page 1.

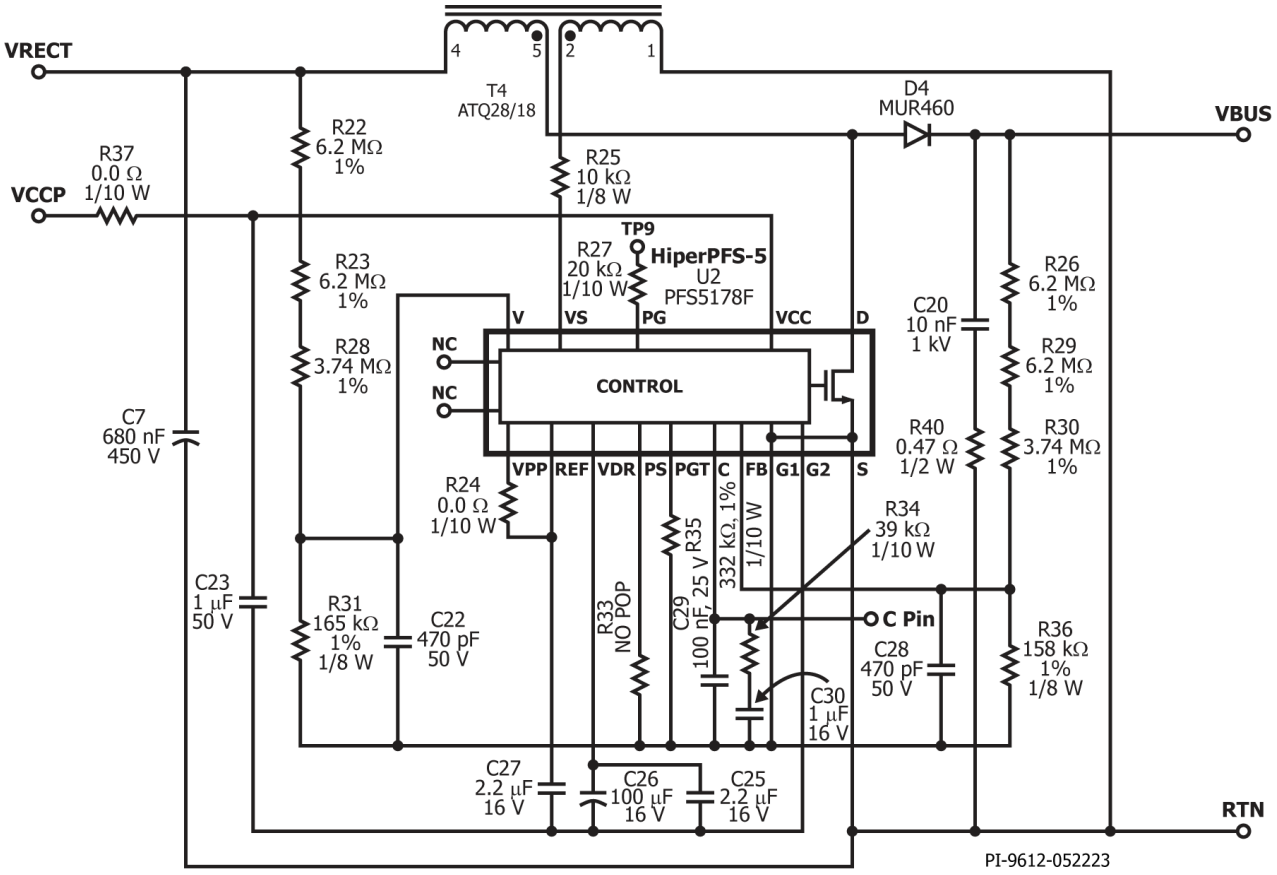


Figure 5 – Schematic, Page 2.

4 Circuit Description

This parallel PFC circuit is designed around the Power Integrations PFS5178F integrated PFC controller. This design is rated for a continuous output power of 500 W and provides a regulated output voltage of 400 VDC nominal, maintaining a high input power factor and overall efficiency over line and load, while remaining low in cost.

4.1 *Input EMI Filter and Rectifier*

Fuse F1 provides overcurrent protection to the circuit and isolates it from the AC supply in the event of a fault. Diode bridge BR1 rectifies the AC input. Capacitors C1, C2, C3, C4, C5 and C6 in conjunction with inductors L1, L3 and L4, constitute the EMI filter for attenuating both common mode and differential mode conducted noise. Film capacitors C7 and C31 provide input decoupling charge storage to reduce input ripple current at the switching frequencies and harmonics.

Resistors R20 and R21 work with the CAPZero, internal to controller / switch U1, to discharge the EMI filter capacitors after line voltage has been removed from the circuit, while dissipating zero power during operation.

Metal oxide varistor (MOV) RV1 protects the circuit during line surge events by effectively clamping the input voltage seen by the power supply.

4.2 *PFS5178F Parallel Boost Converters*

The parallel boost converter stages consist of the boost inductors T1 and T4, along with PFS5178F ICs U1 and U2. These converter stages operate as parallel DCM PFC boost converters, maintaining a sinusoidal input current to the power supply while regulating the output DC voltage.

During start-up, diode D2 provides an inrush current path to the output capacitor C32, bypassing the switching inductors T1 and T4 and switches U1 and U2 in order to prevent a resonant interaction between the switching inductor and output capacitor.

Capacitors C18 and C20 provide a short, high-frequency return path to RTN for improved EMI results and to reduce U1 and U2 GaNFET drain voltage overshoot during turn-off. Resistors R39 and R40 in series with C18 and C20 provide damping to reduce high frequency EMI. Capacitors C9, C11, and C23 decouple and bypass the U1 and U2 VCC pins. Capacitors C12, C13, C25, and C26 decouple the supply for the internal GaNFET drivers inside U1 and U2 via the VDR pins.

Resistors R12 and R35 program the output voltage level [via the POWER GOOD THRESHOLD (PGT) pin] below which the POWER GOOD (PG) pin will go into a high-impedance state.

Capacitors C14 and C27 on the REF pins of U1 and U2 are noise decouplers for the internal voltage reference.

4.3 *Input Feed Forward Sense Circuit*

The input voltage of the power supply is sensed by ICs U1 and U2 using resistors R5-R8 and R22, R23, R28, and R31. Capacitors C10 and C22 bypass the V pins on ICs U1 and U2.

4.4 *Output Feedback*

An output voltage resistive divider network consisting of resistors R16-19 and R26, R29, R30, and R36 provide a scaled voltage proportional to the output voltage as feedback to the controller ICs U1 and U2 setting the PFC output at 400 V. Capacitors C17 and C28 decouple the U1 and U2 FB pins.

Resistor R14 and R34 and capacitors C16 and C30 provide the control loop dominant pole for U1 and U2. Capacitors C15 and C29 provide additional roll-off to attenuate high-frequency noise.

4.5 *Valley Sensing*

PFC inductors T1 and T4 have an auxiliary winding (pins 1 and 2) that is used to sense the valley point of the DCM relaxation ring after the PFC inductor discharges into the load. The signal from each aux winding is applied to the U1 and U2 VS pins via resistors R10 and R25. The PFS5 switches from a valley point of the discontinuous ring waveform to reduce switching losses.

4.6 *Bias Supply*

The PFS5178F, though a self-starting IC, requires a regulated V_{CC} supply of 18-30 VDC for sustained operation, with an absolute maximum voltage rating of 30 V. V_{CC} levels higher than this maximum could result in failure of the IC. Diode D1 and Resistor R4 provide reverse bias protection.

The auxiliary supply is applied to connectors TP4 (+) and TP5 (RTN).

4.7 *Parallel Operation*

The DER-977 consists of two 250 W DCM PFC stages connected in parallel to deliver 500 W. Power sharing between U1 and U2 is accomplished by connecting the C (compensation) pins of U1 and U2 together. The C pin is also the output of the internal OTA error amplifier for the PFS5178F, and its output directly programs the output power of the PFC. Any attempt by one converter to seize output control will result in that converter also driving up the C pin of the companion converter, helping to equalize each converter's contribution to the total output power.

5 PCB Layout

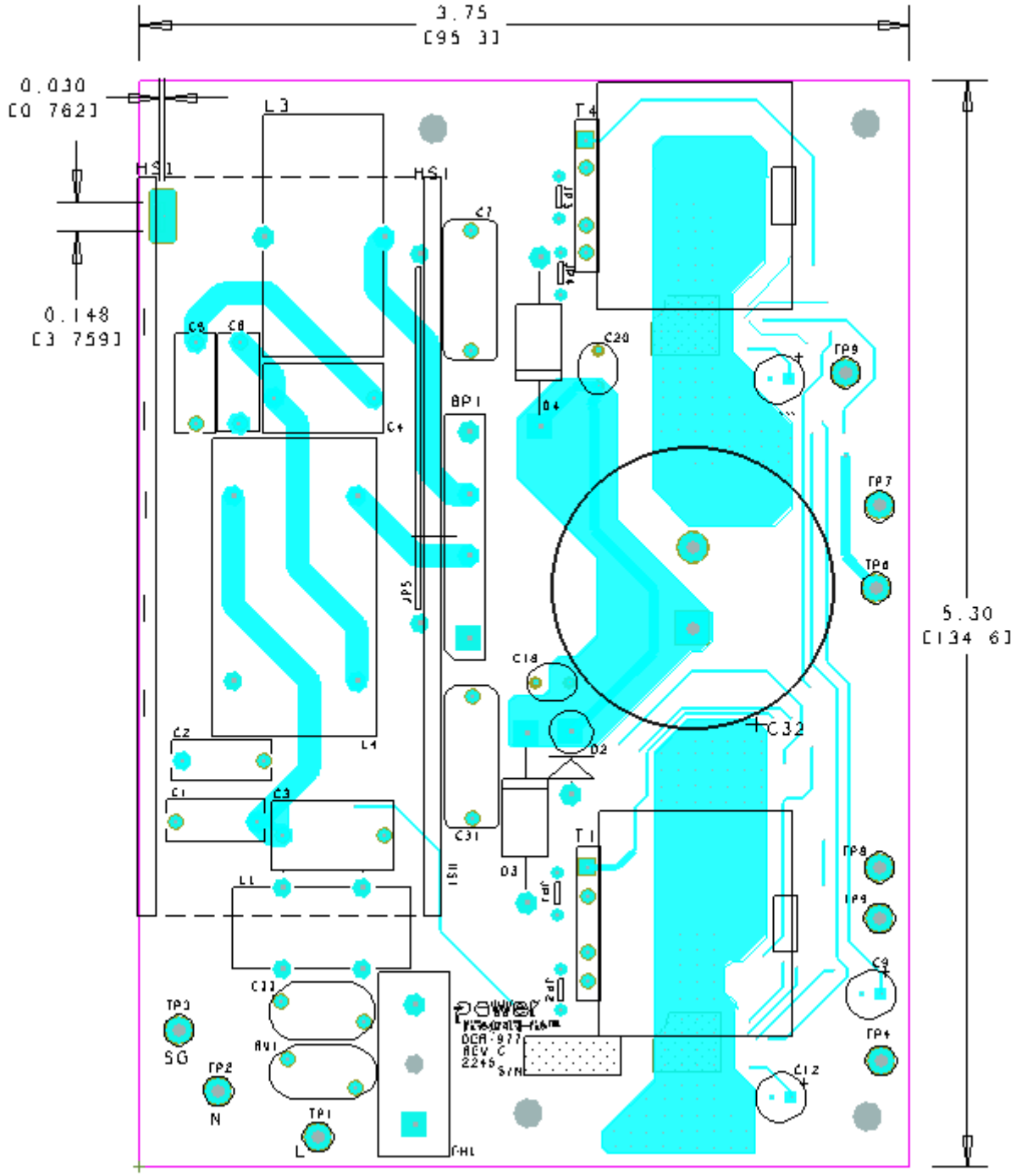


Figure 6 – Printed Circuit Layout, Top.

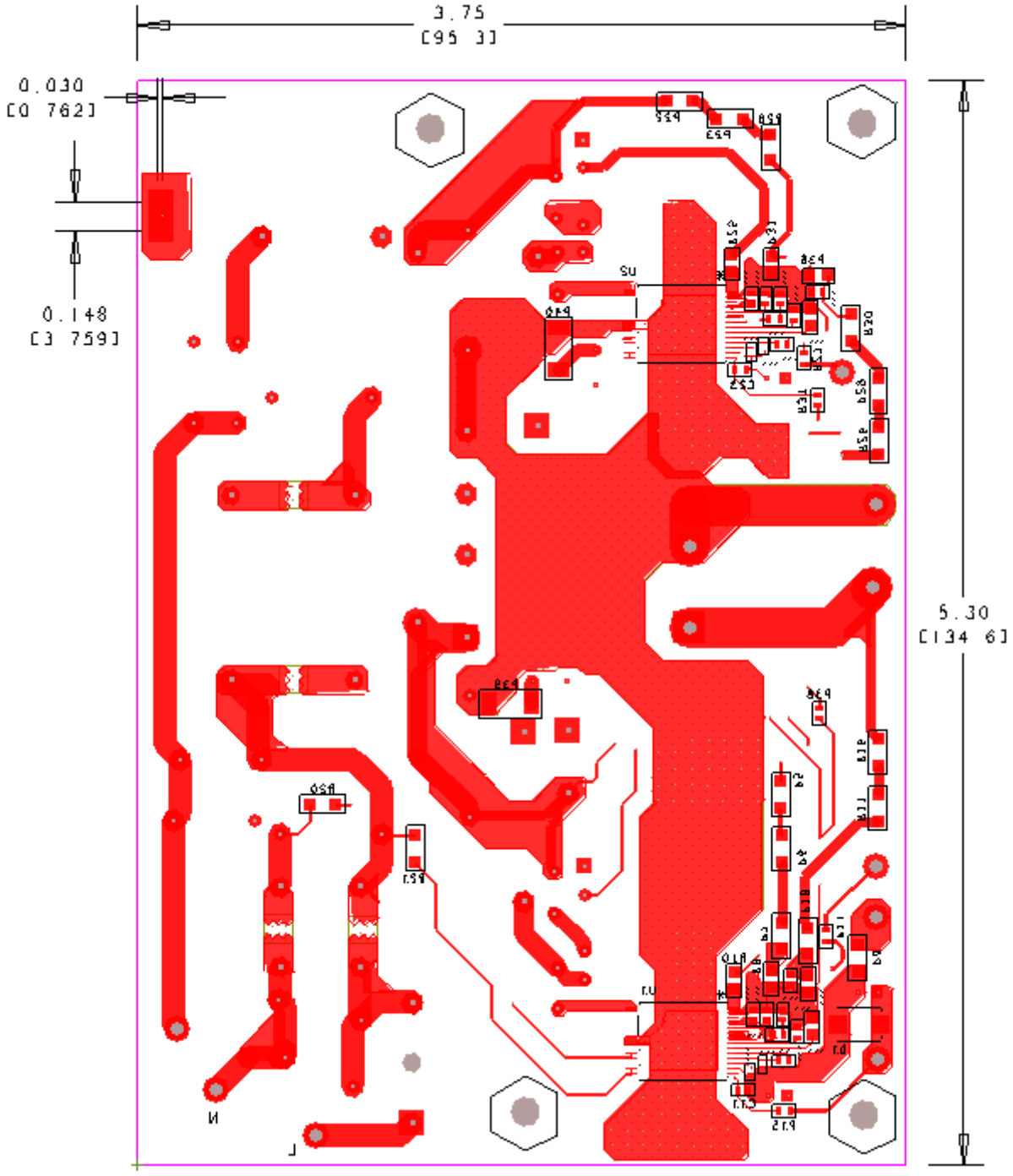


Figure 7 – Printed Circuit Layout, Bottom.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	600 V, 10 A, Bridge Rectifier, GBJ Package	GBJ1006-BP	Micro Commercial
2	4	C1 C2 C5 C6	1 nF, 500 VAC, Ceramic, Y1	VY1102M35Y5UG63V0	Vishay
3	2	C3 C4	330 nF, ±10%, 275 VAC, Polypropylene Film, X2, 15.00 mm x 8.50 mm	890324024003CS	Wurth
4	2	C7 C31	FILM, 0.68 μF, 10%, 450 VDC, RADIAL	ECW-FD2W684K	Panasonic
5	1	C9	47 μF, 50 V, Electrolytic, Gen. Purpose, (6.3 x 11)	EKMG500ELL470MF11D	Nippon Chemi-Con
6	4	C10 C17 C22 C28	470 pF, ±10%, 50 V, Ceramic, X7R, 0603 0.063" L x 0.031" W (1.60 mm x 0.80 mm)	CL10B471KB8NFNC	Samsung
7	2	C11 C23	1 μF, ±10%, 50 V, Ceramic, X5R, -55°C ~ 85°C, 0603	CL10A105KB8NNNC	Samsung
8	2	C12 C26	100 μF, 16 V, Electrolytic, Low ESR, 250 mΩ, (6.3 x 11.5)	ELXZ160ELL101MFB5D	Nippon Chemi-Con
9	4	C13 C14 C25 C27	2.2 μF, ±10%, 16 V, Ceramic, X7R, -55°C ~ 85°C, 0402	GRM155R61C225KE44D	Murata
10	2	C15 C29	100 nF, 0.1μF, ±10%, 25V, Ceramic, X7R, General Purpose, -55°C ~ 125°C, 0603	CL10B104KA8NFNC	Samsung
11	2	C16 C30	1 μF 16 V, Ceramic, X7R, 0603	CL10B105KO8VPNC	Samsung
12	2	C18 C20	10 nF, 1 kV, Disc Ceramic, X7R	SV01AC103KAR	AVX
13	1	C32	470 μF, 450 V, Aluminum Electrolytic Radial, Can - Snap-In, 3000 Hrs @ 105°C, (35 mm x 45 mm)	450HXG470MEFCSN35X45	Rubycon
14	1	C33	2200 PF ±20%, 500 VAC (Y1),760VAC (X1), Ceramic, Y5U (E), RADIAL	440LD22-R	Vishay
15	1	D1	50 V, 1 A, Standard Recovery, GPP, SMB	S1AB-13-F	Diode, Inc.
16	1	D2	1000 V, 3 A, Recitifier, DO-201AD	1N5408G	ON Semi
17	2	D3 D4	600 V, 4 A, Ultrafast Recovery, 35 ns, DO-201AD	MUR460RLG	On Semi
18	1	F1	8 A, 250 V, Fast, 5 mm x 20 mm, Cartridge	0217008.HXP	Littelfuse
19	1	FH1	FUSEHOLDER OPEN 5X20MM PC MNT	64900001039	Wickmann
20	1	HS1	HEAT SINK ASSY, DER-977, AL, 3003, .090”	61-00321-01	Custom
21	4	JP1 JP2 JP3 JP4	Wire Jumper, Non-insulated, #22 AWG, 0.2 in	298	Alpha
22	1	JP5	Wire Jumper, Insulated, TFE, #18 AWG, 1.8 in	C2052A-12-02	Alpha
23	1	L1	1.1 mH, HF Common Mode Choke,	30-00550-00	PI
24	1	L3	220 μH 2 pin Toroidal Choke OD 30 mm, W 15 mm, LS 15 mm	30-00548-00	PI
25	1	L4	5 mH, 8.9 A, Common Mode Choke with header (1.45" W x .80" T x 1.5" H)	8113-RC	Bourns
26	4	POST-CRKT_BRD_6-32_HEX1 POST-CRKT_BRD_6-32_HEX2 POST-CRKT_BRD_6-32_HEX3 POST-CRKT_BRD_6-32_HEX4	Post, Circuit Board, Female, Hex, 6-32, snap, 0.375L, Nylon	561-0375A	Eagle Hardware
27	1	R4	RES, 1 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8RQF1R0V	Panasonic
28	8	R5 R6 R16 R17 R22 R23 R26 R29	RES, 6.2 MΩ, 1%, 1/4 W, Thick Film, 1206	KTR18EZPF6204	Rohm Semi
29	4	R7 R18 R28 R30	RES, 3.74 MΩ, 1%, 1/4 W, Thick Film, 1206	CRCW12063M74FKEA	Vishay

30	2	R8 R31	RES, 165 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1653V	Panasonic
31	4	R9 R15 R24 R37	RES, 0 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEY0R00V	Panasonic
32	2	R10 R25	RES, 10.0 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ103V	Panasonic
33	2	R11 R27	RES, 20 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ203V	Panasonic
34	2	R12 R35	RES, 332 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF3323V	Panasonic
35	2	R13 R33	RES, 180 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ184V	Panasonic
36	2	R14 R34	RES, 39 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ393V	Panasonic
37	2	R19 R36	RES, 158 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1583V	Panasonic
38	2	R20 R21	RES, 75 Ωk, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J753V	Panasonic
39	1	R38	RES,0 Ω Jumper, 1/10 W Chip Resistor 0603 Moisture Resistant Thick Film	RC0603FR-070RL	Yageo
40	2	R39 R40	RES, 0.47 R, 5%, 1/2 W, Thick Film, 2010	ERJ-12ZQJR47U	Panasonic
41	1	RV1	320 Vac, 23 J, 10 mm, RADIAL	V320LA10P	Littlefuse
42	2	T1 T4	DER-977 PFSGAN 250 W Transformer Rev A	25-01199-00	PI
43	4	TP4 TP6 TP8 TP9	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
44	1	TP2	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
45	1	TP3	Test Point, GRN, THRU-HOLE MOUNT	5126	Keystone
46	3	TP1, TP5, TP7	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
47	2	U1 U2	HiperPFS-5 IC, InSOP-T28F	PFS5178F	Power Integrations

7 Inductor Design Spreadsheet

Note: Spreadsheet shows a design for a 250 W PFC stage – two of these stages are paralleled to deliver the 500 W output of the DER-977.

1	Hiper_PFS-5_Boost_050223; Rev.1.2; Copyright Power Integrations 2023	INPUT	INFO	OUTPUT	UNITS	Discontinuous Mode Boost Converter Design Spreadsheet
2	**Enter Application Variables**					**Design Title**
3	Input Voltage Range	Universal		Universal		Input voltage range
4	VACMIN			90	VAC	Minimum AC input voltage. Spreadsheet simulation is performed at this voltage. To examine operation at other votlages, enter here, but enter fixed value for LPFC_ACTUAL.
5	VACMAX			265	VAC	Maximum AC input voltage
6	VBROWNIN			82	VAC	Expected Typical Brown-in Voltage per IC specifications; Line impedance not accounted for.
7	VBROWNOUT			71	VAC	Expected Typical Brown-out voltage per IC specifications; Line impedance not accounted for.
8	VO			400	VDC	Nominal load voltage
9	PO	250		250	W	Nominal Output power
10	fL			50	Hz	Line frequency
11	TA Max			40	°C	Maximum ambient temperature
12	Efficiency Estimate			0.9500		Enter the efficiency estimate for the boost converter at VACMIN. Should approximately match calculated efficiency in Loss Budget section
13	VO_MIN			380	VDC	Minimum Output voltage
14	VO_RIPPLE_MAX			20	VDC	Maximum Output voltage ripple
15	T_HOLDUP			20	ms	Holdup time
16	VHOLDUP_MIN			320	VDC	Minimum Voltage Output can drop to during holdup
17	I_INRUSH			40	A	Maximum allowable inrush current
18	Forced Air Cooling	No		No		Enter "Yes" for Forced air cooling. Otherwise enter "No". Forced air reduces acceptable choke current density and core autopick core size
20	**KP and INDUCTANCE**					
21	LPFC_MIN (0 bias)			119	uH	Minimum PFC inductance value
22	LPFC_TYP (0 bias)			126	uH	LPFC value used for calculations. Enter value to hold constant (also enter core selection) while changing VACMIN to examine brownout operation.
23	LPFC_MAX (0 bias)			132	uH	Maximum PFC inductance value
24	LP_TOL			5.0	%	Tolerance of PFC Inductor Value (ferrite only)
25	LPFC_PEAK			126	uH	Inductance at VACMIN and maximum bias current. For Ferrite, same as LPFC_DESIRED (0 bias)
26	KP_ACTUAL			1.08		Actual KP calculated from LPFC_DESIRED
28	**Basic Current Parameters**					
29	IAC_RMS			2.92	A	AC input RMS current at VACMIN and Full Power load
30	IL_RMS			3.30	A	Inductor RMS current (calculated at VACMIN and Full Power Load)
31	IO_DC			0.63	A	Output average current/Average diode current
34	**PFS Parameters**					
35	PFS Package			F		HiperPFS package selection

36	PFS Part Number	Auto		PFS5178F		If examining brownout operation, over-ride autopick with desired device size
37	Self-Supply Feature	Yes		Yes		Device self-supply feature. Select "Yes" to select device with self-supply feature or "No" for device without self-supply
38	PS_FACTOR	1.0		1.0		Programmable output power selection factor
39	PO_MAX_DEV			250	W	Maximum output power of the device
40	IOCP min			9.22	A	Minimum Current limit
41	IOCP typ			9.70	A	Typical current limit
42	IOCP max			10.19	A	Maximum current limit
43	IP			7.37	A	MOSFET peak current
44	IRMS			2.86	A	PFS MOSFET RMS current
45	RDSON			0.22	Ohms	Typical RDSon at 100 'C
46	FS_PK			90.2	kHz	Estimated frequency of operation at crest of input voltage (at VACMIN)
47	FS_AVG			79.2	kHz	Estimated average frequency of operation over line cycle (at VACMIN)
48	PCOND_LOSS_PFS			1.799	W	Estimated PFS Switch conduction losses
49	PSW_LOSS_PFS			0.031	W	Estimated PFS Switch switching losses
50	PFS_TOTAL			1.830	W	Total Estimated PFS Switch losses
51	TJ Max			100	deg C	Maximum steady-state junction temperature
52	Rth-JS			2.80	°C/W	Maximum thermal resistance (Junction to heatsink)
53	HEATSINK Theta-CA			29.98	°C/W	Maximum thermal resistance of heatsink
56	**INDUCTOR DESIGN**					
57	**Material and Dimensions**					
58	Core Type			Ferrite		Ferrite core
59	Core Material	Auto		PC44/PC95		Select the core material
60	Core Geometry	ATQ		ATQ		Select the core geometry
61	Core	Auto		ATQ28/18.3B		Core part number
62	Ae			153.00	mm^2	Core cross sectional area
63	Le			47.70	mm	Core mean path length
64	AL			9800.00	nH/t^2	Core AL value
65	Ve			7.30	cm^3	Core volume
66	HT (EE/PQ/EQ/RM/POT) / ID (toroid)			4.40	mm	Core height/Height of window; ID if toroid
67	MLT			62.8	mm	Mean length per turn
68	BW			8.50	mm	Bobbin width
69	LG			0.78	mm	Gap length (Ferrite cores only)
70	**Flux and MMF Calculations**					
71	BP_TARGET (ferrite only)	3800		3800	Gauss	Target flux density at worst case: IOCP and maximum tolerance inductance (ferrite only) - drives turns and gap
72	B_OCP (or BP)			3677	Gauss	Target flux density at worst case: IOCP and maximum tolerance inductance (ferrite only) - drives turns and gap
73	B_MAX			2530	Gauss	Peak flux density at AC peak, VACMIN and Full Power Load, nominal inductance,minimum IOCP
77	I_TEST			9.7	A	Current at which B_TEST and H_TEST are calculated, for checking flux at a current other than IOCP or IP; if blank IOCP_typ is used.
78	B_TEST			3500	Gauss	Flux density at I_TEST and maximum tolerance inductance
80	**Wire**					
81	TURNS			24		Inductor turns. To adjust turns, change the BP_TARGET
82	ILRMS			3.30	A	Inductor RMS current
83	Wire type	Litz		Litz		Select between "Litz" or "Magnet" for double coated magnet wire

84	AWG	40		40	AWG	Inductor wire gauge
85	Filar	125		125		Inductor wire number of parallel strands. Leave blank to auto-calc for Litz
86	OD (per strand)			0.079	mm	Outer diameter of single strand of wire
87	OD bundle (Litz only)			1.23	mm	Will be different than OD if Litz
88	DCR			0.055	ohm	Choke DC Resistance
89	P AC Resistance Ratio			0.38		Ratio of total copper loss, including HF AC, to the DC component of the loss
90	J			5.42	A/mm^2	Estimated current density of wires. It is recommended that 4 < J < 6
91	Layers			3.67		Estimated layers in winding
92	**Auxiliary Winding**					
93	N_AUX			2		Recommended auxiliary winding number of turns to ensure the supply to the VS pin
94	V_VS_MAX			1.27	V	Maximum voltage across the auxiliary winding
95	V_VS_MIN			-31.23	V	Minimum voltage across the auxiliary winding
96	RVS			10.00	kohm	Recommended series resistor to the VS pin. Place as close as possible to the VS pin of Hiper-PFS5
97	**Loss Calculations**					
98	BAC-p-p			2379	Gauss	Core AC peak-peak flux excursion at VACMIN, peak of sine wave
99	LPFC_CORE_LOSS			0.412	W	Estimated Inductor core Loss
100	LPFC_COPPER_LOSS			0.659	W	Estimated Inductor copper losses
101	LPFC_TOTAL_LOSS			1.071	W	Total estimated Inductor Losses
104	**PFC Diode**					
105	PFC Diode Part Number	MUR460		MUR460		PFS Diode Part Number
106	Type / Part Number			Ultrafast		PFC Diode Type / Part Number
107	Manufacturer			ON Semi		Diode Manufacturer
108	VRRM			600.0	V	Diode rated reverse voltage
109	IF			4.00	A	Diode rated forward current
110	Qrr			21.0	nC	Qrr at High Temperature
111	VF			1.05	V	Diode rated forward voltage drop
112	PCOND_DIODE			0.642	W	Estimated Diode conduction losses
113	PSW_DIODE			0.000	W	Estimated Diode switching losses
114	P_DIODE			0.642	W	Total estimated Diode losses
115	TJ Max			100.0	deg C	Maximum steady-state operating temperature
116	Rth-JS		Info	6.60	degC/W	Rth too high. Will result in high diode loss
117	HEATSINK Theta-CA			86.34	degC/W	Maximum thermal resistance of heatsink
118	IFSM			110.0	A	Non-repetitive peak surge current rating. Consider larger size diode if inrush or thermal limited.
121	**Output Capacitor**					
122	COUT	Auto		180	uF	Minimum value of Output capacitance
123	VO_RIPPLE_EXPECTED			11.6	V	Expected ripple voltage on Output with selected Output capacitor
124	T_HOLDUP_EXPECTED			20.7	ms	Expected holdup time with selected Output capacitor
125	ESR_LF			0.92	ohms	Low Frequency Capacitor ESR
126	ESR_HF			0.37	ohms	High Frequency Capacitor ESR
127	IC_RMS_LF			0.39	A	Low Frequency Capacitor RMS current
128	IC_RMS_HF			1.48	A	High Frequency Capacitor RMS current
129	CO_LF_LOSS			0.138	W	Estimated Low Frequency ESR loss in Output capacitor
130	CO_HF_LOSS			0.804	W	Estimated High frequency ESR loss in Output capacitor

131	Total CO LOSS			0.942	W	Total estimated losses in Output Capacitor
134	**Input Bridge (BR1) and Fuse (F1)**					
135	I^2t Rating			12.64	A^2*s	Minimum I^2t rating for fuse
136	Fuse Current rating			4.49	A	Minimum Current rating of fuse
137	VF			0.90	V	Input bridge Diode forward Diode drop
138	IAVG			2.79	A	Input average current at VBROWNOUT.
139	PIV_INPUT BRIDGE			375	V	Peak inverse voltage of input bridge
140	PCOND_LOSS_BRIDGE			4.739	W	Estimated Bridge Diode conduction loss
141	CIN			0.82	uF	Input capacitor. Use metallized polypropylene or film foil type with high ripple current rating
142	CIN_DF			0.001		Input Capacitor Dissipation Factor (tan Delta)
143	CIN_PLOSS			0.012	W	Input Capacitor Loss
144	RT1			9.37	ohms	Input Thermistor value. Adjust I_INRUSH to get the closest standard thermistor value
145	D_Precharge			1N5407		Recommended precharge Diode
148	**PFS5 Small Signal Components**					
149	RVS			10.0	kOhms	VS pin resistor for valley sensing. This resistor should be optimized such that proper delay is introduced from the instant the voltage on the sense winding goes below the Vvs2 threshold to the instant when the cascode turns-on (valley sensing). Must be tested on the bench
150	RPS			> 400	kOhms	Power programmability resistor. Leaving PS pin open is acceptable
151	RV1			4.0	MOhms	Line sense resistor 1
152	RV2			6.0	MOhms	Line sense resistor 2
153	RV3			6.0	MOhms	Typical value of the lower resistor connected to the V-PIN. Use 1% resistor only!
154	RV4			161.6	kOhms	Description pending, could be modified based on feedback chain R1-R4
155	C_V			0.495	nF	V pin decoupling capacitor (RV4 and C_V should have a time constant of 80us) Pick the closest available capacitance.
156	C_VCC			1.0	uF	Supply decoupling capacitor
157	C_C			100	nF	Feedback C pin decoupling capacitor
158	Power good Vo lower threshold VPG(L)			333	V	Vo lower threshold voltage at which power good signal will trigger
159	PGT set resistor			320.5	kohm	Power good threshold setting resistor
162	**Feedback Components**					
163	RFB_1			4.00	Mohms	Feedback network, first high voltage divider resistor
164	RFB_2			6.00	Mohms	Feedback network, second high voltage divider resistor
165	RFB_3			6.00	Mohms	Feedback network, third high voltage divider resistor
166	RFB_4			155.5	kohms	Feedback network, lower divider resistor
167	CFB_1			0.514	nF	Feedback network, loop speedup capacitor. (R4 and C1 should have a time constant of 80us) Pick the closest available capacitance.
168	RFB_5			30.1	kohms	Feedback network: zero setting resistor
169	CFB_2			1000	nF	Feedback component- noise suppression capacitor
172	**Loss Budget (Estimated at VACMIN)**					
173	PFS Losses			1.830	W	Total estimated losses in PFS
174	Boost diode Losses			0.642	W	Total estimated losses in Output Diode

175	Input Bridge losses			4.739	W	Total estimated losses in input bridge module
176	Input Capacitor Losses			0.012	W	Total estimated losses in input capacitor
177	Inductor losses			1.071	W	Total estimated losses in PFC choke
178	Output Capacitor Loss			0.942	W	Total estimated losses in Output capacitor
179	EMI choke copper loss			0.855	W	Total estimated losses in EMI choke copper
180	Total losses			10.090	W	Overall loss estimate
181	Efficiency			96.12	%	Estimated efficiency at VACMIN, full load.
184	**HiperPFS-5 Integrated CAPZero Function**					
185	Total Series Resistance (Rcapzero1+Rcapzero2)			0.602	MOhms	Maximum total series resistor value to discharge X-capacitors with time constant of 1 second. Resistors must be connected to D1 and D2 pins of the HiperPFS-5 part for integrated CAPZero function
188	**EMI Filter Components Recommendation**					
189	CX2			680	nF	X-capacitor after differencial mode choke and before bridge, ratio with Po
190	LDM_calc			169	uH	Estimated minimum differential inductance to avoid <10kHz resonance in input current
191	CX1			470	nF	X-capacitor before common mode choke, ratio with Po
192	LCM			10.0	mH	Typical common mode choke value
193	LCM_leakage			30	uH	Estimated leakage inductance of CM choke, typical from 30~60uH
194	CY1 (and CY2)			220	pF	typical Y capacitance for common mode noise suppression
195	LDM_Actual			139	uH	cal_LDM minus LCM_leakage, utilizing CM leakage inductance as DM choke.
196	DCR_LCM			0.070	Ohms	Total DCR of CM choke for estimating copper loss
197	DCR_LDM			0.030	Ohms	Total DCR of DM choke(or CM #2) for estimating copper loss
199	Note: CX2 can be placed between CM choke and DM choke depending on EMI design requirement.					

Note Value of CIN used in DER977 is 0.68 µF rather than 0.82 µF shown in spreadsheet.

8 PFC Inductor Specification

8.1 *Electrical Diagram*

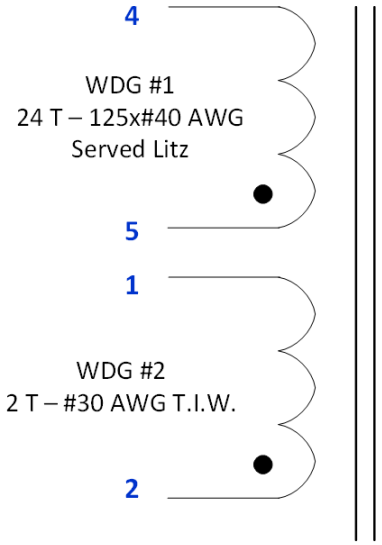


Figure 8 – Inductor Electrical Diagram.

8.2 *Electrical Specifications*

Inductance	Pins 4-5 measured at 100 kHz, 0.4 RMS.	130 µH +5%
Resonant Frequency	Pins 4-5. N/A	kHz (Min.)

8.3 *Materials*

Item	Description
[1]	Core: ATQ28-18, Gap for A_L of 226 nH/T^2 PI P/N 99-00071-00.
[2]	Bobbin: ATQ 28/18 Vertical, 5 Pins, (5/0) PI P/N 25-01170-00.
[3]	Litz Wire: 125 #40 AWG Single Coated Solderable, Served.
[4]	Triple Insulated Wire, #30 AWG, Furukawa Tex=E or Equivalent.
[5]	Tape, Polyester Film: 3M 1350-F1 or Equivalent, 9 mm Wide.
[6]	Foil, Copper, 0.002” (0.051mm) thick, 6 mm Wide (cut down from 10 mm wide foil).
[7]	Varnish: Dolph BC-359, or Equivalent.

8.4 *Inductor Build Diagram*

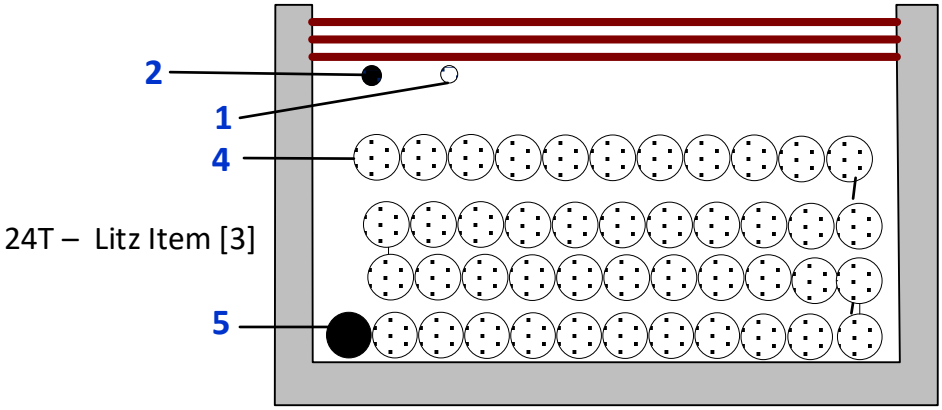
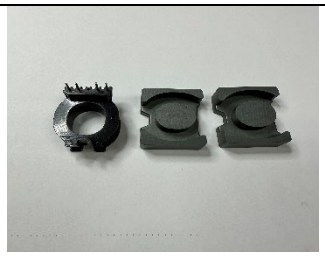
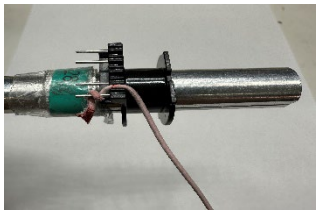
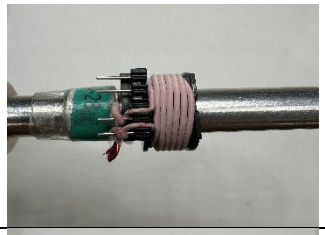
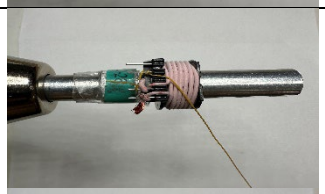
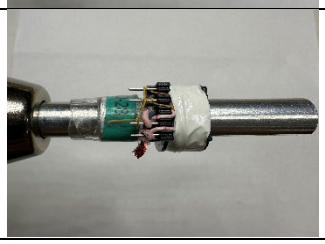


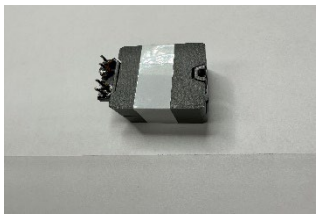
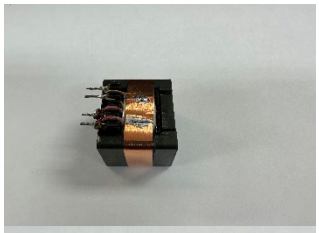
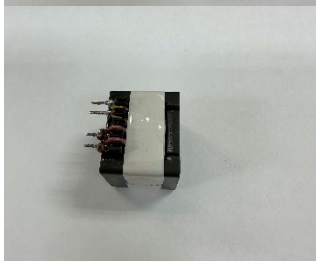
Figure 9 – Inductor Build Diagram.

8.5 *Inductor Construction*

Bobbin prep	Pull pin 3 of bobbin [2].
WDG #1 (Main Wdg)	Starting at pin 5, wind 24 turns of Litz Wire [3] in four layers. Finish at pin 4.
WDG #2 (desmag sense wdg)	Starting at pin 1, wind 2 turns of TIW [4]. Finish on pin 1.
Insulation	Apply 3 turns of tape [5] for finish wrap.
Core Gapping	Grind core for inductance of 130 uH +/- 5%
Assembly	Assemble core halves and bobbin. Secure cores with 2 turns of tape [5]
Flux band	Using copper foil [6], apply a flux band around the outside perimeter of the transformer, centered in the bobbin window. Secure foil ends with solder to form a shorted turn.
Grounding wire	Solder 1” piece of TIW [4] to copper band near pin 1. Terminate wire on pin 1.
Insulating wrap	Cover copper flux band with 2 turns of tape [5].
Varnish	Dip varnish [7].

8.6 *Winding Illustrations*

Winding preparation		Bobbin & Cores. Pull pin 3 of bobbin.
WD1 **Main Wdg**	 	Start at pin 5, wind 24 turns of Litz wire item [3] in four layers, Finish at pin 4.
WD2 **Demag sense Wdg**	 	Starting at pin 2, Wind 2 turns of TIW (4). Finish on pin1.
Insulation		Apply 3 turns of tape item [5] for finish wrap.

Core Gapping & Assembly		Grind core for inductance of 130 uH +/_ 5% Assemble core halves and bobbin. Secure cores with 2 turns of tape [5]
Flux band & Grounding wire	 	Using copper foil [6], apply a flux band around the outside of transformer, centered in the bobbin window. Secure foil ends with solder to form a shorted turn. Solder 1" piece of TIW [4] to copper band near pin 1. Terminate wire on pin 1.
Insulating Wrap	 Finished Inductor	Cover copper flux band with 2 turns of tape [5] Dip Varnish [7].

9 L3 Differential Mode Inductor

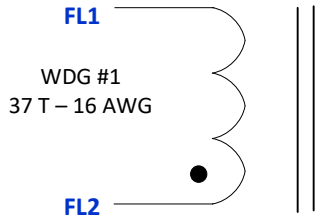


Figure 10 – Inductor Schematic Diagram.

9.1 *Electrical Specifications*

Inductance	Pins 4-5 measured at 100 kHz, 0.4 RMS.	220 µH +10%
Resonant Frequency	Pins 4-5. N/A	kHz (Min.)

9.2 *Materials*

Item	Description
[1]	Core: Sendust / Kool-Mu, 125u, Magnetics, Inc. 77930-A7 or Equivalent.
[2]	Magnet Wire, 1#6 AWG, Double Coated.
{3}	Tape, Polyester Web, 3M #44 or equivalent, 8 mm Wide.

Use hook winder to apply turns on core. After winding, apply circumferential wrap of 2 turns of tape [3].

Figure 11 – Finished Inductor.

10 L1 High Frequency Common Mode Choke

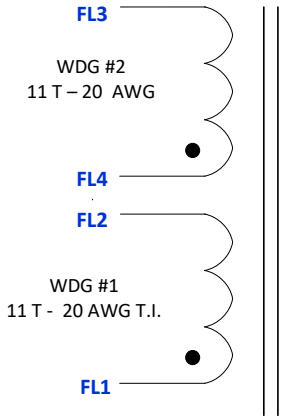


Figure 12 – Inductor Electrical Diagram

10.1 *Inductor Electrical Specifications*

Inductance	Pins FL1 – FL2 or FL3 – FL4 measured at 100 kHz, 0.4 RMS.	1.1 mH +20%
Resonant Frequency	Pins 4-5. N/A	kHz (Min.)

10.2 *Materials*

Item	Description
[1]	Toroid Core, Ferrite, Coated, High Perm. P/N 30-00398-00
[2]	Magnet wire, 20AWG
[3]	Triple Insulated Wire, Furukawa TEX-E or equivalent, 20 AWG

10.3 *Winding Instructions*

Winding	Using 1 strand each of magnet wire [2] and triple Insulated wire [3], wind 11 bifilar turns in 1 layer on toroid [1]
Termination	Trim flying leads to ½ in, tin to within 1/8 inch of toroid.

Figure 13 – Finished Inductor.

11 Diode Bridge BR1 Heat Sink

11.1 *BR1 Heat Sink Sheet Metal*

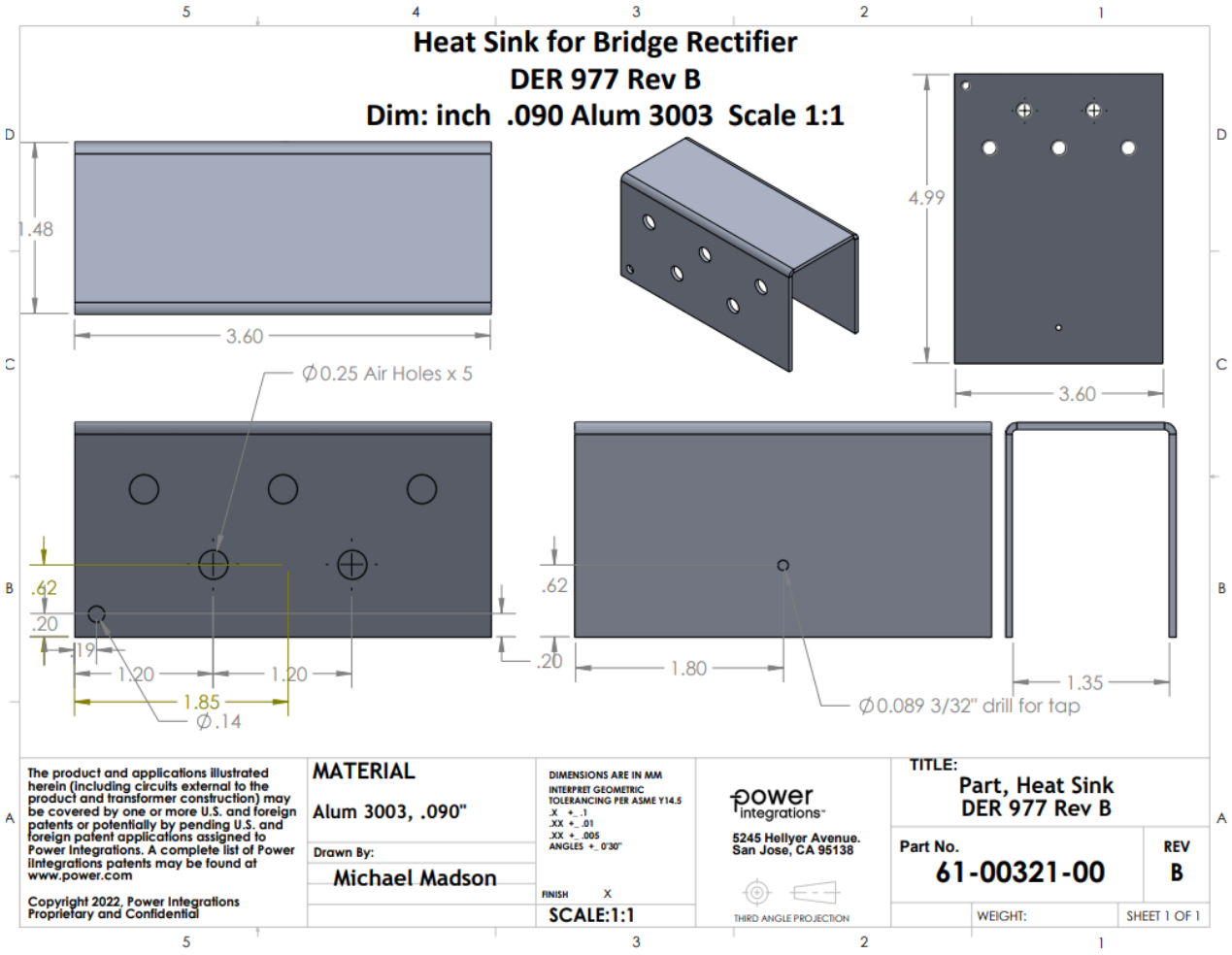


Figure 14 – DER977 Bridge Rectifier Heat Sink, Sheet Metal

11.2 *BR1 Heat Sink Fabrication Drawing*

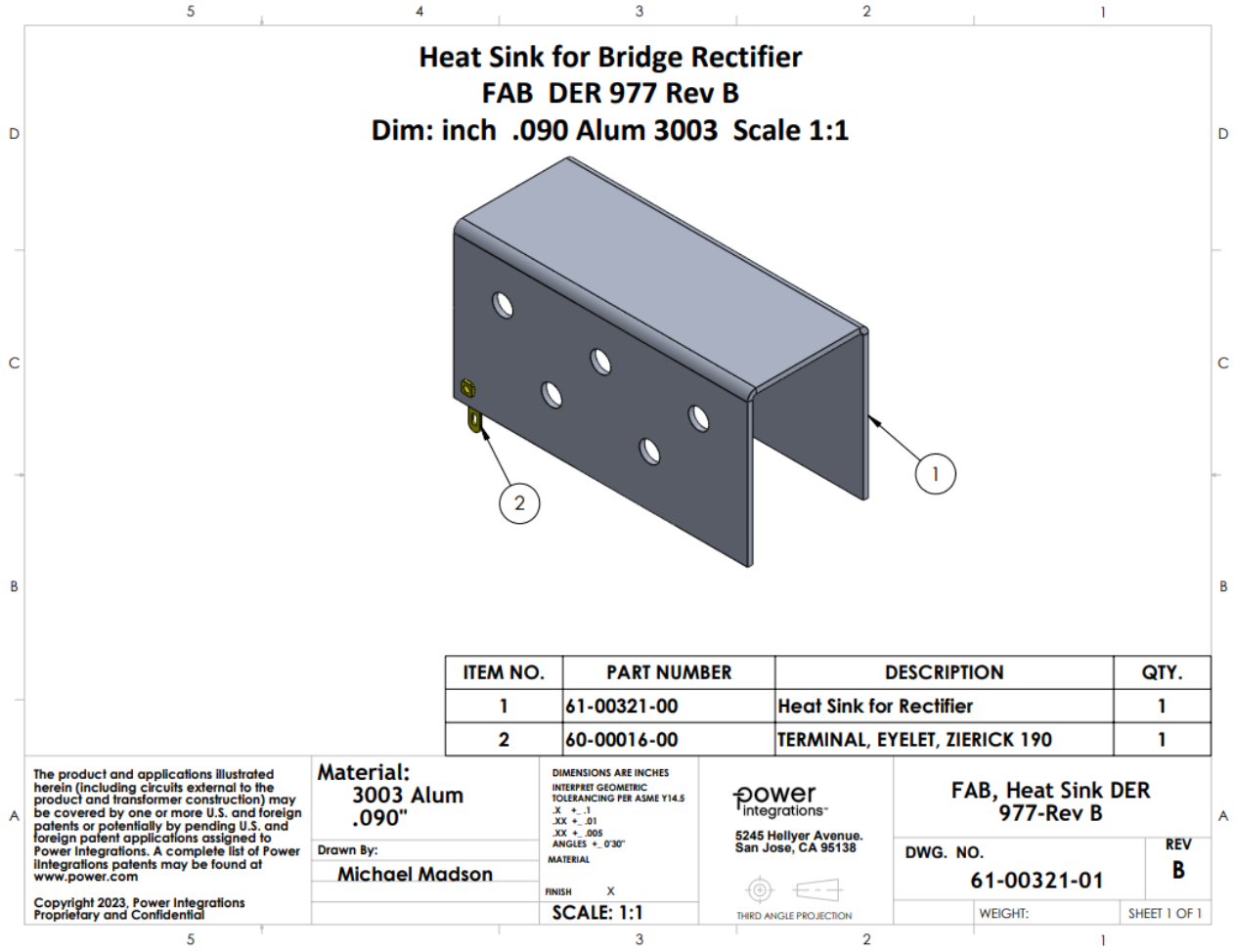
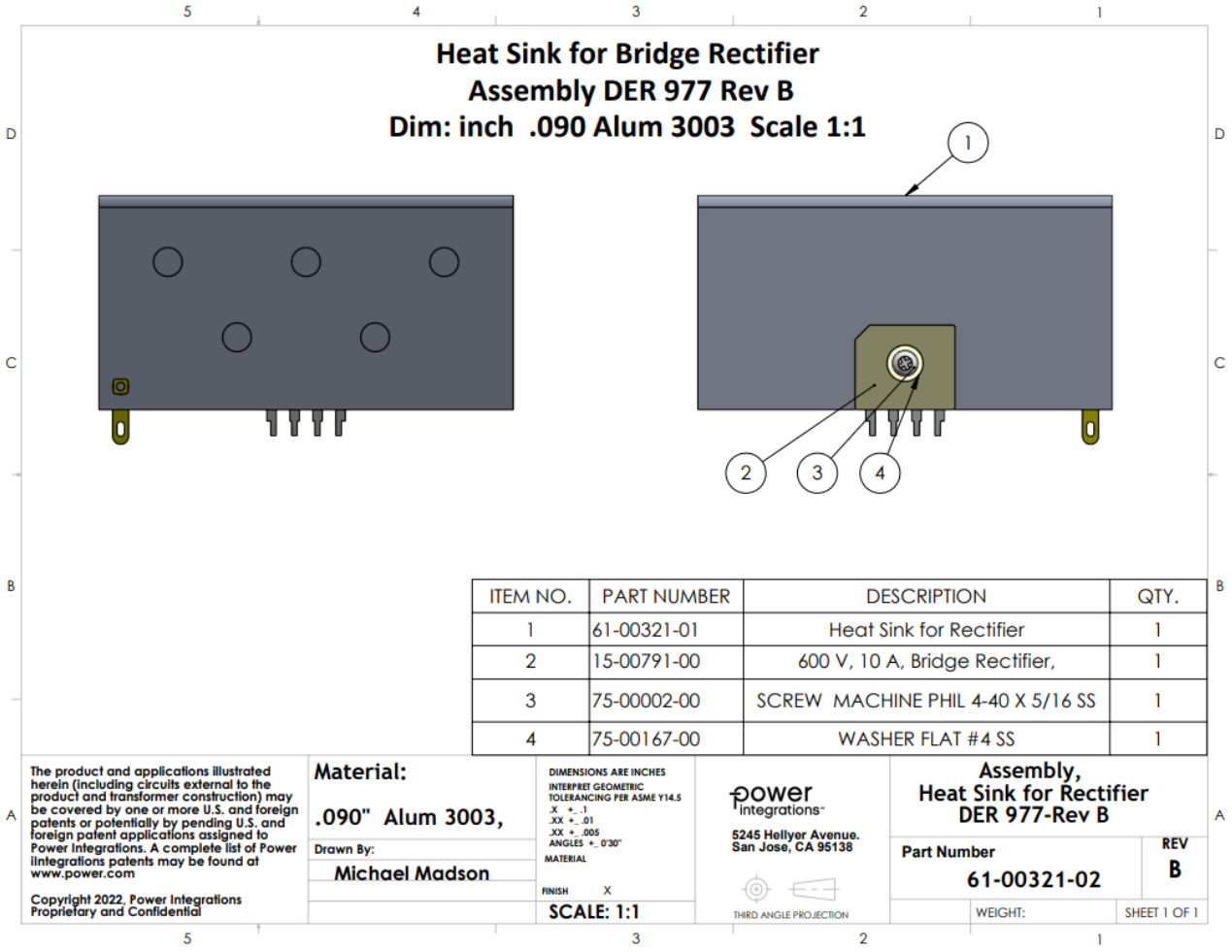


Figure 15 – DER977 Bridge Rectifier Heat Sink, Assembly with Fastener

11.3 *BR1 / Heat Sink Assembly Drawing*



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00321-01	Heat Sink for Rectifier	1
2	15-00791-00	600 V, 10 A, Bridge Rectifier,	1
3	75-00002-00	SCREW MACHINE PHIL 4-40 X 5/16 SS	1
4	75-00167-00	WASHER FLAT #4 SS	1

Material:
.090" Alum 3003,

Drawn By:
Michael Madson

DIMENSIONS ARE INCHES
INTERPRET GEOMETRIC TOLERANCING PER ASME Y14.5
.X +-.1
.XX +-.01
.XX +-.005
ANGLES +-.0'30"
MATERIAL
FINISH X
SCALE: 1:1

power integrations
5245 Hellyer Avenue.
San Jose, CA 95138
THIRD ANGLE PROJECTION

Assembly,
Heat Sink for Rectifier
DER 977-Rev B

Part Number
61-00321-02

REV
B

WEIGHT:
SHEET 1 OF 1

Figure 16 – DER977 Bridge Rectifier Heat Sink, Final Assy with Bridge Rectifier

12 Performance Data

All measurements performed at room temperature, 60 Hz input frequency for voltages below 150 VAC and input frequency of 50 Hz for 150 VAC and higher.

12.1 *No-Load Input Power*

Input power was measured using a Yokogawa WT210 set for integration mode, with an integration time of 20 minutes.

The UUT was operated with an auxiliary V_{CC} of 12 V. V_{CC} voltage and current were measured as 11.99 V and 1.33 mA, resulting in a V_{CC} power consumption of 15.95 mW. The table below shows the sum of no-load consumption plus Vcc consumption.

90 VAC		115 VAC		230 VAC		264 VAC	
P_{OUT} (mW)	P_{IN} (mW)	P_{OUT} (mW)	P_{IN} (mW)	P_{OUT} (mW)	P_{IN} (mW)	P_{OUT} (mW)	P_{IN} (mW)
0	48.99	0	54.09	0	85.13	0	97.64

12.2 *PFC Efficiency*

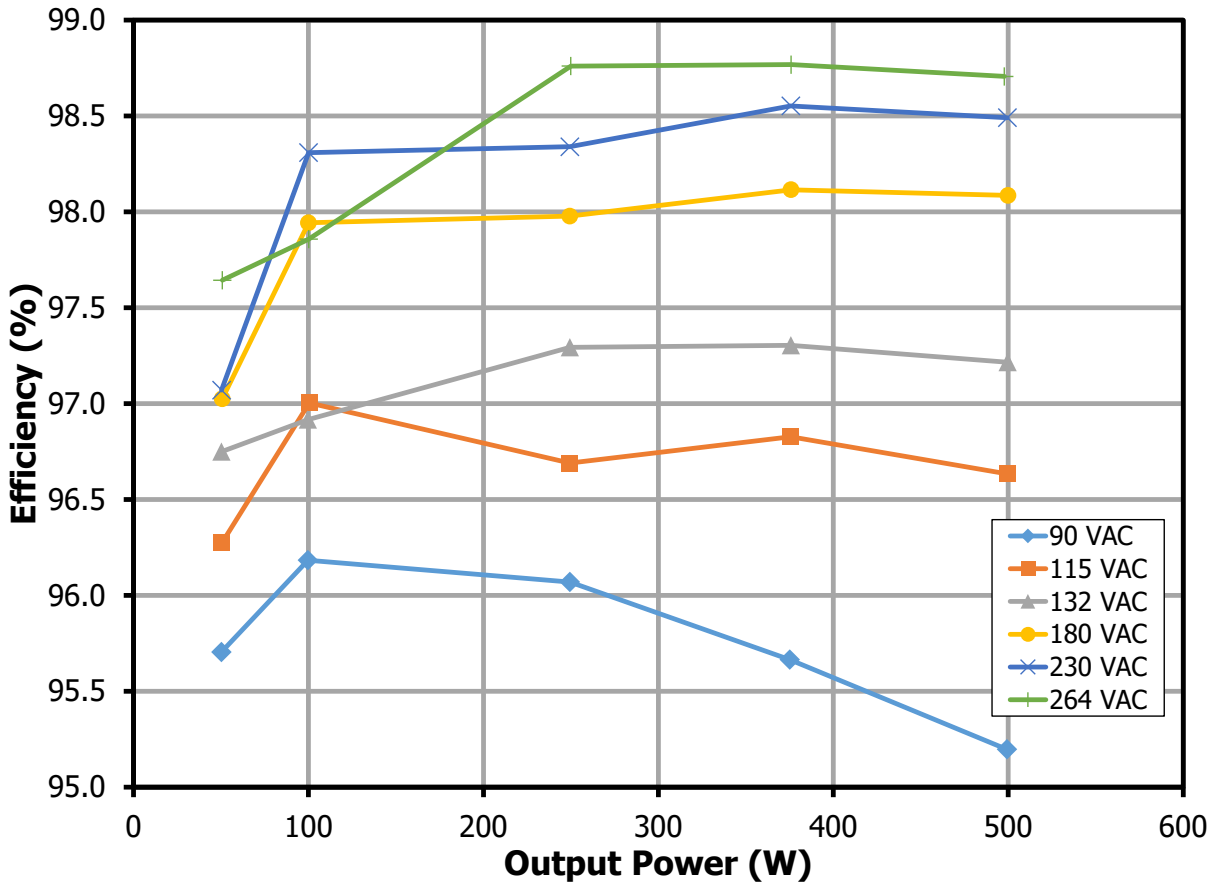


Figure 17 – Efficiency vs. Output Power.

12.3 *Power Factor*

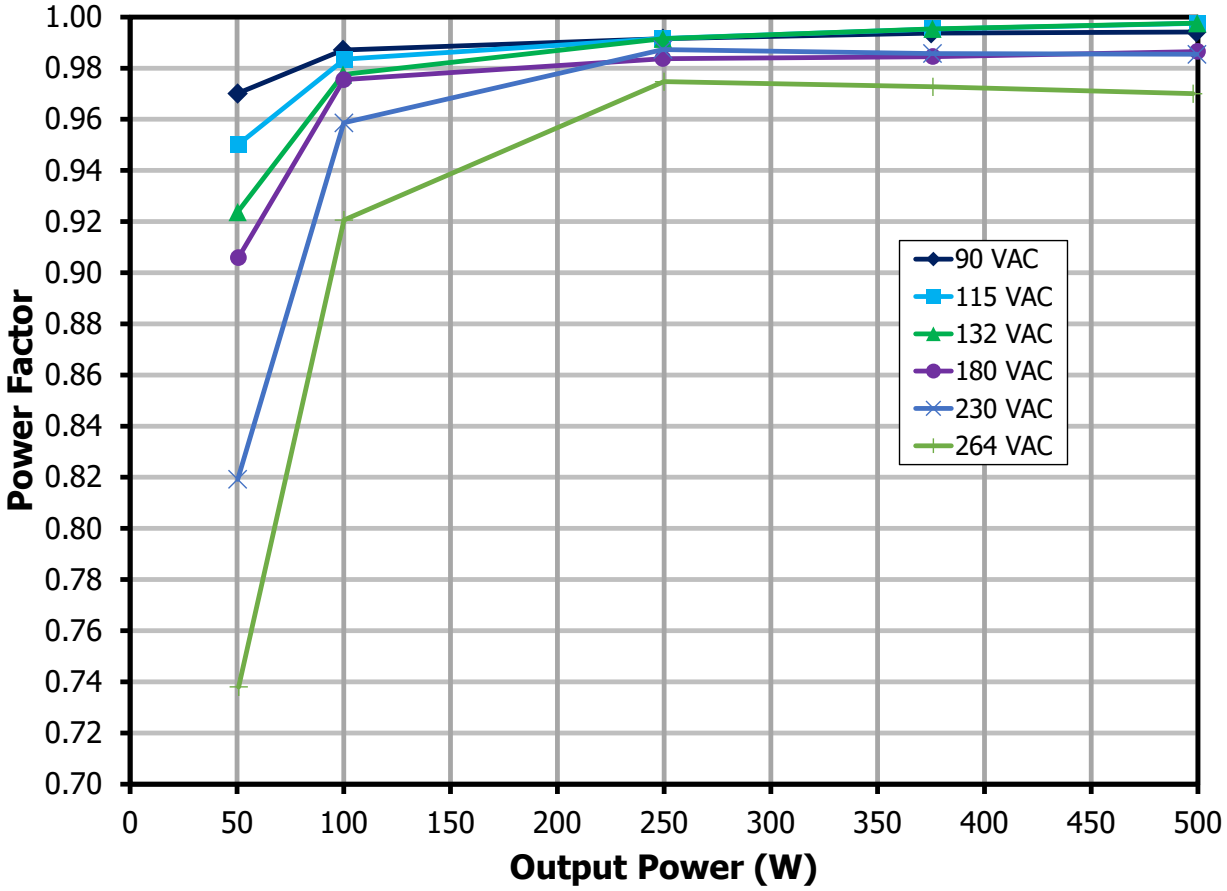


Figure 18 – Input Power Factor vs. Output Power.

12.4 *Regulation*

12.4.1 Load Regulation

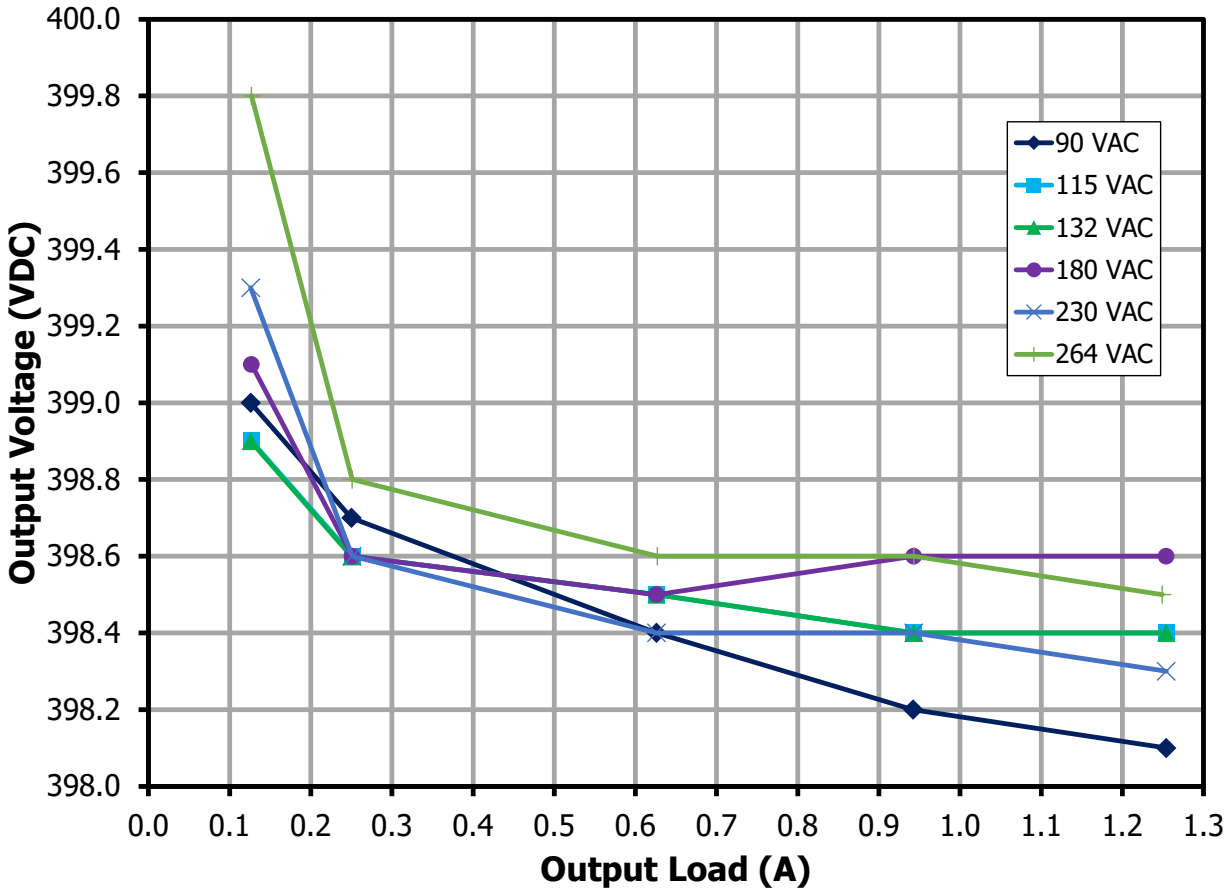


Figure 19 – Load Regulation

12.4.2 Line Regulation

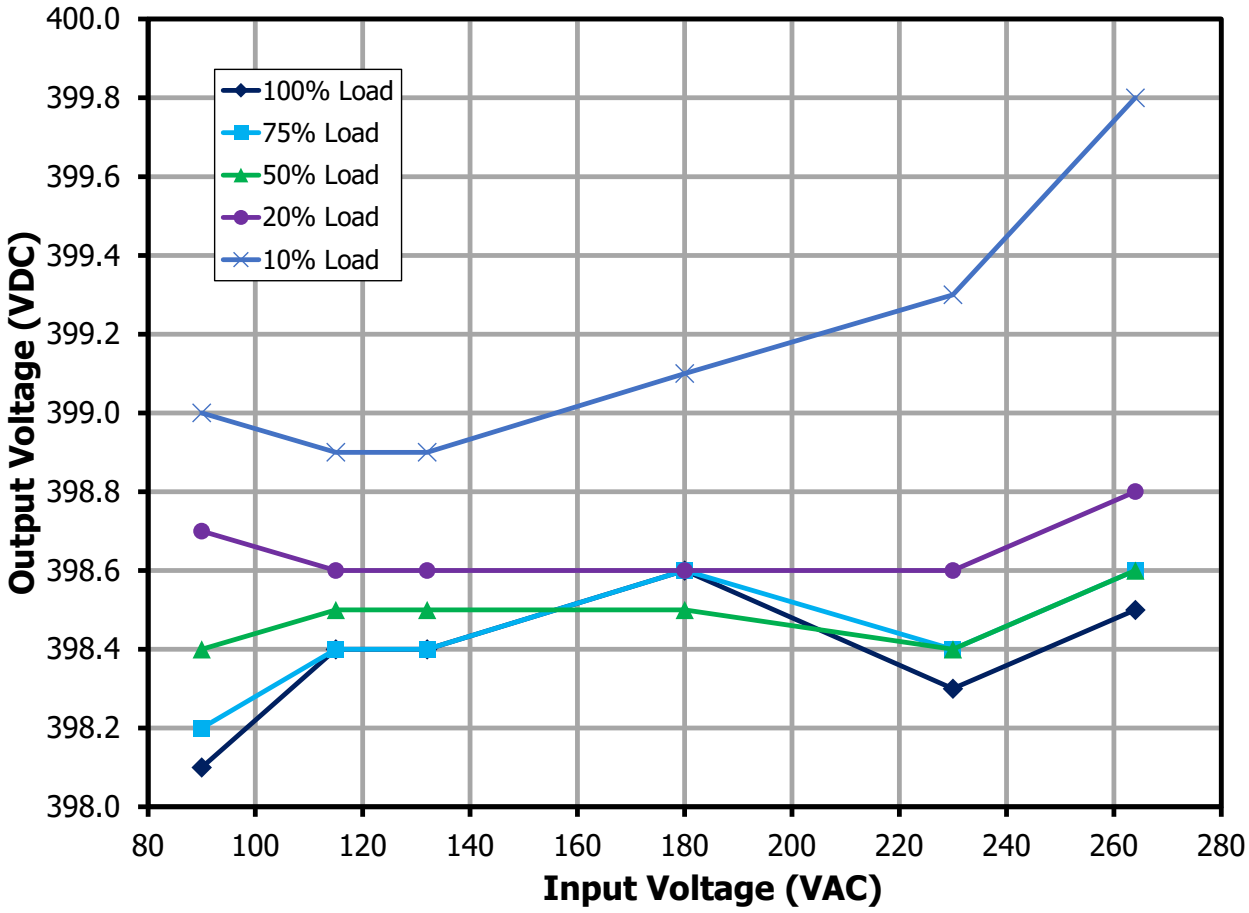


Figure 20 – Line Regulation.

12.5 *THD*

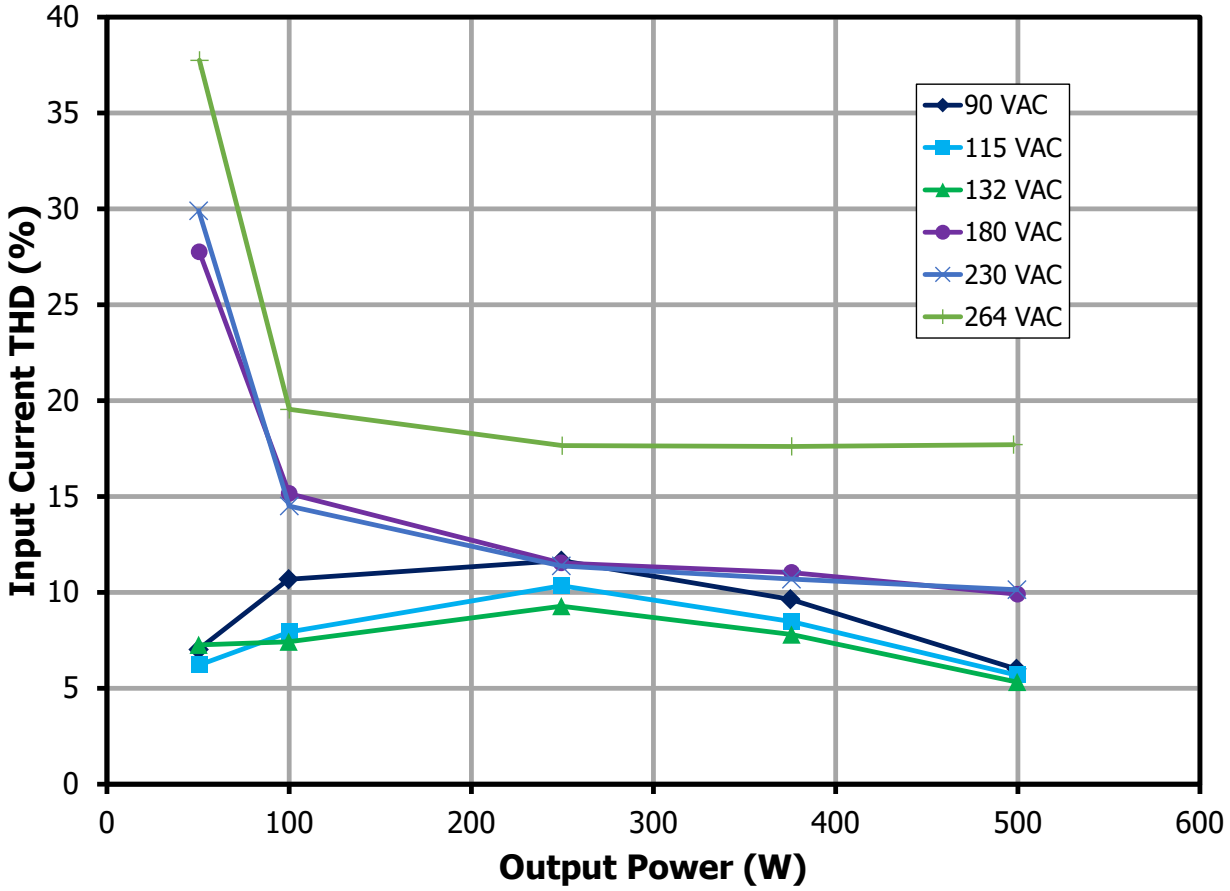


Figure 21 – Input Current THD vs. Load.

Note: When on highline (230 VAC and 264 VAC) and 10% load the unit is in burst mode, making the THD reading very high. To get an accurate reading the light load THD value should be integrated over several minutes.

12.6 *Input Current Harmonic Distortion (IEC 61000-3-2 Class-D)*

Measured at 115 and 230 VAC Input 60/50 Hz.

12.6.1 230 VAC 50 Hz, 100% Load at Output

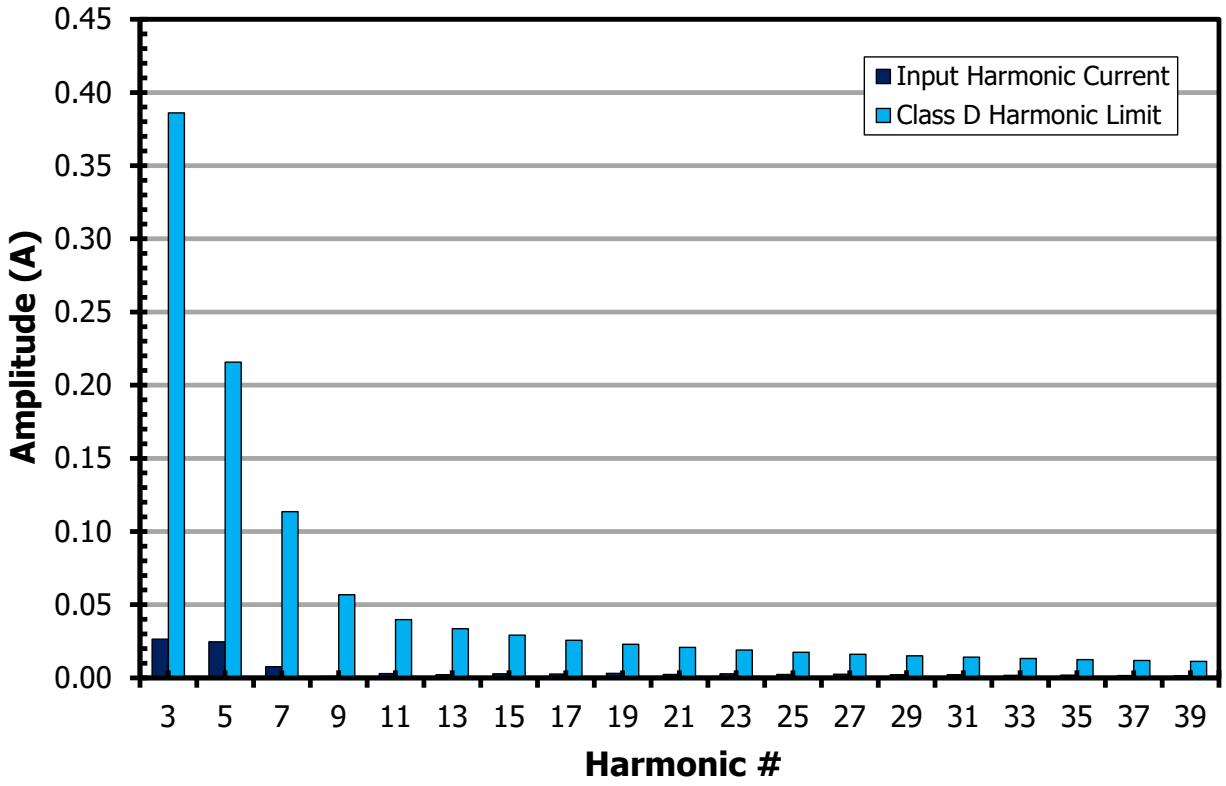


Figure 22 – Amplitude of Input Current Harmonics for 50% Load at 230 VAC Input.

12.6.2 230 VAC, 50 Hz, 50% Load at Output

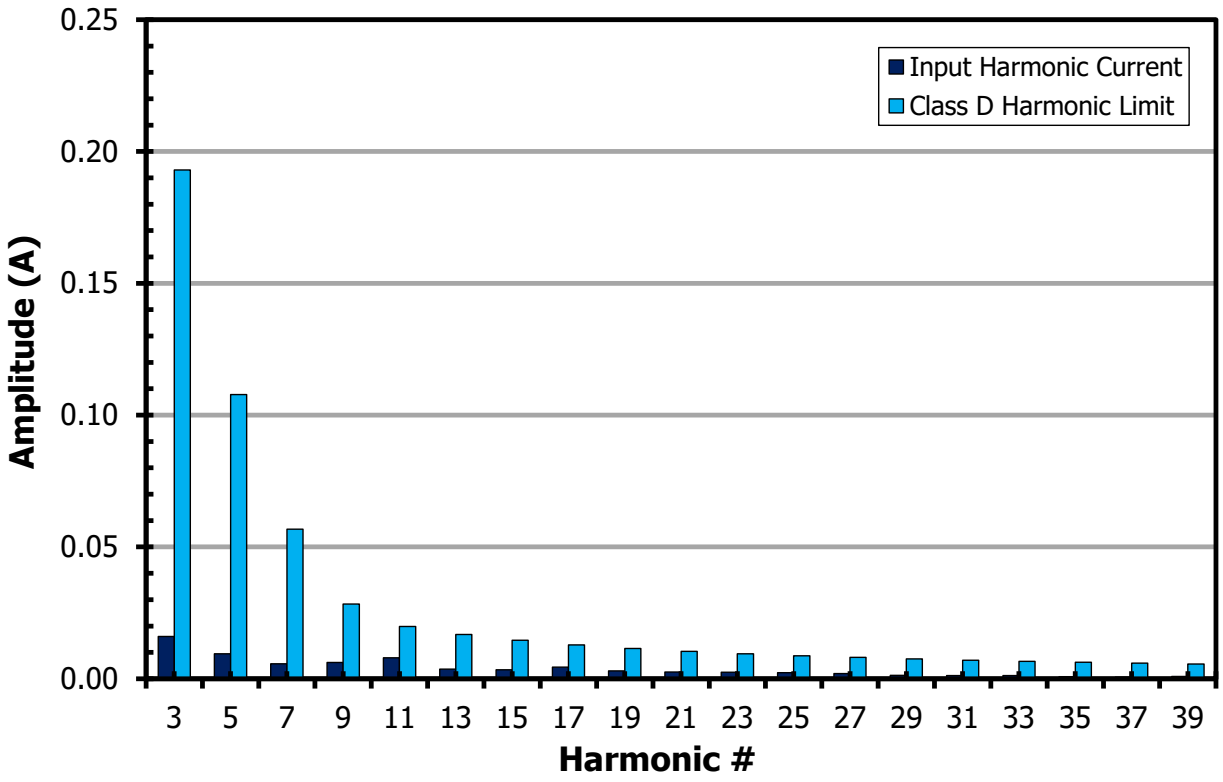


Figure 23 – Amplitude of Input Current Harmonics for 100% Load at 230 VAC Input.

12.6.3 115 VAC, 60 Hz, 100% Load at Output

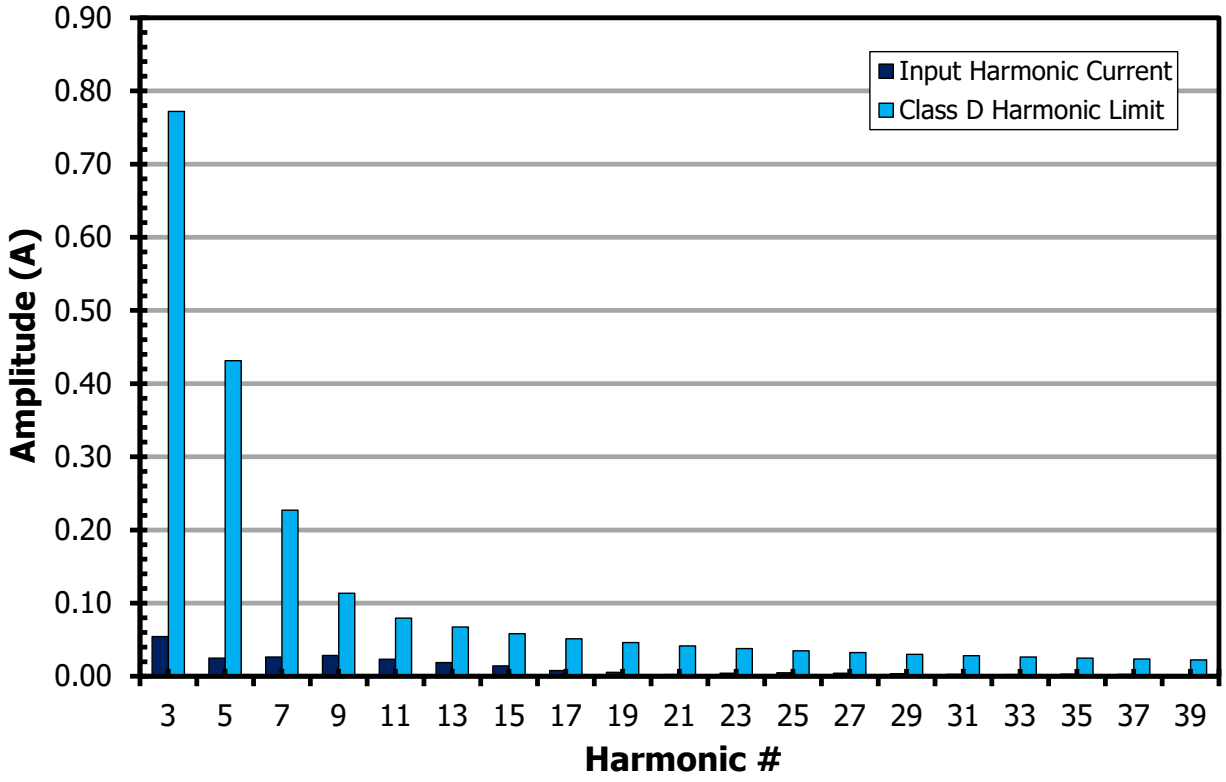


Figure 24 – Amplitude of Input Current Harmonics for 100% Load, 115 VAC, 60Hz.

12.6.4 115 VAC, 60 Hz, 50% Load at Output

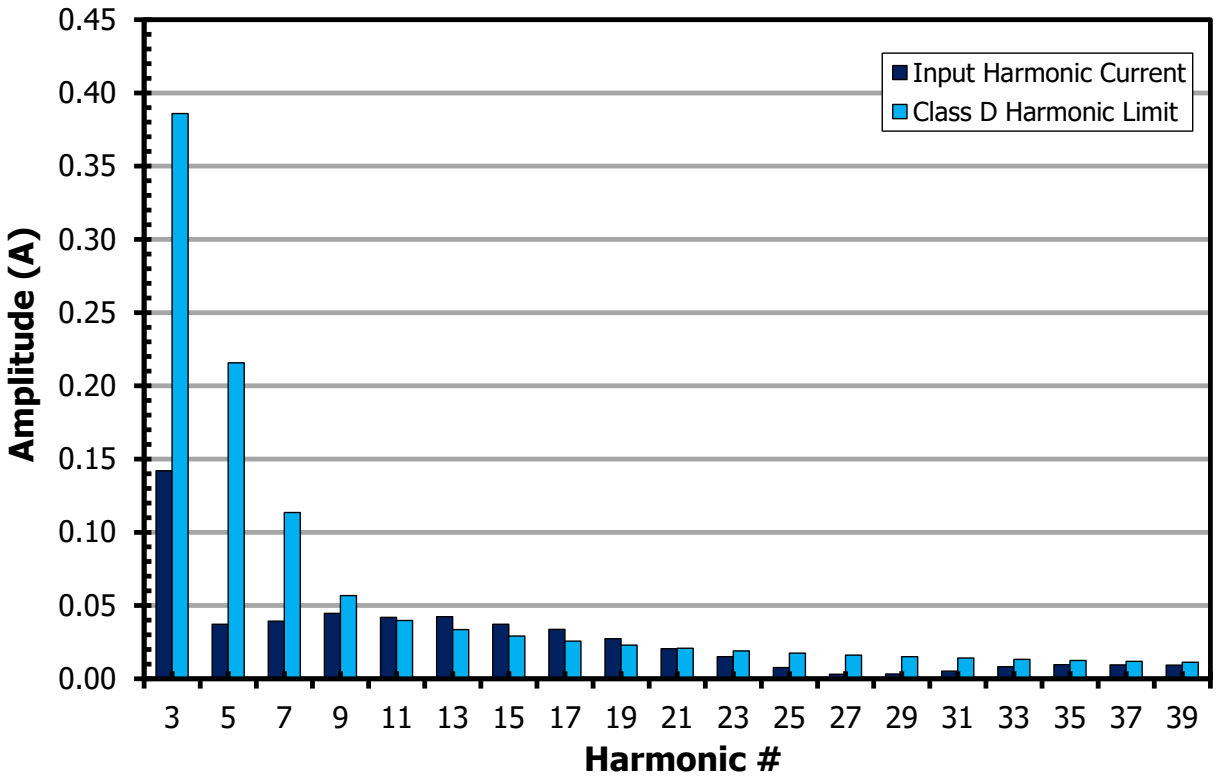


Figure 25 – Amplitude of Input Current Harmonics for 50% Load, 115 VAC, 60Hz

13 Thermal Performance

The unit was allowed to reach thermal equilibrium [~2 hrs.] inside a plastic box to suppress air cross-currents prior to thermal measurement with a FLIR camera. Table 1 shows full load temperature of key components measured at equilibrium, room temperature.

Temperature (ºC) 500 W Load			
Component		**115 VAC**	**230 VAC**
Ambient (measured by thermocouple)		24	25
CM Inductor	L4	71	49
DM Inductor	L3	51.4	39.3
Main Inductor 1	T1 Wire	75.4	56.5
	T1 Core	76.3	55.9
Main Inductor 2	T4 Wire	73	55.9
	T4 Core	70.9	53.9
Output Rectifier	D3	89.4	72.9
Output Rectifier	D4	91.3	73
Bridge Rectifier	BR1	92.5	68.4
Output Capacitor	C32	54	43
PFS5178F	U1	77.4	60.9
	U2	70.3	61.5

Table 1 – Steady-State Thermal Performance.

14 Input Waveforms

14.1 *Input Voltage/Current at 90 VAC, 60 Hz*

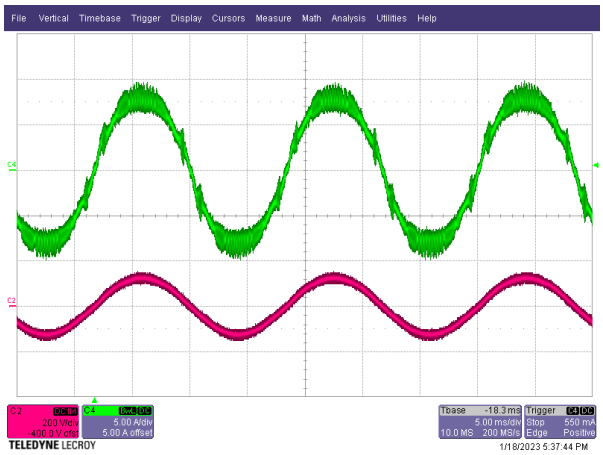


Figure 26 – 90 VAC, 100% Load.
Upper: I_{IN}, 5 A / div.
Lower: V_{IN}, 200 V, 5 ms / div.

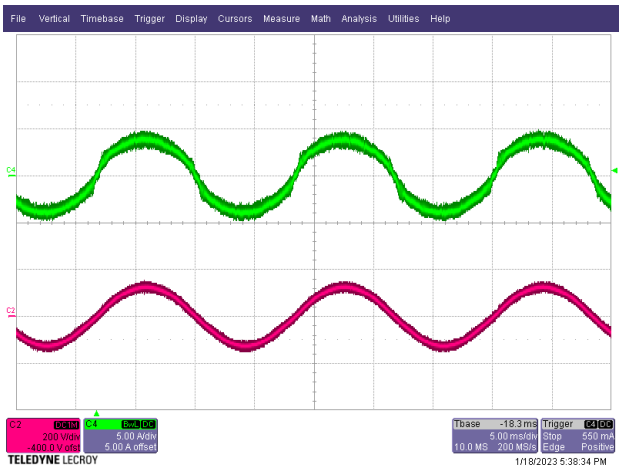


Figure 27 – 90 VAC, 50% Load.
Upper: I_{IN}, 5 A / div.
Lower: V_{IN}, 200 V, 5 ms / div..

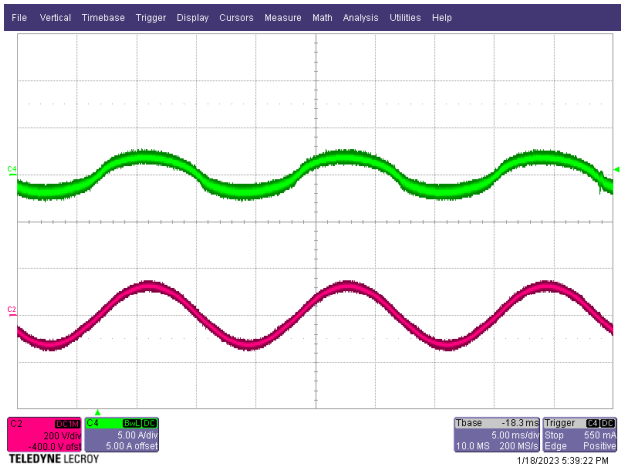


Figure 28 – 90 VAC, 25% Load.
Upper: I_{IN}, 5 A / div.
Lower: V_{IN}, 200 V, 5 ms / div.

14.2 *Input Voltage/Current at 115 VAC, 60 Hz*

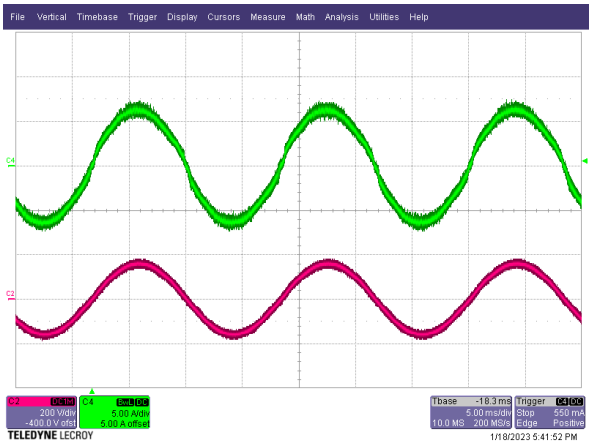


Figure 29 – 115 VAC, 100% Load.
Upper: I_{IN}, 5 A / div.
Lower: V_{IN}, 200 V, 5 ms / div.

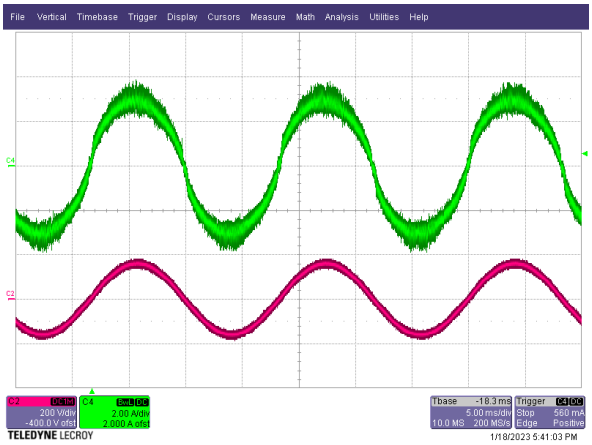


Figure 30 – 115 VAC, 50% Load.
Upper: I_{IN}, 2 A / div.
Lower: V_{IN}, 200 V, 5 ms / div.

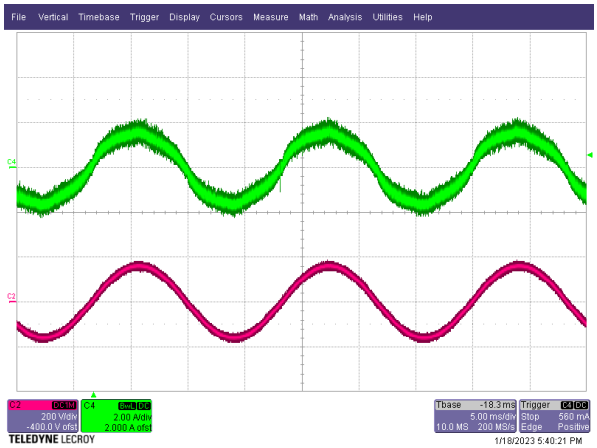


Figure 31 – 115 VAC, 25% Load.
Upper: I_{IN}, 2 A / div.
Lower: V_{IN}, 200 V, 5 ms / div.

14.3 *Input Voltage/Current, 230 VAC, 50 Hz*

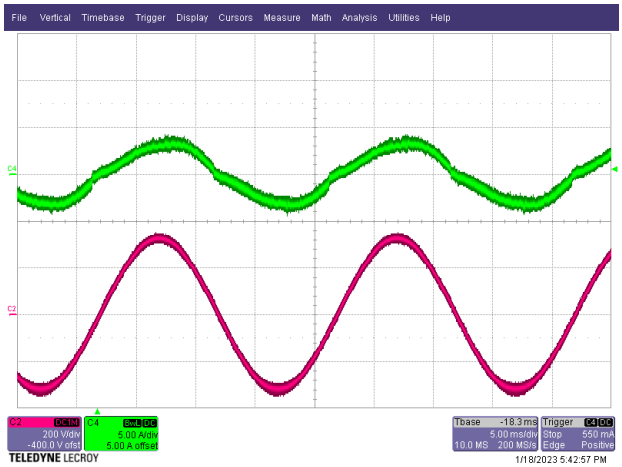


Figure 32 – 230 VAC, 100% Load.
Upper: I_{IN}, 5 A / div.
Lower: V_{IN}, 200 V, 5 ms / div.

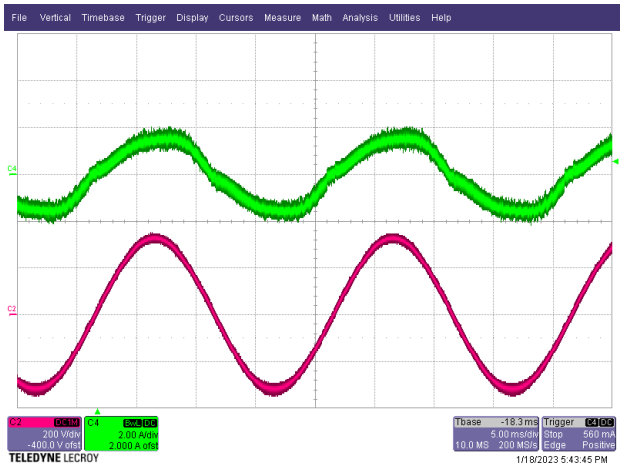


Figure 33 – 230 VAC, 50% Load.
Upper: I_{IN}, 2 A / div.
Lower: V_{IN}, 200 V, 5 ms / div.

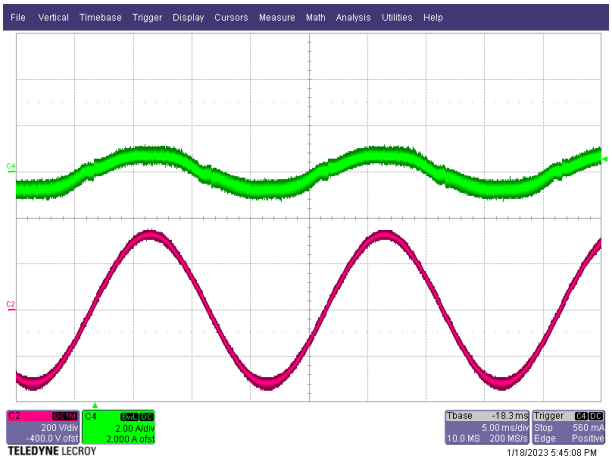


Figure 34 – 230 VAC, 25% Load.
Upper: I_{IN}, 2 A / div.
Lower: V_{IN}, 200 V, 5 ms / div.

14.4 *Input Voltage/Current Waveforms, 264 VAC, 50 Hz*

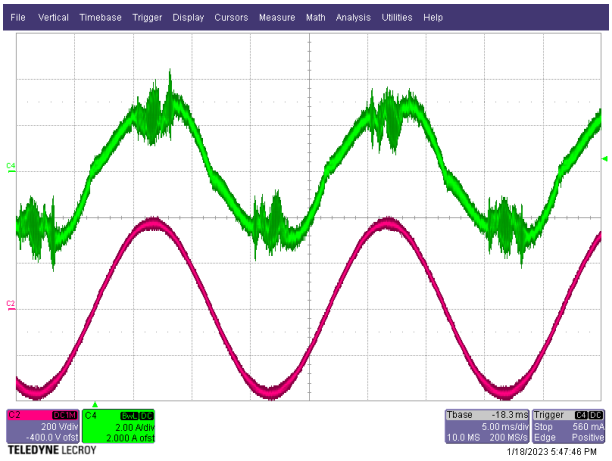


Figure 35 – 264 VAC, 100% Load.
Upper: I_{IN}, 2 A / div.
Lower: V_{IN}, 200 V, 5 ms / div.

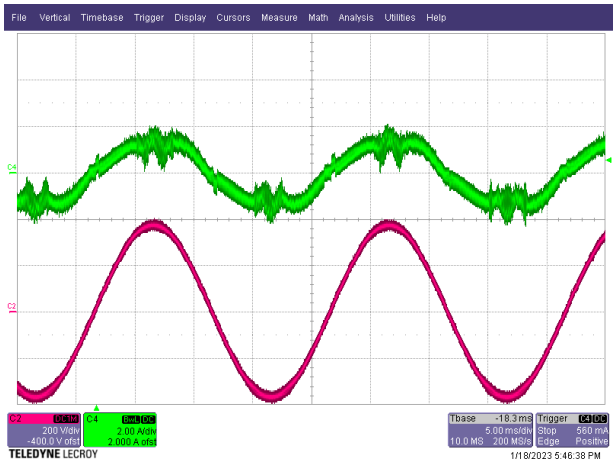


Figure 36 – 264 VAC, 50% Load.
Upper: I_{IN}, 2 A / div.
Lower: V_{IN}, 200 V, 5 ms / div.

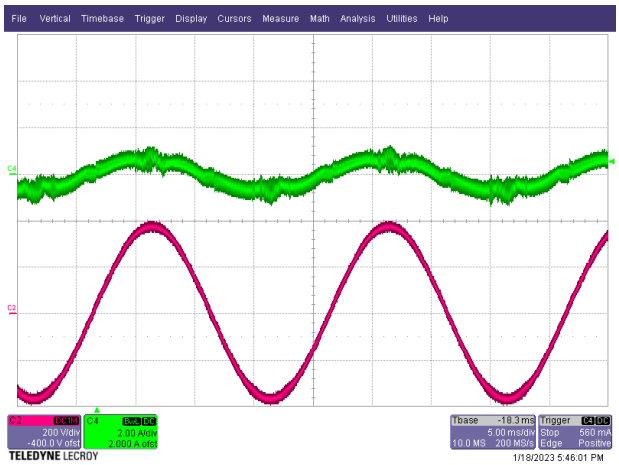


Figure 37 – 264 VAC, 25% Load.
Upper: I_{IN}, 2 A / div.
Lower: V_{IN}, 200 V, 5 ms / div.

14.4.1 Start-up Waveforms

14.4.2 90 VAC, 60 Hz

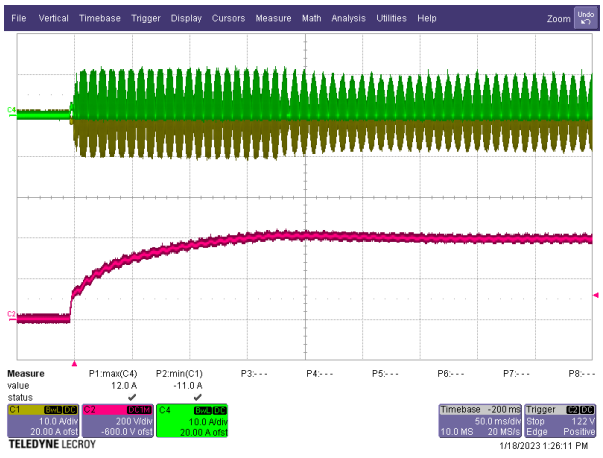


Figure 38 – 90 VAC, 100% Load.
Grn: T4 Inductor Current, 10 A / div.
Yel: T1 Inductor Current, 10 A / div.
Red: V_{OUT}, 200 V, 50 ms/ div.
Lower: I_{IN}, 5 A / div., 50 ms / div.

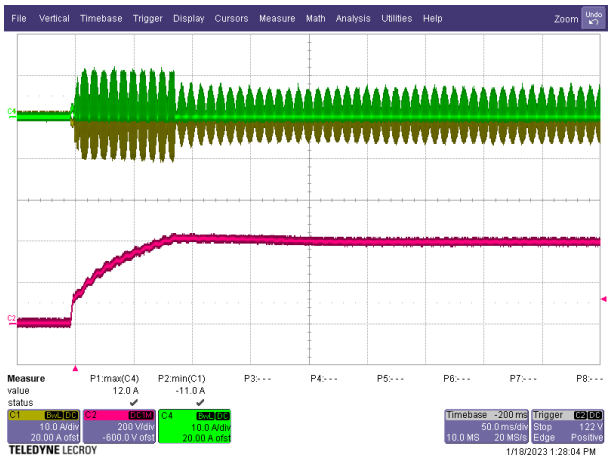


Figure 39 – 90 VAC, 50% Load.
Grn: T4 Inductor Current, 10 A / div.
Yel: T1 Inductor Current, 10 A / div.
Red: V_{OUT}, 200 V, 50 ms/ div.
Lower: I_{IN}, 5 A / div., 50 ms / div.

Figure 40 – 90 VAC, 25% Load.
Grn: T4 Inductor Current, 10 A / div.
Yel: T1 Inductor Current, 10 A / div.
Red: V_{OUT}, 200 V, 50 ms / div.

14.4.3 115 VAC, 60 Hz

Figure 41 – 115 VAC, 100% Load.
Grn: T4 Inductor Current, 10 A / div.
Yel: T1 Inductor Current, 10 A / div.
Red: V_{OUT}, 200 V, 50 ms/ div.

Figure 42 – 115 VAC, 50% Load.
Grn: T4 Inductor Current, 10 A / div.
Yel: T1 Inductor Current, 10 A / div.
Red: V_{OUT}, 200 V, 50 ms/ div.

Figure 43 – 115 VAC, 25% Load.
Grn: T4 Inductor Current, 10 A / div.
Yel: T1 Inductor Current, 10 A / div.
Red: V_{OUT}, 200 V, 50 ms/ div.

14.4.4 230V, 50 Hz

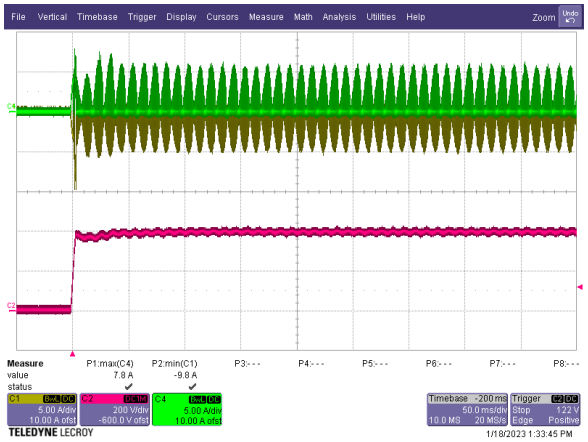


Figure 44 – 230 VAC, 100% Load.
Grn: T4 Inductor Current, 10 A / div.
Yel: T1 Inductor Current, 10 A / div.
Red: V_{OUT}, 200 V, 50 ms/ div.

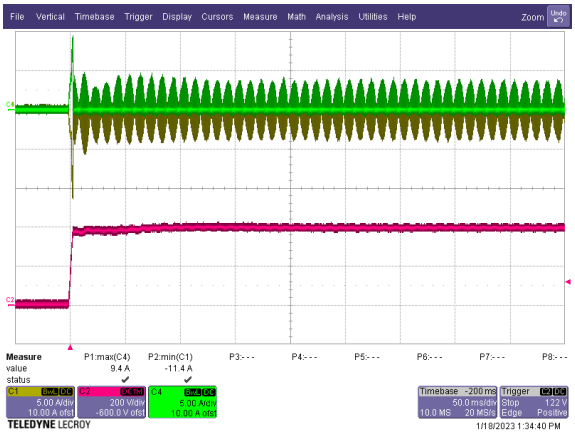


Figure 45 – 230 VAC, 50% Load.
Grn: T4 Inductor Current, 10 A / div.
Yel: T1 Inductor Current, 10 A / div.
Red: V_{OUT}, 200 V, 50 ms/ div.

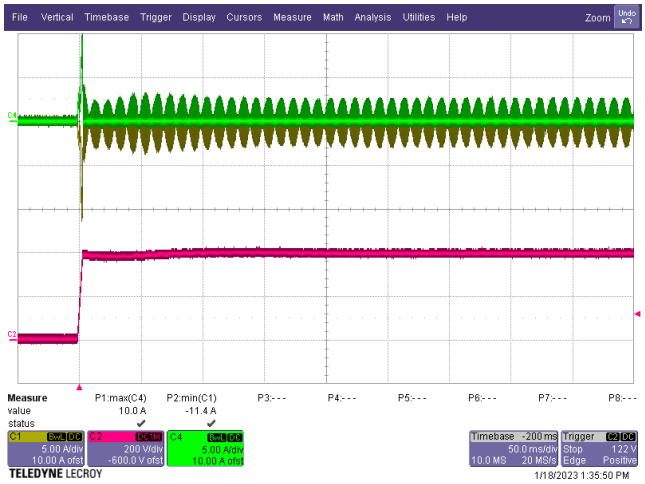


Figure 46 – 230 VAC, 25% Load.
Grn: T4 Inductor Current, 10 A / div.
Yel: T1 Inductor Current, 10 A / div.
Red: V_{OUT}, 200 V, 50 ms/ div.

14.4.5 264 VAC, 50 Hz

Figure 47 – 264 VAC**,** 100% Load.
Grn: T4 Inductor Current, 10 A / div.
Yel: T1 Inductor Current, 10 A / div.
Red: V_{OUT}, 200 V, 50 ms/ div.

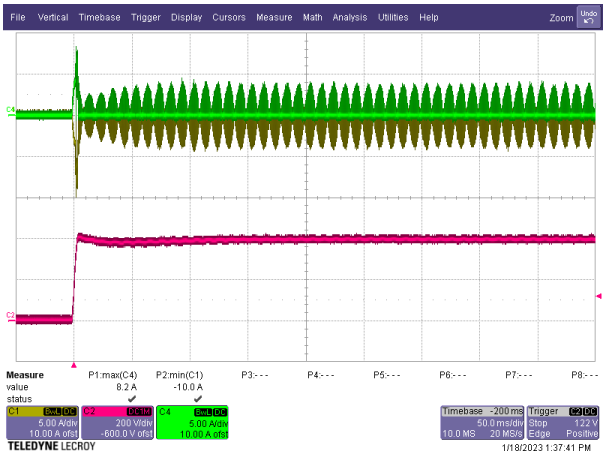


Figure 48 – 264 VAC, 50% Load.
Grn: T4 Inductor Current, 10 A / div.
Yel: T1 Inductor Current, 10 A / div.
Red: V_{OUT}, 200 V, 50 ms/ div.

Figure 49 – 264 VAC, 25% Load.
Grn: T4 Inductor Current, 10 A / div.
Yel: T1 Inductor Current, 10 A / div.
Red: V_{OUT}, 200 V, 50 ms/ div.

14.5 *Load Transient Response*

14.5.1 90 VAC, 60 Hz

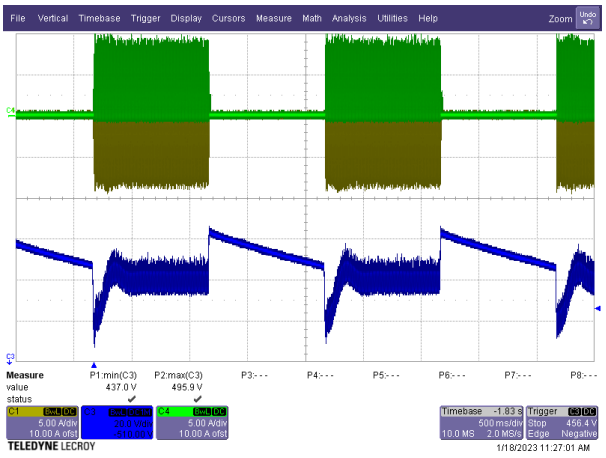


Figure 50 – Transient Response, 90 VAC, 0-100-0% Load Step.
Grn: T1 Inductor Current, 5 A / div.
Yel: T4 Inductor Current, 5 A / div.
Blu: V_{OUT} (DC Coupled), 20 V, 500 ms / div.

Figure 51 – Transient Response, 90 VAC, 10-100-10% Load Step.
Grn: T1 Inductor Current, 5 A / div.
Yel: T4 Inductor Current, 5 A / div.
Blu: V_{OUT} (DC Coupled), 20 V, 500 ms / div.

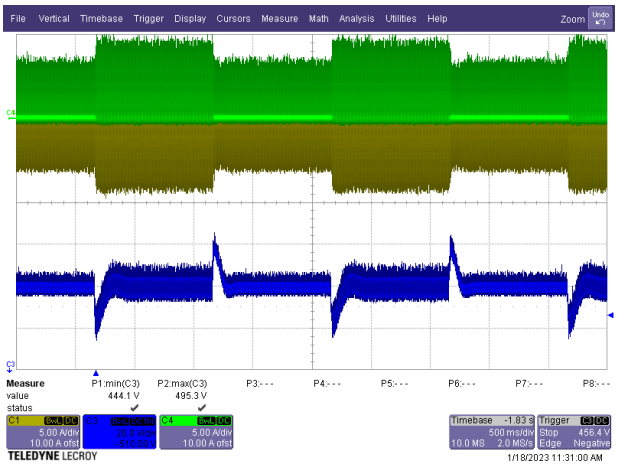


Figure 52 – Transient Response, 90 VAC, 50-100-50% Load Step.
Grn: T1 Inductor Current, 5 A / div.
Yel: T4 Inductor Current, 5 A / div.
Blu: V_{OUT} (DC Coupled), 20 V, 500 ms / div.

14.5.2 115 VAC, 60 Hz

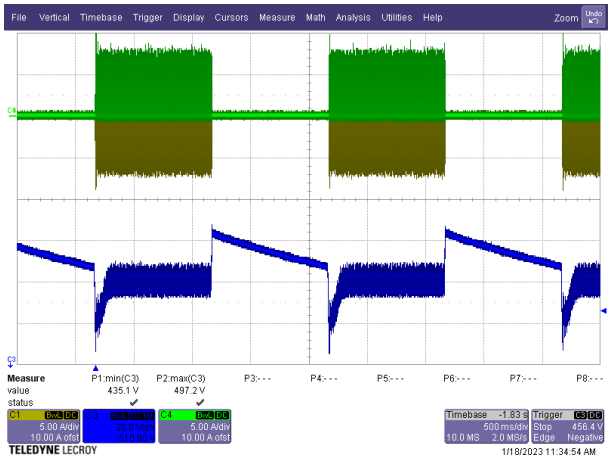


Figure 53 – Transient Response, 115 VAC, 0-100-0% Load Step.
Grn: T1 Inductor Current, 5 A / div.
Yel: T4 Inductor Current, 5 A / div.
Blu: V_{OUT} (DC Coupled), 20 V, 500 ms / div.

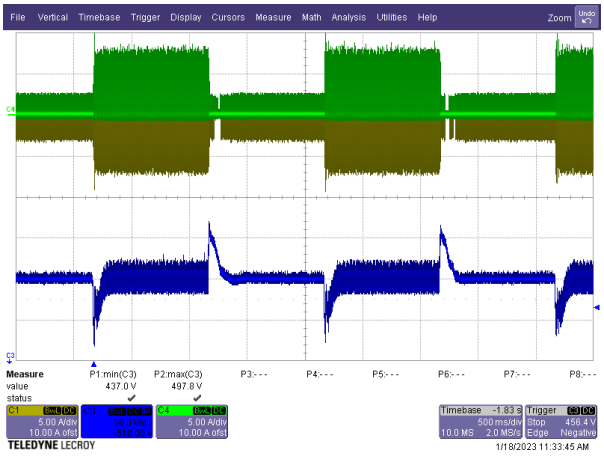


Figure 54 – Transient Response, 115 VAC, 10-100-10% Load Step.
Grn: T1 Inductor Current, 5 A / div.
Yel: T4 Inductor Current, 5 A / div.
Blu: V_{OUT} (DC Coupled), 20 V, 500 ms / div.

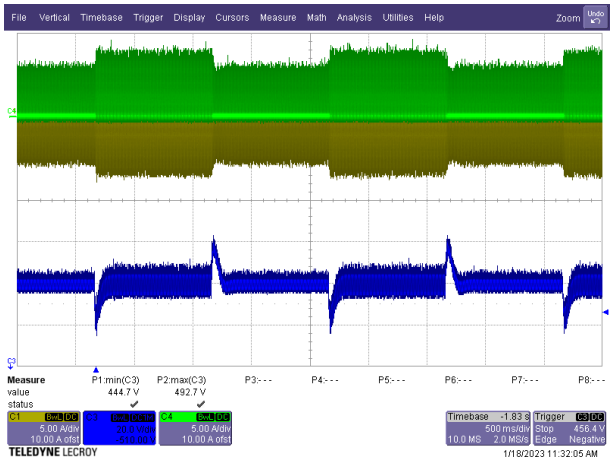


Figure 55 – Transient Response, 115 VAC, 50-100-0% Load Step.
Grn: T1 Inductor Current, 5 A / div.
Yel: T4 Inductor Current, 5 A / div.
Blu: V_{OUT} (DC Coupled), 20 V, 500 ms / div.

14.5.3 230 VAC, 50 Hz

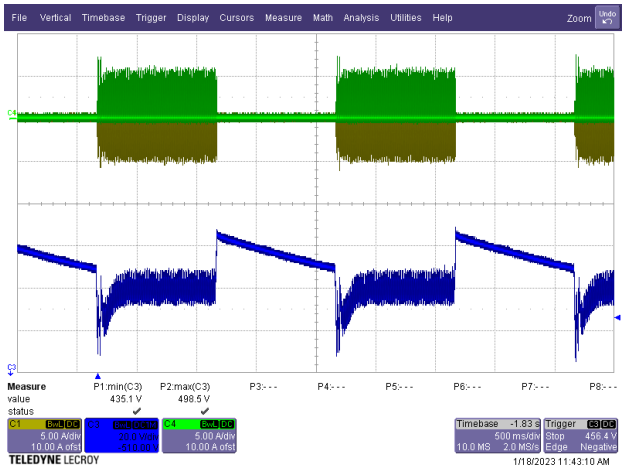


Figure 56 – Transient Response, 230 VAC, 0-100-0% Load Step.
Grn: T1 Inductor Current, 5 A / div.
Yel: T4 Inductor Current, 5 A / div.
Blu: V_{OUT} (DC Coupled), 20 V, 500 ms / div.

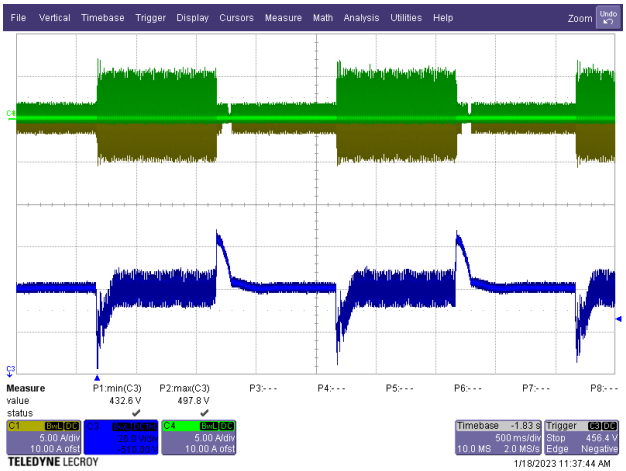


Figure 57 – Transient Response, 230 VAC, 10-100-10% Load Step.
Grn: T1 Inductor Current, 5 A / div.
Yel: T4 Inductor Current, 5 A / div.
Blu: V_{OUT} (DC Coupled), 20 V, 500 ms / div.

Figure 58 – Transient Response, 230 VAC, 50-100-0% Load Step.
Grn: T1 Inductor Current, 5 A / div.
Yel: T4 Inductor Current, 5 A / div.
Blu: V_{OUT} (DC Coupled), 20 V, 500 ms / div.

14.5.4 264 VAC, 50 Hz

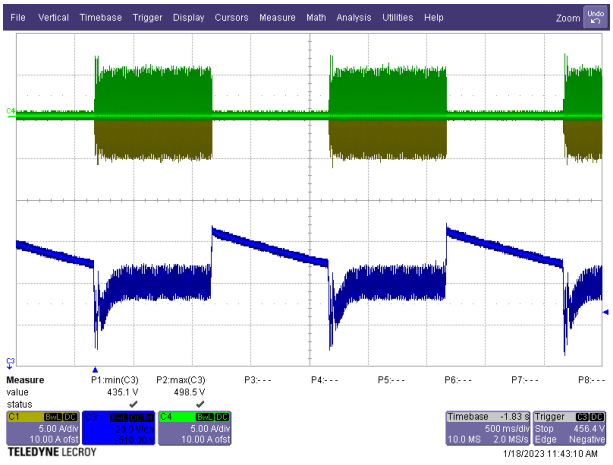


Figure 59 – Transient Response, 264 VAC, 0-100-0% Load Step.
Grn: T1 Inductor Current, 5 A / div.
Yel: T4 Inductor Current, 5 A / div.
Blu: V_{OUT} (DC Coupled), 20 V, 500 ms / div.

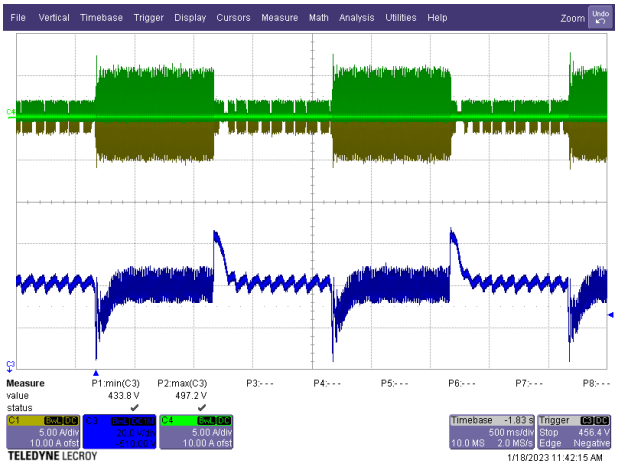


Figure 60 – Transient Response, 264 VAC, 10-100-10% Load Step.
Grn: T1 Inductor Current, 5 A / div.
Yel: T4 Inductor Current, 5 A / div.
Blu: V_{OUT} (DC Coupled), 20 V, 500 ms / div.

Figure 61 – Transient Response, 264 VAC, 50-100-0% Load Step.
Grn: T1 Inductor Current, 5 A / div.
Yel: T4 Inductor Current, 5 A / div.
Blu: V_{OUT} (DC Coupled), 20 V, 500 ms / div.

14.6 *Line Dropout*

14.6.1 1000 ms Line Dropout (115 VAC / 60 Hz and 230 VAC / 50 Hz)

14.6.1.1 50% Load at Output

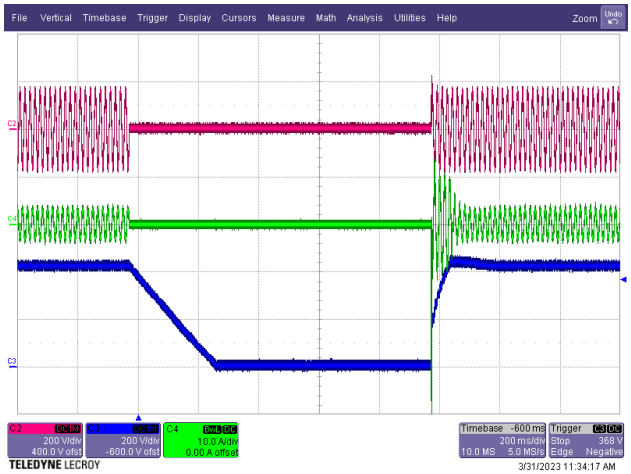


Figure 62 – Line Dropout 115 VAC, 1000 ms.
Upper: V_{IN}, 200 V / div.
Middle: I_{IN}, 10 A / div.
Lower: V_{OUT}, 200 V / div., 200 ms / div.

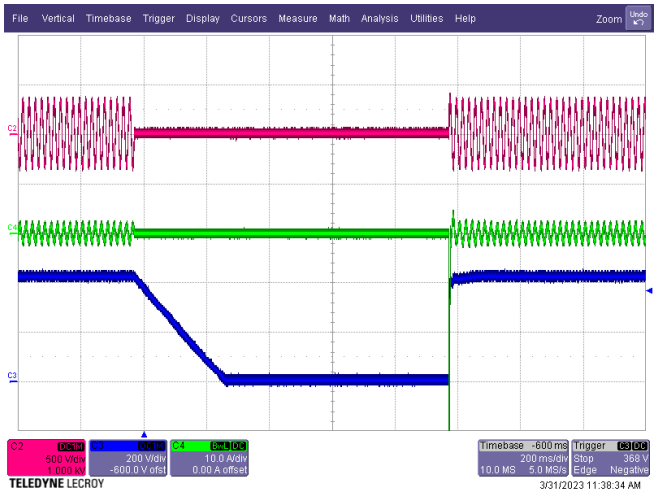


Figure 63 – Line Dropout 230 VAC, 1000 ms.
Upper: V_{IN}, 500 V / div.
Middle: I_{IN}, 10 A / div.
Lower: V_{OUT}, 200 V / div., 200 ms / div.

14.6.1.2 Full Load at Output

Figure 64 – Line Dropout 115 VAC, 1000 ms.
Upper: V_{IN}, 200 V / div.
Middle: I_{IN}, 10 A / div.
Lower: V_{OUT}, 200 V / div., 200 ms / div.

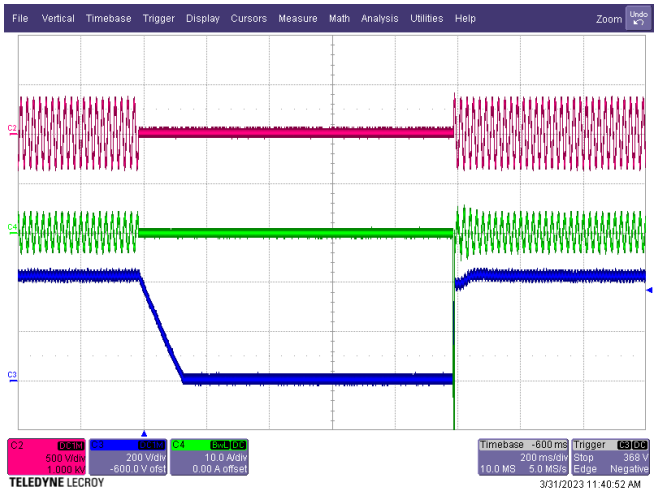


Figure 65 – Line Dropout 230 VAC, 1000 ms.
Upper: V_{IN}, 500 V / div.
Middle: I_{IN}, 10 A / div.
Lower: V_{OUT}, 200 V / div., 200 ms / div.

14.6.2 One Cycle Line Dropout (115 VAC / 60 Hz and 230 VAC / 50 Hz)

14.6.2.1 Full Load at Output

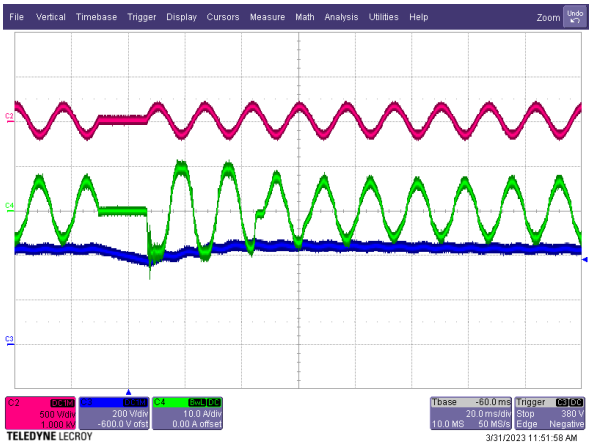


Figure 66 – Line Dropout 115 VAC, 60 Hz.
Upper: V_{IN}, 500 V / div.
Middle: I_{IN}, 10 A /div.
Lower: V_{OUT}, 200 V / div., 20 ms / div.

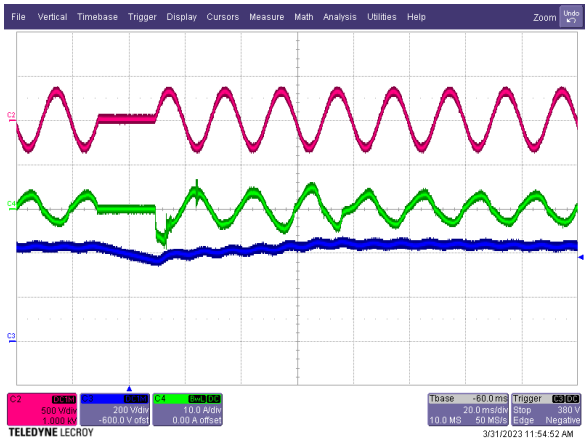


Figure 67 – Line Dropout 230 VAC, 50 Hz.
Upper: V_{IN}, 500 V / div.
Middle: I_{IN}, 10 A /div.
Lower: V_{OUT}, 200 V / div., 20 ms /div

14.7 *Input Line Step*

14.7.1 Line Sag (85 VAC ~ 115 VAC ~ 85 VAC, 60 Hz)

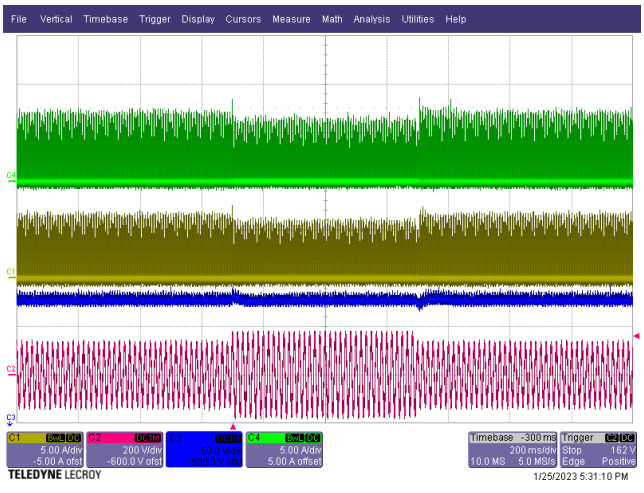


Figure 68 – Line Sag 85-115-85 VAC, 50% Load.
Grn: IT4, 5 A / div.
Yel: IT1, 5 A / div.
Blu: V_{OUT} (DC Coupled), 50 V / div.
Red: V_{IN}, 200 V, 200 ms / div.

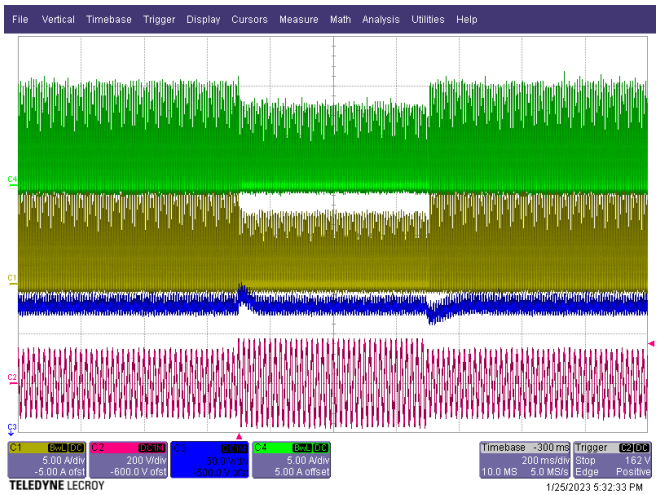


Figure 69 – Line Sag 85-115-85 VAC, 100% Load.
Grn: IT4, 5 A / div.
Yel: IT1, 5 A / div.
Blu: V_{OUT} (DC Coupled), 50 V / div.
Red: V_{IN}, 200 V, 200 ms / div.

14.7.2 Line Swell (147 VAC ~ 132 VAC ~ 147 VAC, 60 Hz)

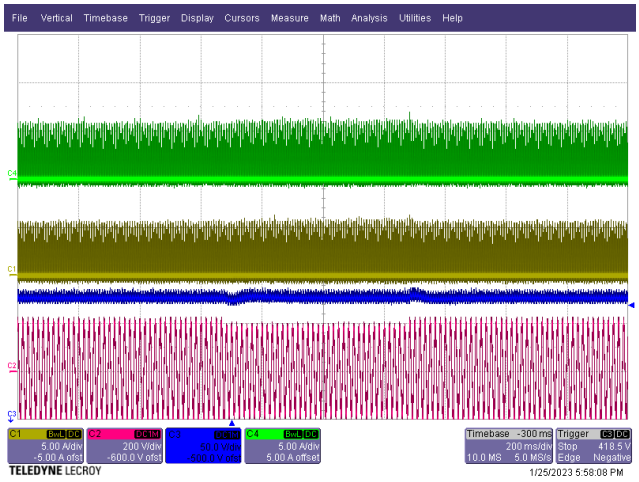


Figure 70 – Line Surge 132 VAC, 50% Load.
Grn: I_{T4}, 5 A / div.
Yel: I_{T1}, 5 A / div.
Blu: V_{OUT} (DC Coupled), 50 V / div., 50
Red: V_{in}, 200V, 200 ms / div.

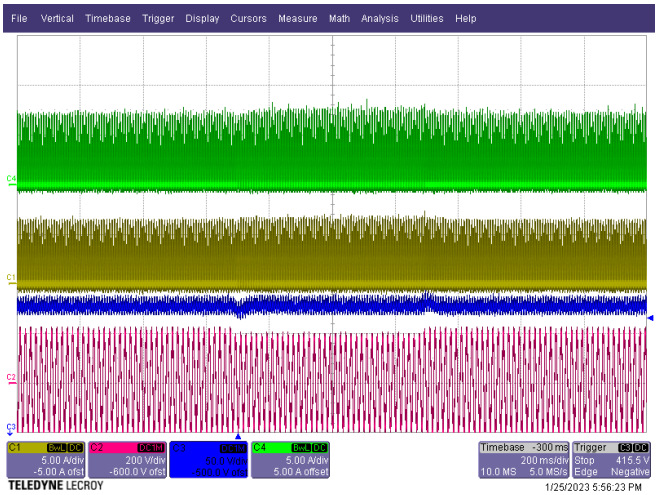


Figure 71 – Line Surge 132 VAC, 100% Load.
Upper: V_{IN}, 200 V / div.
Middle: I_{IN}, 5 A / div.
Lower: V_{OUT} (DC Coupled), 20 V / div., 50
Red: V_{in}, 200 V, 200 ms / div.

14.7.3 Line Sag (170 VAC ~ 230 VAC ~ 170 VAC, 50 Hz)

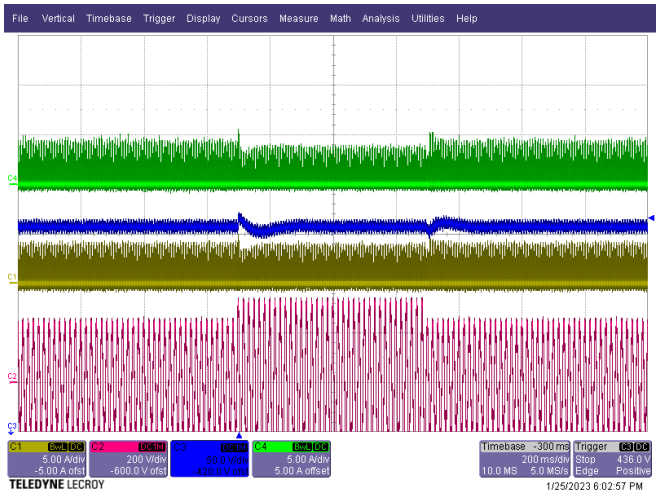


Figure 72 – Line Sag 230 VAC, 50% Load.
Grn: I_{T4}, 5 A / div.
Yel: I_{T1}, 5 A / div.
Blu: V_{OUT} (DC Coupled), 50 V / div.,
Red: V_{in}, 200 V, 200 ms / div.

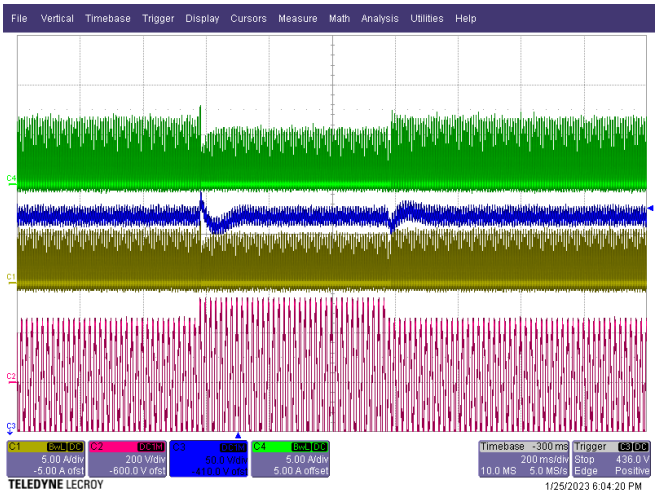


Figure 73 – Line Sag 230 VAC, 100% Load.
Grn: I_{T4}, 5 A / div.
Yel: I_{T1}, 5 A / div.
Blu: V_{OUT} (DC Coupled), 50 V / div.
Red: V_{in}, 200V, 200 ms / div.

14.7.4 Line Swell (293 VAC ~ 264 VAC ~ 293 VAC, 50 Hz)

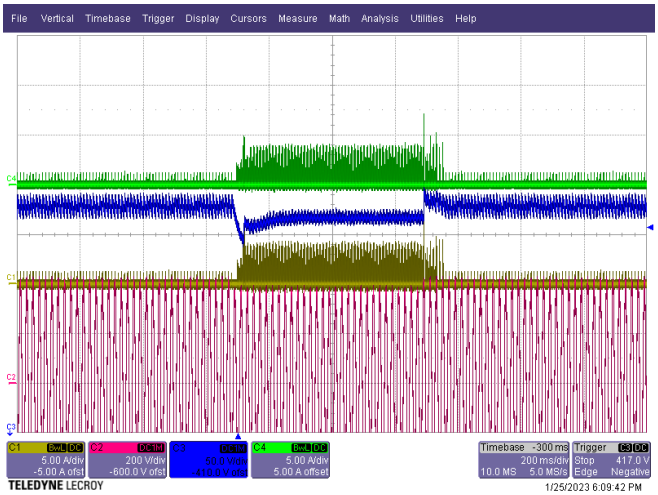


Figure 74 – Line Surge 264 VAC, 50% Load.
Grn: I_{T4}, 5 A / div.
Yel: I_{T1}, 5 A / div.
Blu: V_{OUT} (DC Coupled), 50 V / div.
Red: V_{in}, 200V, 200 ms / div.

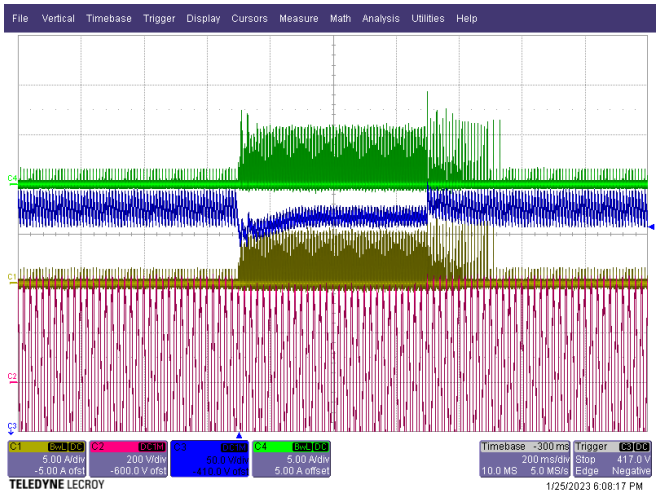


Figure 75 – Line Surge 264 VAC, 100% Load.
Grn: I_{T4}, 5 A / div.
Yel: I_{T1}, 5 A / div.
Blu: V_{OUT} (DC Coupled), 50 V / div.
Red: V_{in}, 200 V, 200 ms / div.

14.8 *Power Good (PG)*

Power Good (PG) waveforms were measured at start-up and shutdown with the PG pull-up resistor (TP-8) tied to V_{REF}.

14.8.1 115 VAC and 60 Hz

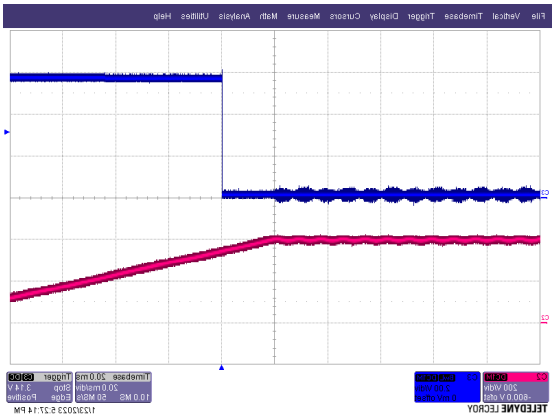


Figure 76 – 115 VAC, Full Load, V_{OUT} Rising Edge.
Blue: PG 2 V / div.
Red: V_{OUT}, 200 V, 20 ms / div.

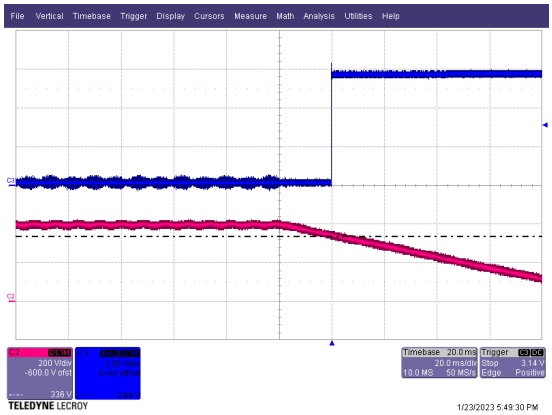


Figure 77 – 115 VAC, Full Load, V_{OUT} Falling Edge.
Blu: PG, 2 V / div.
Red: V_{OUT}, 200 V, 20 ms / div.

14.8.2 230 VAC and 50 Hz

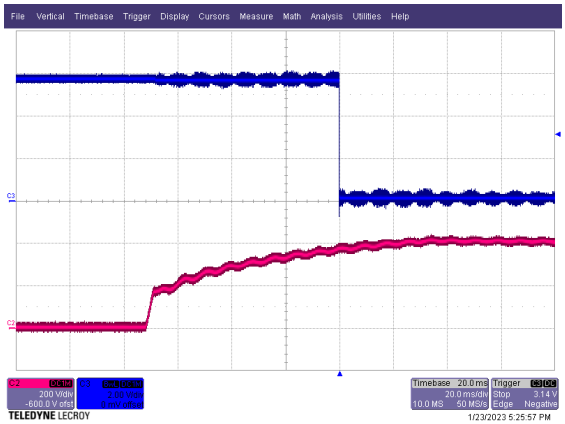


Figure 78 – 230 VAC, 100% Load, Vout Rising Edge.
Blu: PG, 2 V / div.
Red: V_{OUT}, 200 V, 20 ms / div.

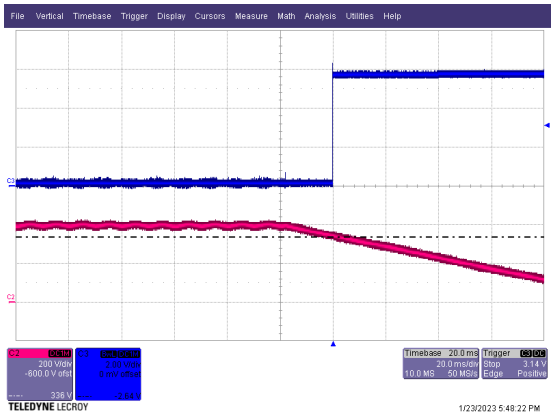


Figure 79 – 230 VAC, 100% Load, Vout Falling Edge.
Blu: PG, 2 V / div.
Red: V_{OUT}, 200 V, 20 ms / div.

Note: For Figures 56 and 58, input AC voltage was turned off to verify PG transition threshold. Trip point in each case was 336 VDC

14.9 *Brown-In and Brown-Out at 6 V / Minute Rate*

Test conducted by first reducing, followed by increasing input AC voltage source at a rate of 6 V / min. The PFC converter DC output was loaded to 100% of rated load (electronic load), which was programmed to release the load when the DC output of the PFC dropped below 310 V [at brown-out]. After the load switches off it continues to draw about 1.5mA and discharges the output capacitor of the PFC after the dynamic load is released at brown-out.

14.9.1 Thresholds

Measured PFC Brown-Out Threshold	71.28 VAC
Measured PFC Brown-In Threshold	75.69 VAC

14.9.2 Waveforms

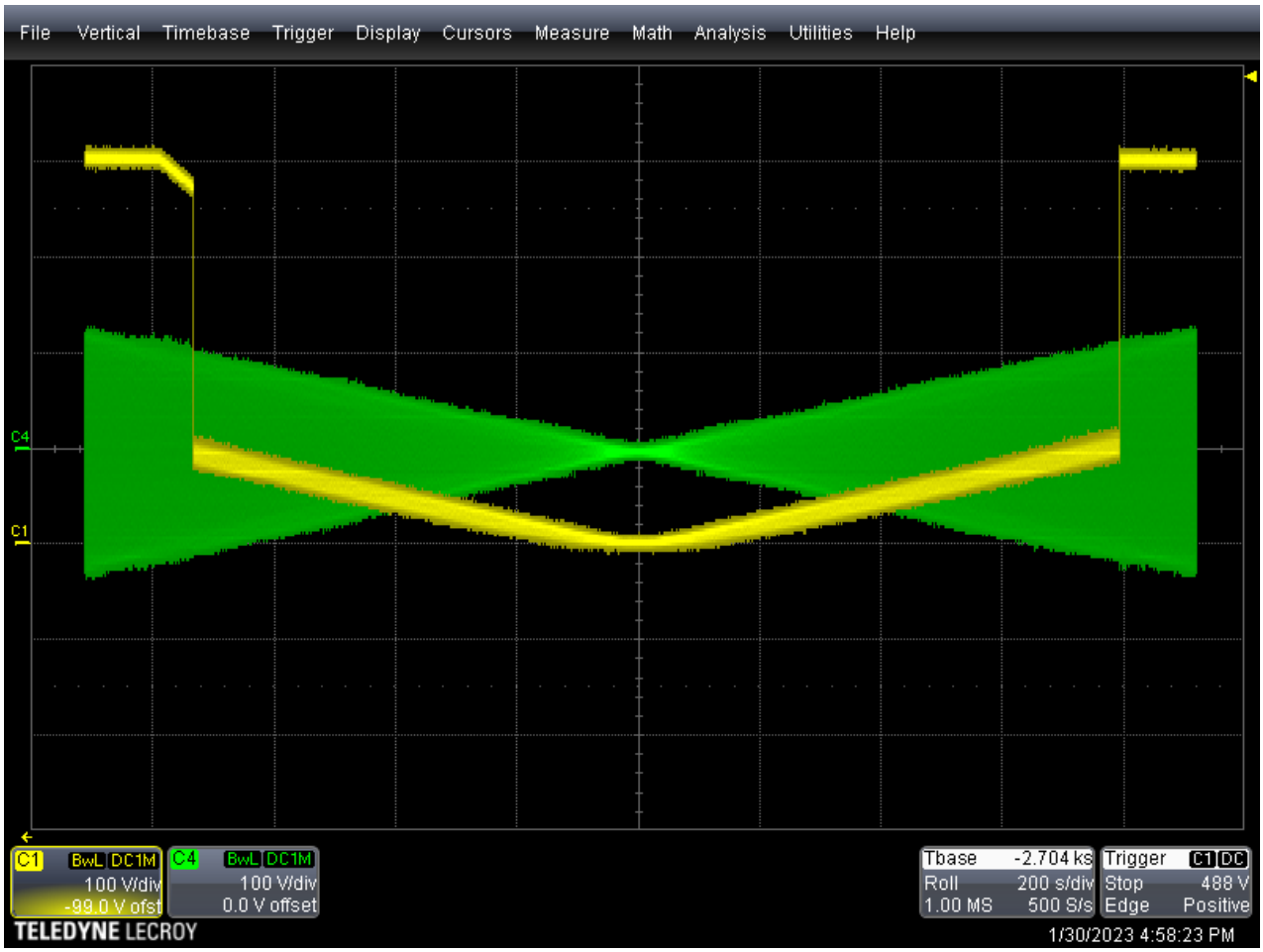


Figure 80 – Brown-Out Followed by Brown-In at 100% Load.
Yel: V_o, 100 V / div.
Grn: V_{IN}, 100V, 200s / div.

14.9.3 Drain Voltage and Inductor Current

PFC peak inductor current waveform was used as a metric for power sharing between the two paralleled 250 W PFC stages of the DER-977. A zoom is captured at the peak current to show maximum drain voltage and inductor current.

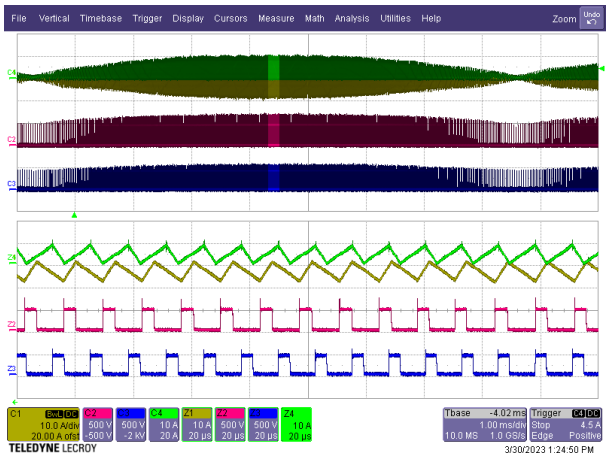


Figure 81 – Input Voltage 90 VAC, 100% Load.
Grn: IT1, 10 A / div.
Yel: IT4, 10 A / div.
Red: V_{DR} U2, 500 V / div.
Blu: V_{DR} U1, 500 V / div, 1 ms / div.

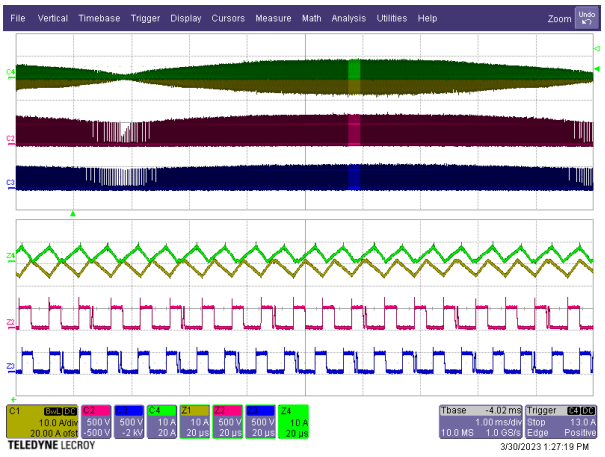


Figure 82 – Input Voltage 115 VAC, 100% Load.
Grn: IT1, 10 A / div.
Yel: IT4, 10 A / div.
Red: V_{DR} U2, 500 V / div.
Blu: V_{DR} U1, 500 V / div, 1 ms / div.

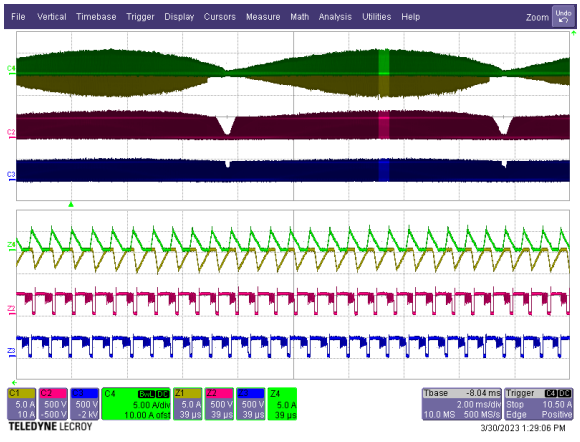


Figure 83 – Input Voltage 230 VAC, 100% Load.
Grn: IT1, 10 A / div.
Yel: IT4, 10 A / div.
Red: V_{DR} U2, 500 V / div.
Blu: V_{DR} U1, 500 V / div, 2 ms / div.

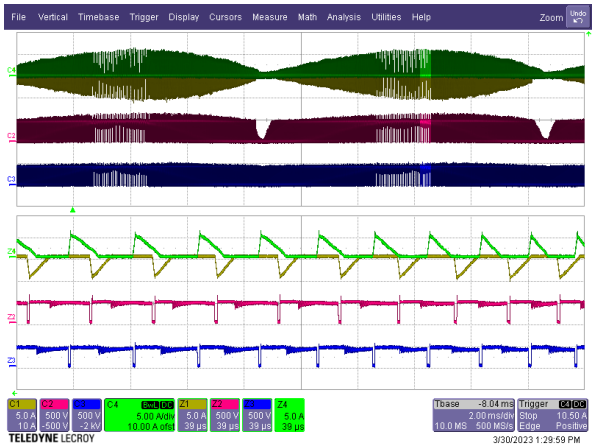


Figure 84 – Input Voltage 264 VAC, 100% Load.
Grn: IT1, 10 A / div.
Yel: IT4, 10 A / div.
Red: V_{DR} U2, 500 V / div.
Blu: V_{DR} U1, 500 V / div, 2 ms / div.

14.10 *Output Ripple Measurements*

14.10.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick up. Details of the probe modification are provided in the figures below.

The 4987BA probe adapter is modified with one 0.022 μF/ 630V film capacitor, tied across the probe tip.

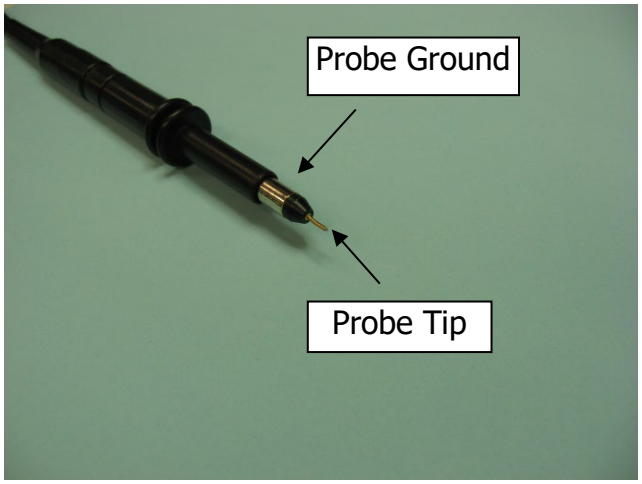


Figure 85 – Oscilloscope Probe Prepared for Ripple Measurement (End cap and ground lead removed.)

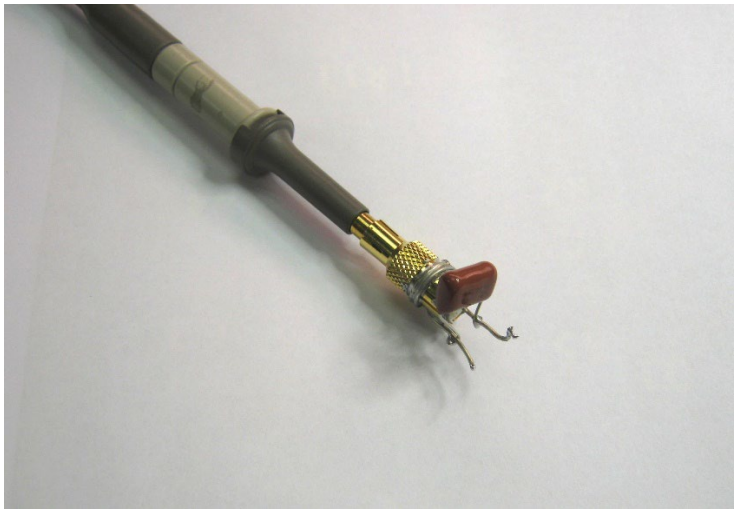


Figure 86 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter (Modified with wires for ripple measurement, and one 0.022 μF decoupling capacitor added.)

14.10.2 Measurement Results 90 VAC

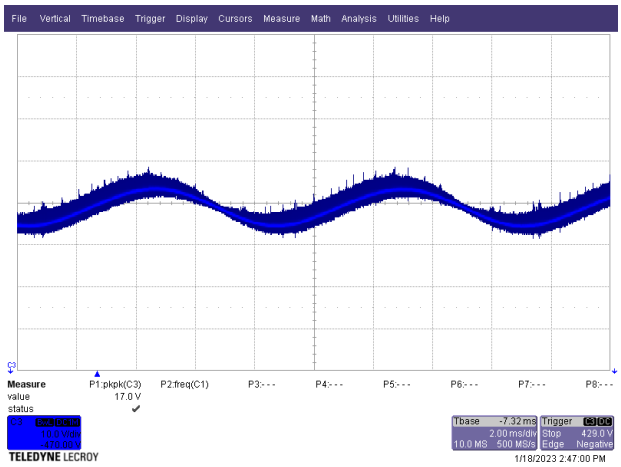


Figure 87 – Ripple, 90 VAC, 100% Load.
5 V / div., 2 ms / div.

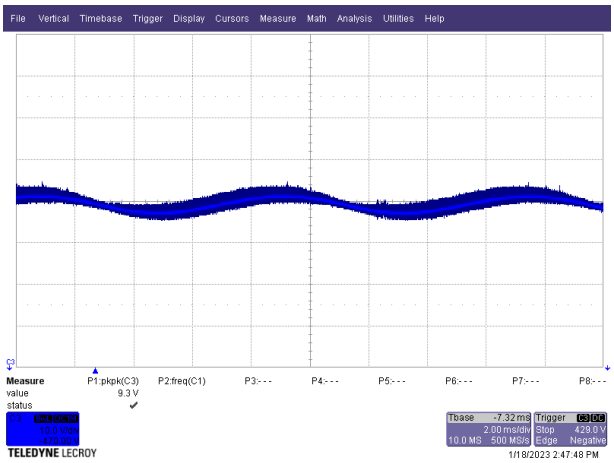


Figure 88 – Ripple, 90 VAC, 50% Load.
5 V / div., 2 ms / div.

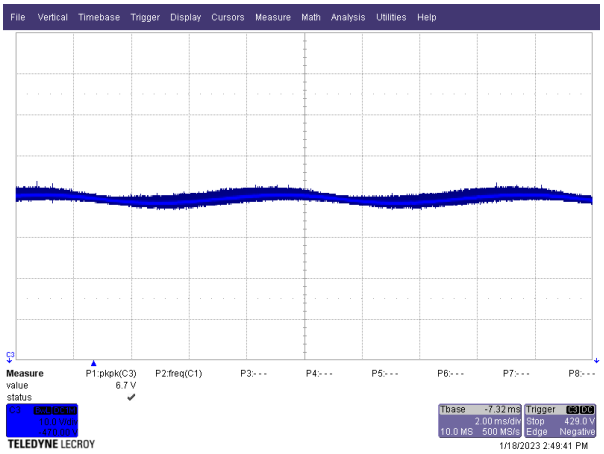


Figure 89 – Ripple, 90 VAC, 25% Load.
5 V / div., 2 ms / div.

14.10.3 Measurement Results, 115 VAC

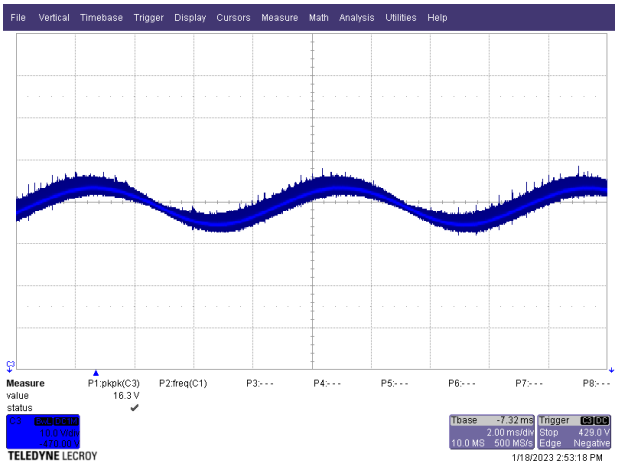


Figure 90 – Ripple, 115 VAC, 100% Load.
5 V / div., 2 ms / div.

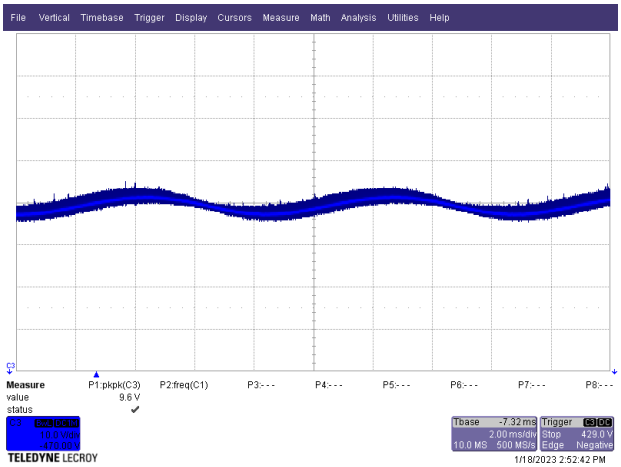


Figure 91 – Ripple, 115 VAC, 50% Load.
5 V / div., 2 ms / div.

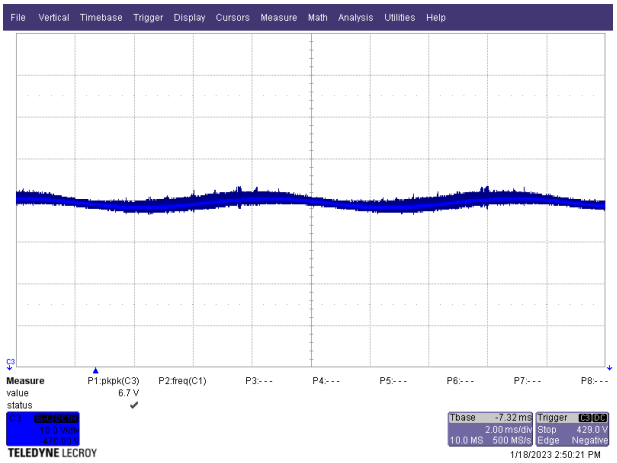


Figure 92 – Ripple, 115 VAC, 25% Load.
5 V / div., 2 ms / div.

14.10.4 Measurement Results, 230 VAC

For 230 and 264 VAC measurements, time base was increased to 100ms/div to view low frequency ripple content.

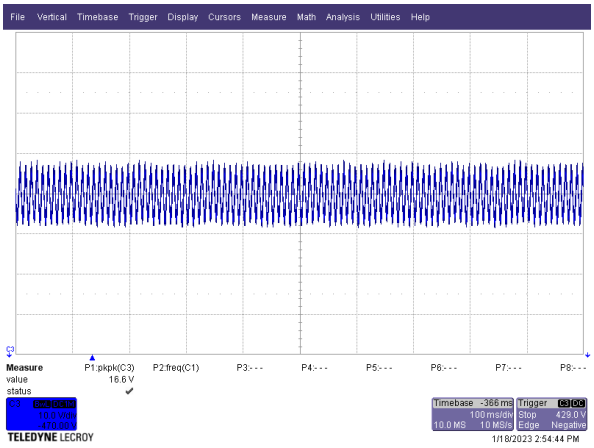


Figure 93 – Ripple, 230 VAC, 100% Load. 10 V / div., 100 ms / div.

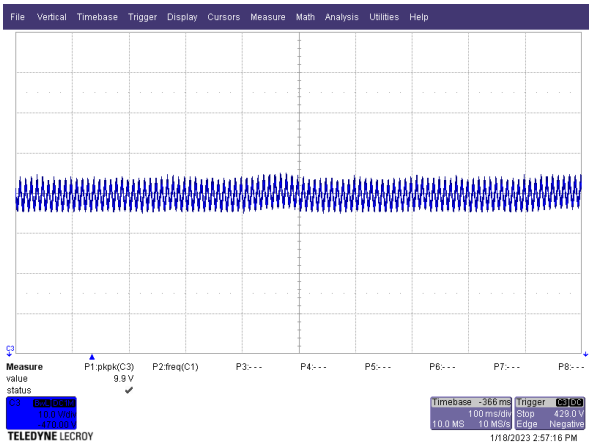


Figure 94 – Ripple, 230 VAC, 50% Load. 10 V / div., 100 ms / div.

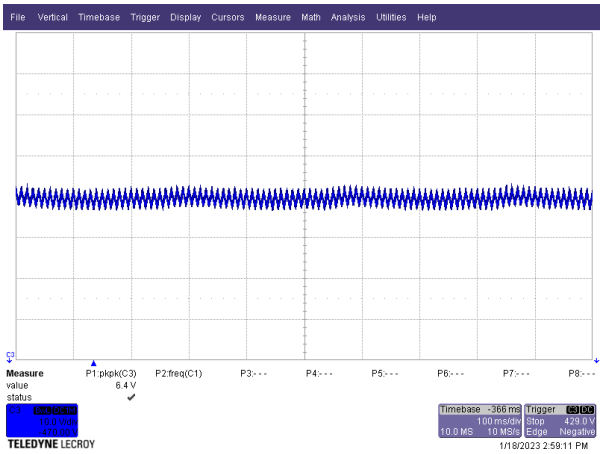


Figure 95 – Ripple, 230 VAC, 25% Load. 10 V / div., 100 ms / div.

14.10.5 Measurement Results, 264 VAC

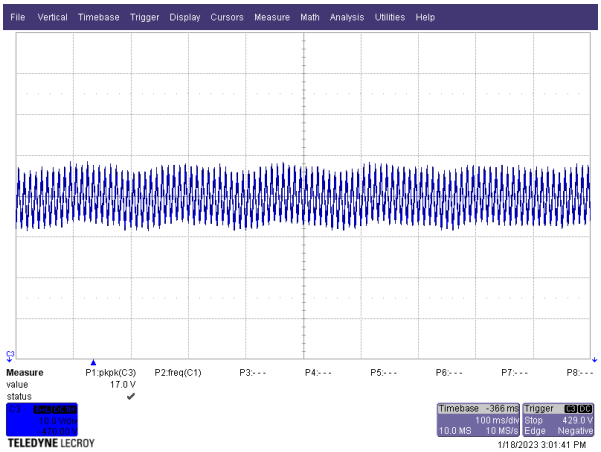


Figure 96 – Ripple, 264 VAC, 100% Load.
10 V / div., 100 ms / div.

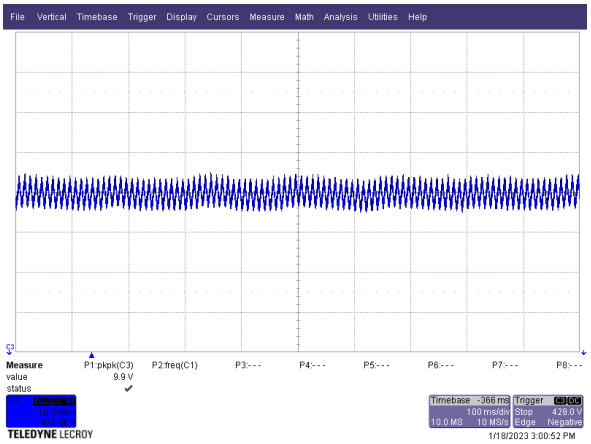


Figure 97 – Ripple, 264 VAC, 50% Load.
10 V / div., 100 ms / div.

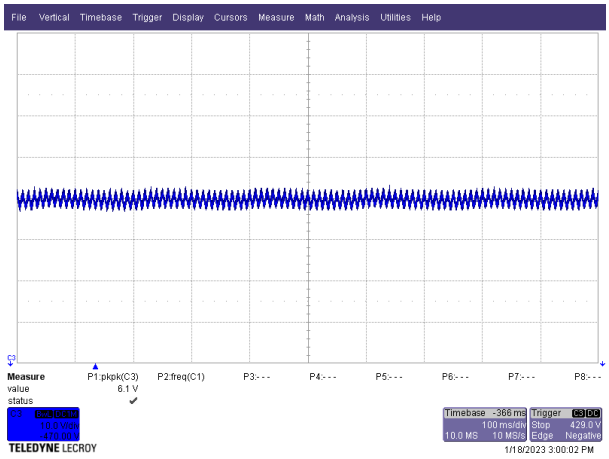


Figure 98 – Ripple, 264 VAC, 25% Load.
10 V / div., 100 ms / div.

14.11 *Gain-Phase Measurement Procedure and Results*

- The PFC stage is supplied from an adjustable AC source for this test. Connect the circuit as shown in figure below. Open the top end of the feedback divider network and insert a 100 Ω–2 W resistor in series as shown. The signal injected in the loop for gain–phase measurement will be injected across this resistor.
- Nodes A and B (two ends of the injection resistor) are connected to Channel 1 and Channel 2 of the frequency response analyzer using high voltage x100 attenuator probes. GND leads of both probes are connected to output return as shown.
- The signal to be injected is isolated using the Bode–Box injection transformer Model 200–000 from Venable Industries.

Test Procedure:

- Adjust the input voltage to 115 VAC and confirm that the PFC output voltage is within regulation limits.
- Inject a signal from the frequency response analyzer Use ~5V peak.
- Confirm the injected signal can be seen in the output voltage ripple of the PFC.
- Plot the gain phase by sweeping the injected signal frequency from 2 Hz to 90 Hz.
- Adjust the input voltage to 230 VAC and confirm PFC output is within regulation limits.
- Inject a signal from the frequency response analyzer Use ~5V peak.
- Confirm the injected signal can be seen in the output voltage ripple of the PFC.
- Plot the gain phase by sweeping the injected signal frequency from 2 Hz to 90 Hz.

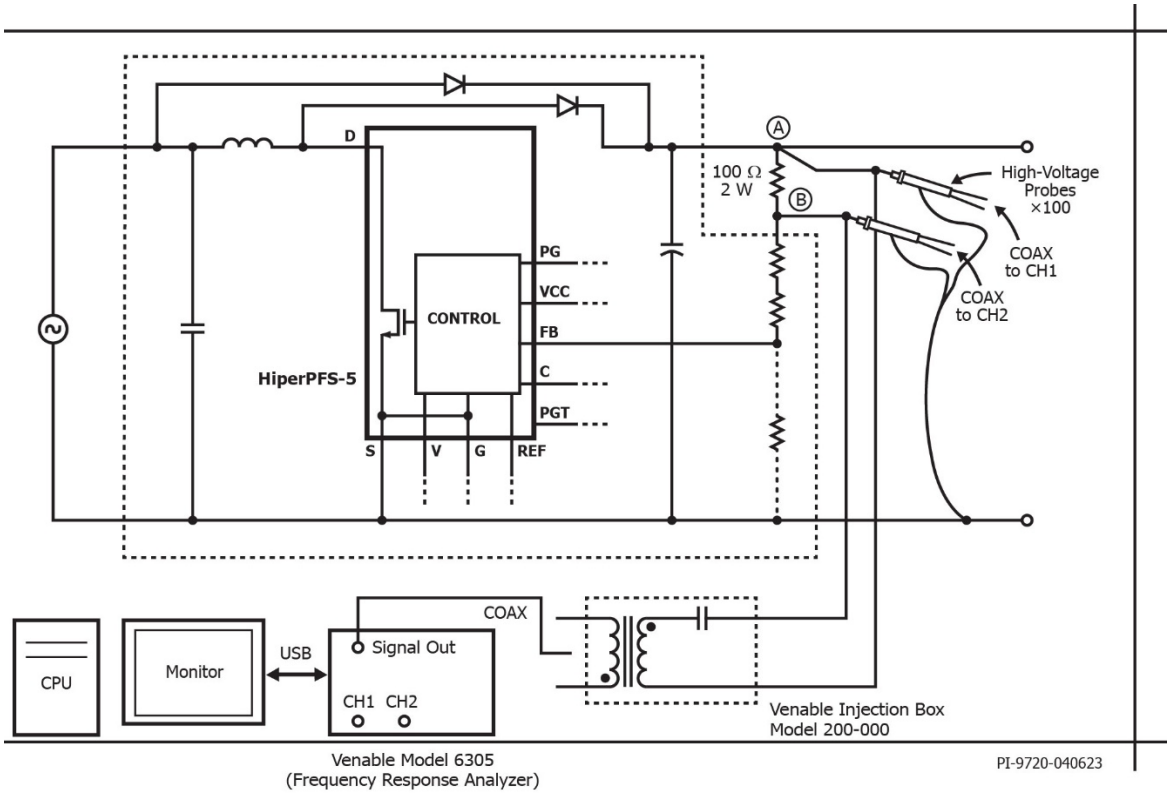


Figure 99 – System Test Set-up for Loop Gain-Phase Measurement.

14.11.1 Measured Bode Plots

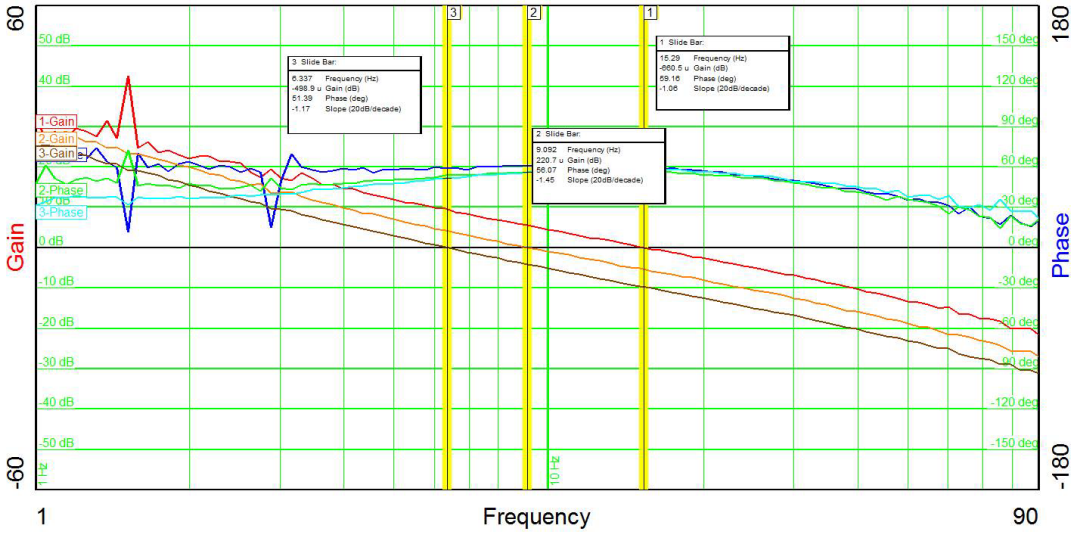


Figure 100 – Bode Plot with V_{IN} = 115 VAC at 100%, 50% and 25% Load.

100% Load (Red/Blu) – Slide Bar #1 Gain Crossover, 15.3 Hz, Phase Margin 59.2°.
50% Load (Orn/Grn) – Slide Bar #2, Gain Crossover 9.09 Hz, Phase Margin 56°.
25% Load (Brn/Aqua) – Slide Bar #3, Gain Crossover 6.3 Hz, Phase Margin 51.4°.

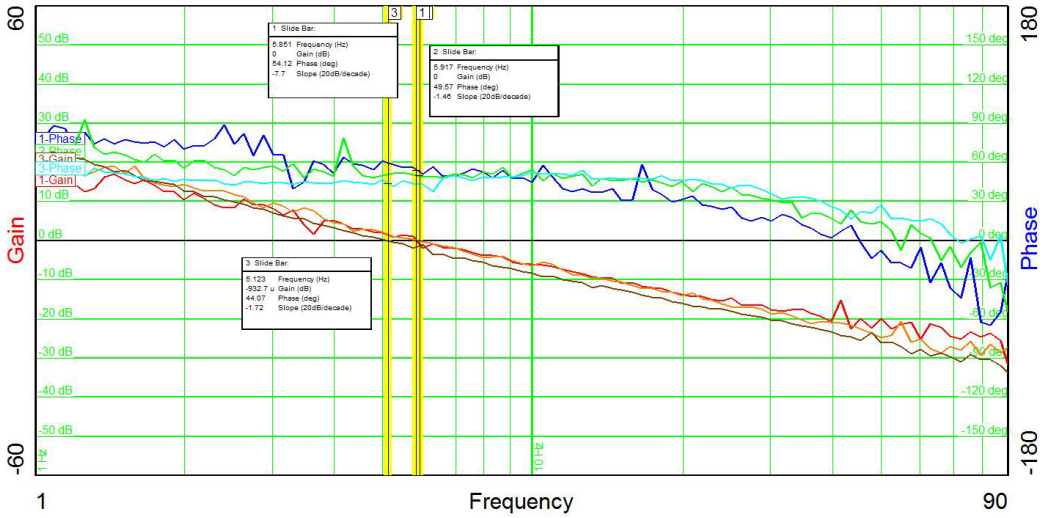


Figure 101 – Bode Plot with V_{IN} = 230 VDC at 100%, 50% and 25% Load.
100% Load (Red/Blu) – Slide Bar #1, Gain Crossover 5.85 Hz, Phase Margin 54.1°.
50% Load (Orn/Grn) – Slide Bar #2, Gain Crossover 5.92 Hz, Phase Margin 49.6°.
25% Load (Brn/Aqua) – Slide Bar #3, Gain Crossover 5.1 Hz, Phase Margin 44.1°.

15 Line Surge Test

Input line surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 50 Hz. The UUT output was resistively loaded at full load and operation was verified following each surge event. The UUT was powered with a 9 V battery. A single-sided 0.062” thick copper-clad FR4 material was placed under the UUT, insulation side up, and with the copper side of the board connected to earth ground at the AC input connector. A series string of 3 neon indicator lamps with a 100k limiting resistor was used to monitor the output voltage and detect output interruptions. Pass criteria was no interruption of output voltage.

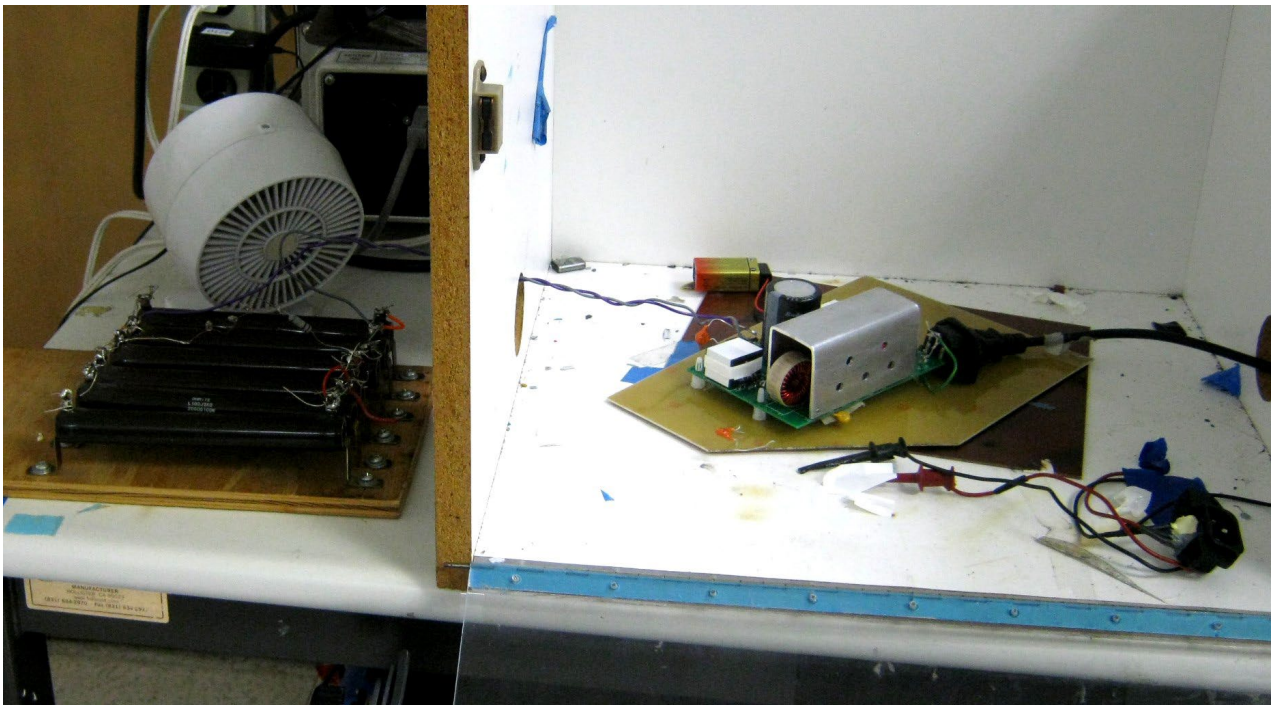


Figure 102 – Line Surge UUT Set-up.

15.1 *Differential Mode Surge*

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (°)	Generator Impedance (Ω)	Number of Strikes	Test Result
230	+1	0	2	10	PASS
230	-1	0	2	10	PASS
230	+1	90	2	10	PASS
230	-1	90	2	10	PASS
230	+1	180	2	10	PASS
230	-1	180	2	10	PASS
230	+1	270	2	10	PASS
230	-1	270	2	10	PASS

15.2 *Common Mode Surge (L, N-PE)*

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (°)	Generator Impedance (Ω)	Number of Strikes	Test Result
230	+2	0	12	10	PASS
230	-2	0	12	10	PASS
230	+2	90	12	10	PASS
230	-2	90	12	10	PASS
230	+2	180	12	10	PASS
230	-2	180	12	10	PASS
230	+2	270	12	10	PASS
230	-2	270	12	10	PASS

15.3 *Common Mode Surge (L – PE)*

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (°)	Generator Impedance (Ω)	Number of Strikes	Test Result
230	+2	0	12	10	PASS
230	-2	0	12	10	PASS
230	+2	90	12	10	PASS
230	-2	90	12	10	PASS
230	+2	180	12	10	PASS
230	-2	180	12	10	PASS
230	+2	270	12	10	PASS
230	-2	270	12	10	PASS

15.4 *Common Mode Surge (N – PE)*

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (º)	Generator Impedance (Ω)	Number of Strikes	Test Result
230	+2	0	12	10	PASS
230	-2	0	12	10	PASS
230	+2	90	12	10	PASS
230	-2	90	12	10	PASS
230	+2	180	12	10	PASS
230	-2	180	12	10	PASS
230	+2	270	12	10	PASS
230	-2	270	12	10	PASS

15.5 *Ring Wave (L, N – PE)*

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (º)	Generator Impedance (Ω)	Number of Strikes	Test Result
230	+2	0	12	10	PASS
230	-2	0	12	10	PASS
230	+2	90	12	10	PASS
230	-2	90	12	10	PASS
230	+2	180	12	10	PASS
230	-2	180	12	10	PASS
230	+2	270	12	10	PASS
230	-2	270	12	10	PASS

15.6 *Ring Wave (L – PE)*

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (º)	Generator Impedance (Ω)	Number of Strikes	Test Result
230	+2	0	12	10	PASS
230	-2	0	12	10	PASS
230	+2	90	12	10	PASS
230	-2	90	12	10	PASS
230	+2	180	12	10	PASS
230	-2	180	12	10	PASS
230	+2	270	12	10	PASS
230	-2	270	12	10	PASS

15.7 *Ring Wave (N – PE)*

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (°)	Generator Impedance (Ω)	Number of Strikes	Test Result
230	+2	0	12	10	PASS
230	-2	0	12	10	PASS
230	+2	90	12	10	PASS
230	-2	90	12	10	PASS
230	+2	180	12	10	PASS
230	-2	180	12	10	PASS
230	+2	270	12	10	PASS
230	-2	270	12	10	PASS

15.8 *EMI Test Set-up*

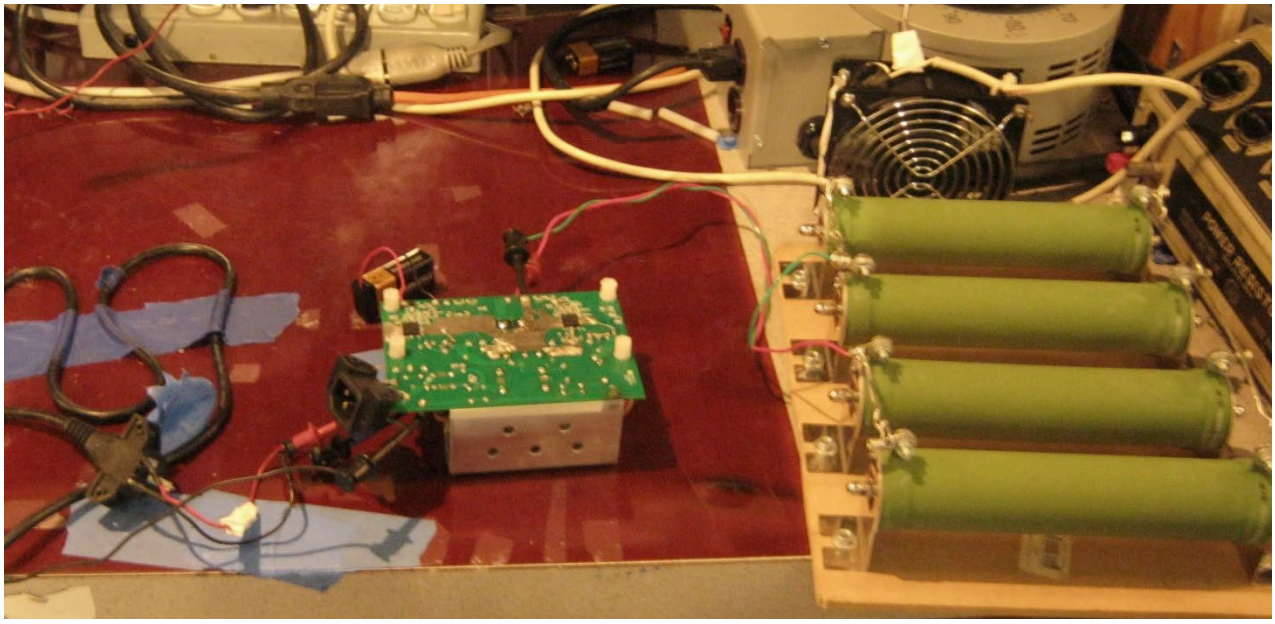


Figure 103 – EMI PFC Test Set-Up.

Auxiliary power to the PFS board at terminals TP4 (+) and TP5 (-) was supplied by a 9V battery. Connection from the AC safety ground at the DER-977 (TP3) was made directly to the LISN ground via a direct jumper, rather than through the AC line cord 3rd wire. All interconnections were made as short as possible. See Figure 100 above for set-up details.

15.9 *EMI Scans*

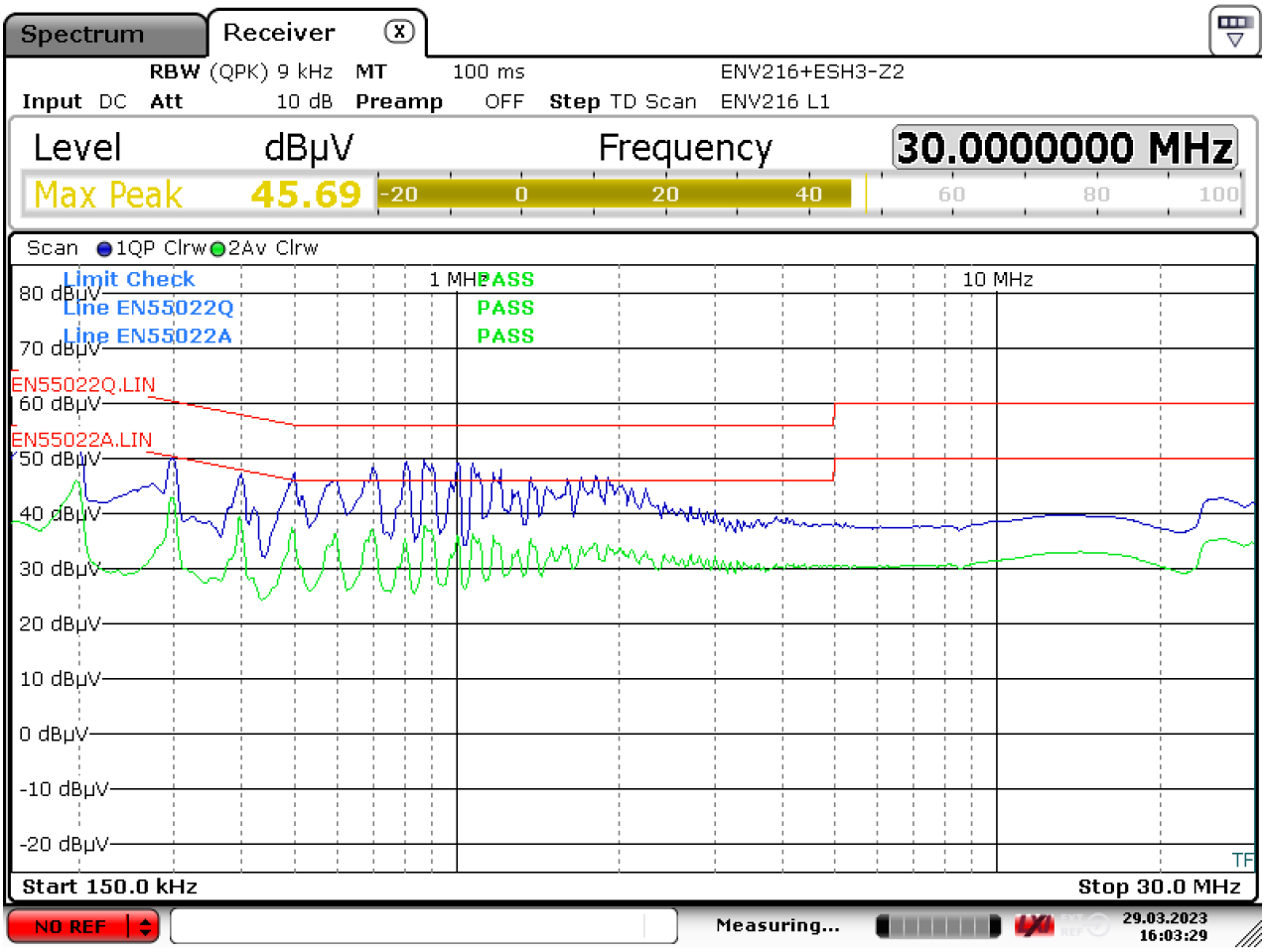


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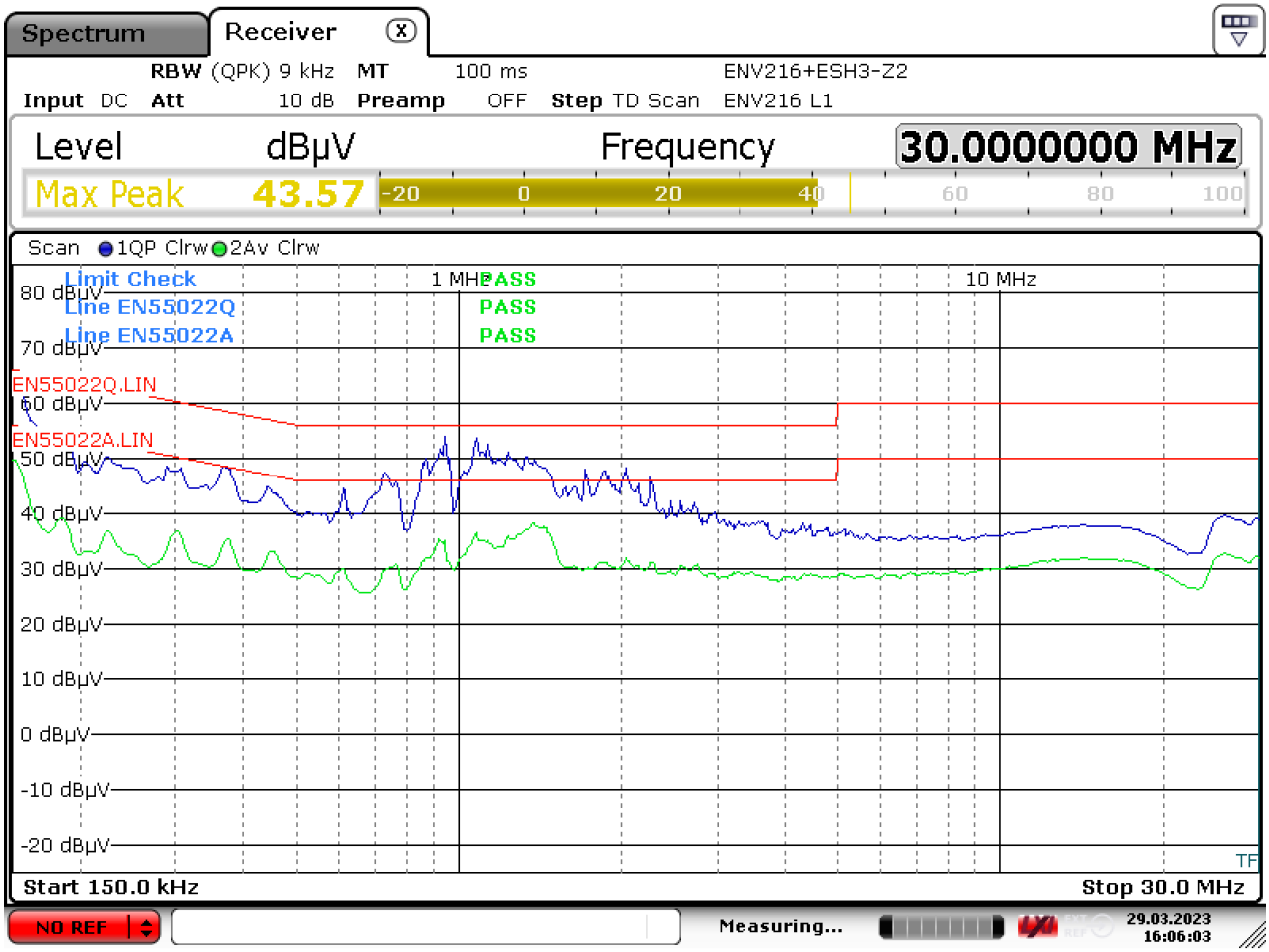
Figure 104 – EMI, 115 VAC, 100% Load.



Date: 29.MAR.2023 16:06:03

Figure 105 – EMI**,** 230 VAC, 100% Load.

16 Revision History

Date	Author	Revision	Description & changes	Reviewed
22-May-23	RH	1.0	Initial Release	Apps & Mktg

For the latest updates, visit our website: www.power.com

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