

## Design Example Report

<b>Title</b>	<b><i>20 W Isolated Flyback Power Supply Using InnoSwitch™ 3-AQ INN3977CQ</i></b>
<b>Specification</b>	30 VDC – 550 VDC Input; 30 VDC – 12 V / 0.83 A; 60 VDC – 12 V / 1.25 A; 130-550 VDC – 12 V / 1.67 A Output
<b>Application</b>	Wide Input Range For Automotive
<b>Author</b>	Applications Engineering Department
<b>Document Number</b>	DER-907Q
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### **Summary and Features**

- Wide input voltage range: 30 VDC to 550 VDC
- InnoSwitch3-AQ – industry first AC/DC ICs with isolated, safety rated integrated feedback
- Built-in synchronous rectification for >80 % efficiency
- All the benefits of secondary-side control with the simplicity of primary-side regulation
  - Insensitive to transformer variation
  - Extremely fast transient response independent of load timing

### **PATENT INFORMATION**

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at [www.power.com](http://www.power.com). Power Integrations grants its customers a license under certain patent rights as set forth at <https://www.power.com/company/intellectual-property-licensing/>.

### **Power Integrations**

5245 Hellyer Avenue, San Jose, CA 95138 USA.  
Tel: +1 408 414 9200 Fax: +1 408 414 9201  
[www.power.com](http://www.power.com)

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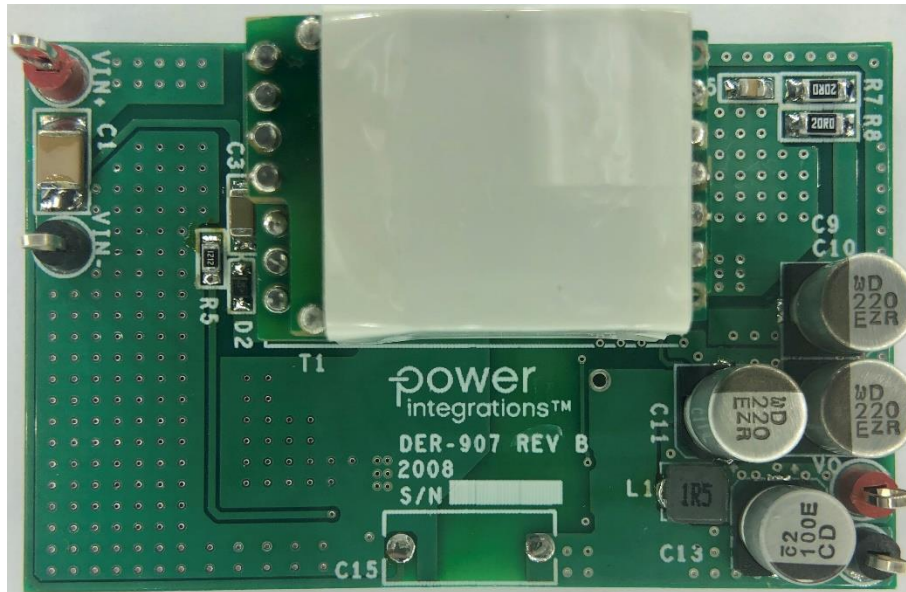
**Important Note:**

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

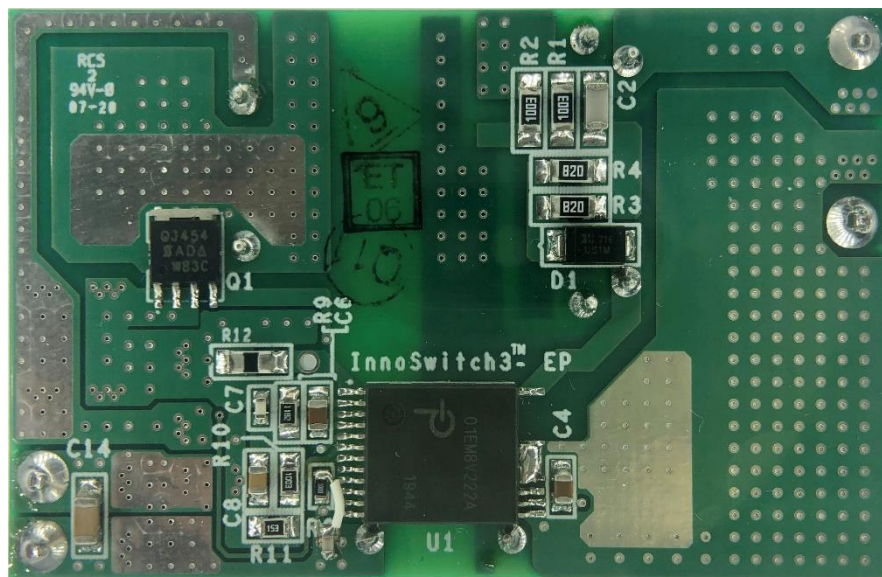


## 1 Introduction

This document is an engineering report describing a 30 VDC to 550 VDC input, 12 V output, 30 W Power Supply utilizing INN3977CQ from Power Integrations. The document contains the power supply specification, schematic, bill-of-materials and basic performance data.



**Figure 1** – Populated Circuit Board Photograph, Top.



**Figure 2** – Populated Circuit Board Photograph, Bottom.

## 2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
<b>Input</b>						
Voltage	$V_{IN}$	30	400	550	VDC	For Electric Vehicle Emergency PSU.
No-load Input Power (400 VDC)				50	mW	@ 400 VDC.
<b>Output</b>						
Output Voltage	$V_{OUT}$		12		V	±5%
Output Current	$I_{OUT}$		1.67	2.08	A	$V_{IN}$ 130 VDC to 550 VDC. (2.08 A Peak Current.)
Output Ripple Voltage	$V_{RIPPLE}$			240	mV	On Board.
<b>Total Output Power</b>						
Continuous Output Power	$P_{OUT}$			10	W	$V_{IN}$ of 30 VDC to 60 VDC. (Start-up at 5 W max.)
Continuous Output Power	$P_{OUT}$			15	W	$V_{IN}$ of 60 VDC to 130 VDC.
Continuous Output Power	$P_{OUT}$		20		W	$V_{IN}$ 130 VDC to 550 VDC.
Peak Power	$P_{OUT}$			25	W	$V_{IN}$ 130 VDC to 550 VDC.
<b>Isolation</b>		Meets IEC 60664-1 as a minimum. Reinforce better				
<b>Ambient Temperature</b>	$T_{AMB}$	-40		85	°C	Inside Inverter.

### 3 Schematic

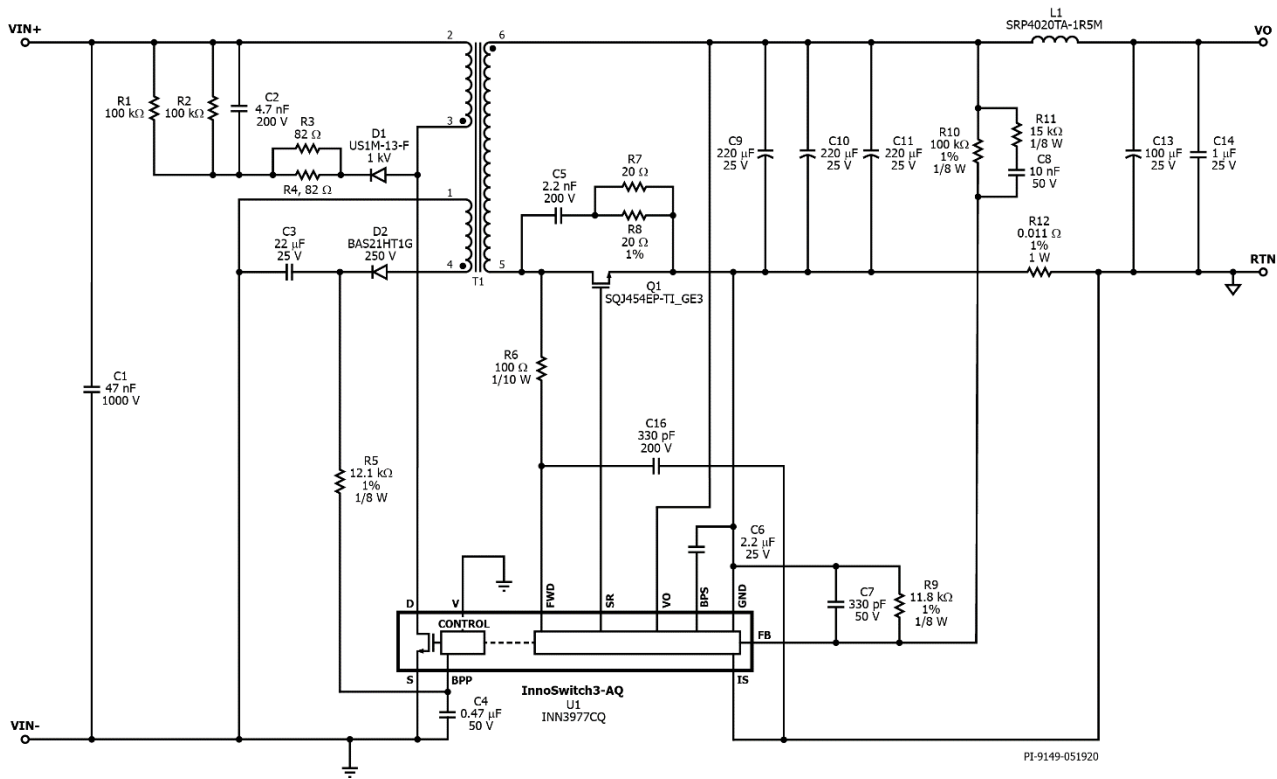


Figure 3 – Schematic.



## 4 Circuit Description

### 4.1 *INN3977CQ IC Primary*

One end of the transformer primary is connected to the DC bus, the other is connected to the integrated power MOSFET inside the INN3977CQ IC (U1). High-voltage ceramic capacitor C1 is used for the decoupling capacitor for the DC input voltage, and a low cost RCD clamp formed by D1, R1, R2, R3, and C2 limits the peak Drain voltage due to the effects of transformer leakage inductance. Capacitor C15, Y capacitor, is used to attenuate the high frequency common mode noise on the output.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor, C4, when DC input voltage is first applied. During normal operation the primary-side block is powered from an auxiliary winding on the transformer. The output of this is configured as a flyback winding which is rectified and filtered using diode D2 and capacitor C3, and fed in the BPP pin via a current limiting resistor R5.

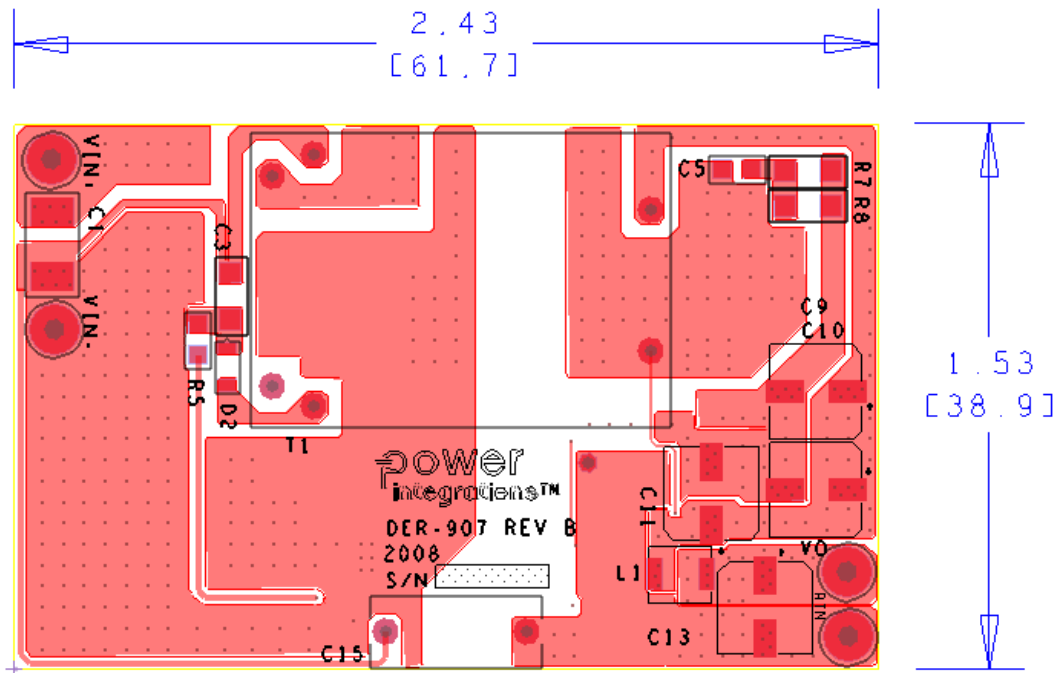
### 4.2 *INN3977CQ IC Secondary*

The secondary-side of the INN3977CQ IC provides output voltage, output current sensing and drive to a MOSFET providing synchronous rectification.

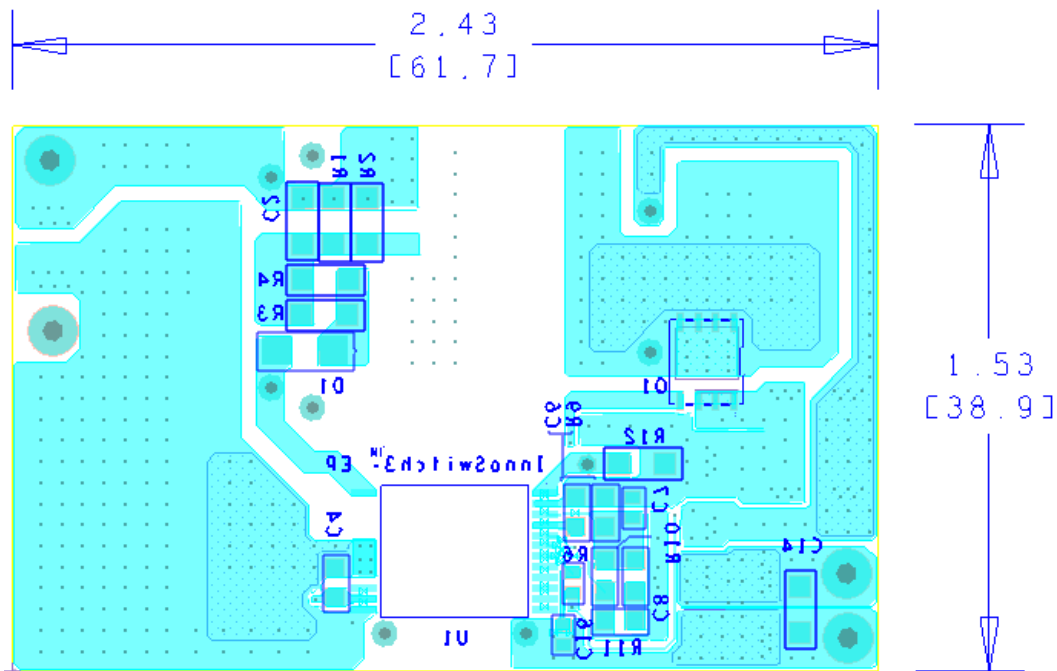
Output rectification for the 12 V output is provided by SR FET Q1. Low ESR capacitors, C9, C10, C11, C13 and output inductor L1 provide filtering. Ceramic capacitor C14 attenuates high frequency noise on the output. RC snubber network comprising R7, R8 and C5 for Q1 damps high frequency ringing across SR FETs, which results from leakage inductance of the transformer windings and the secondary trace inductances. The gate of Q1 is turned on based on the winding voltage sensed via R6 and the FWD pin of the IC. In continuous conduction mode operation, the power MOSFET is turned off just prior to the secondary-side controller commanding a new switching cycle from the primary. In discontinuous mode the MOSFET is turned off when the voltage drop across the MOSFET falls below ground. Secondary-side control of the primary-side MOSFET ensures that it is never on simultaneously with the synchronous rectification MOSFET. The MOSFET drive signal is output on the SR pin. The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. The output voltage powers the device, fed into the VO pin. It will charge the decoupling capacitor C6 via an internal regulator.

Resistors R9 and R10 form a voltage divider network that senses the output voltage. INN3977CQ IC has an internal reference of 1.265 V. Capacitor C7 provides decoupling from high frequency noise affecting power supply operation, and C8 and R11 is the feedforward networks to speed up the response time to lower the output ripple. The output current is sensed by R12 with a threshold of approximately 35 mV to reduce losses. Once the current sense threshold across these resistors is exceeded, the device adjusts the number of switch pulses to maintain a fixed output current.

## 5 PCB Layout



**Figure 4 – Printed Circuit Board Layout (Top).**



**Figure 5 – Printed Circuit Board Layout (Bottom).**



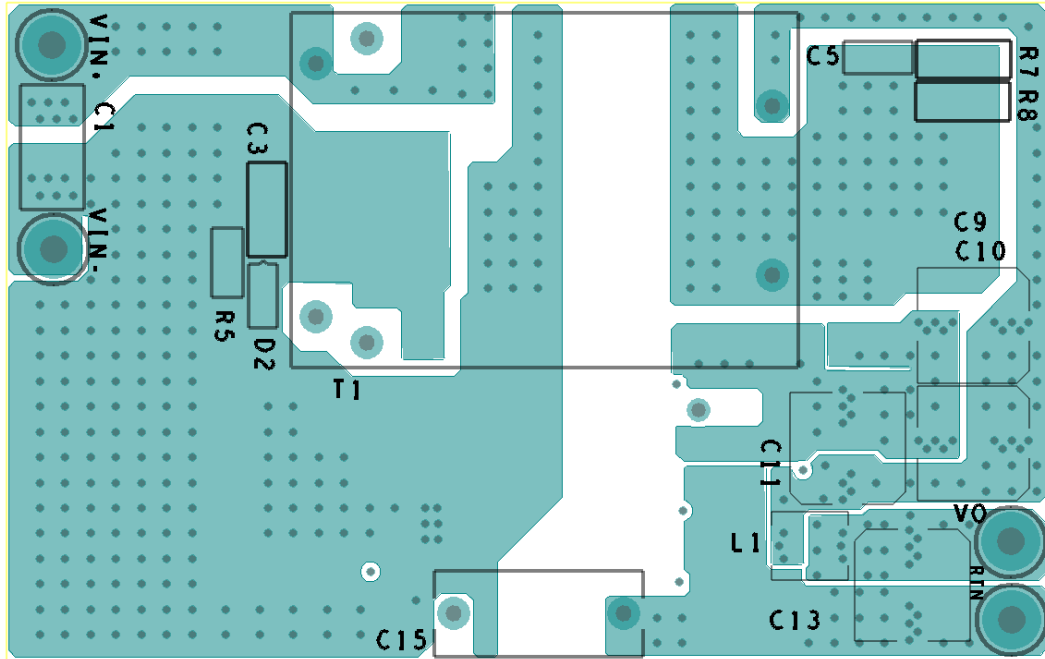


Figure 6 – Printed Circuit Board Layout (Internal layer 1).

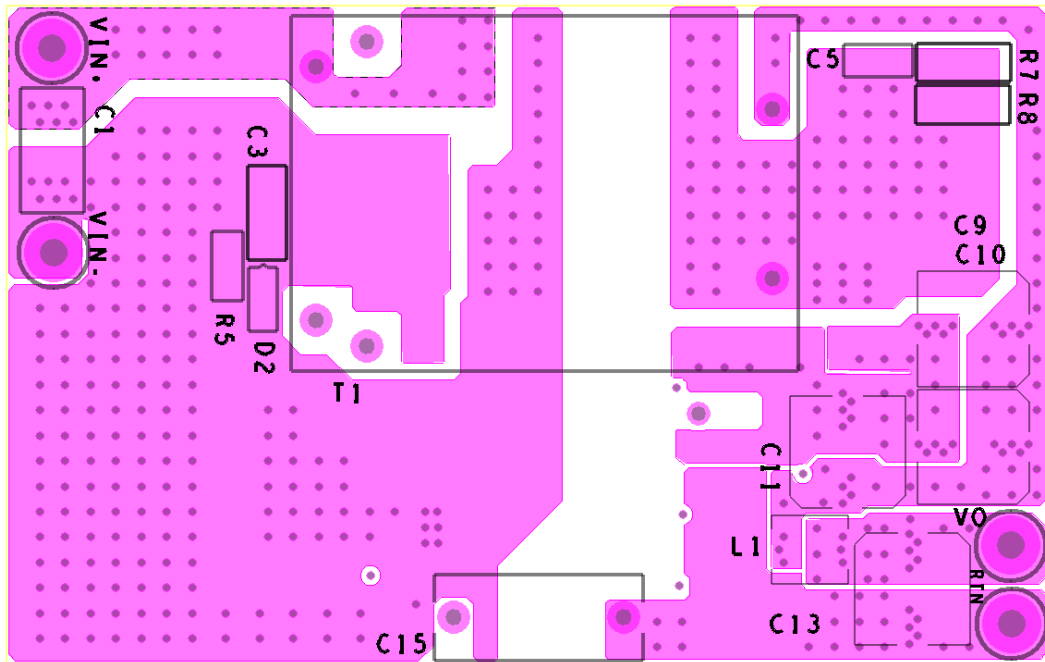


Figure 7 – Printed Circuit Board Layout (Internal layer 2).

## 6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	MFG
1	1	C1	0.047 $\mu$ F, $\pm$ 10%, 1000V (1kV), Ceramic, X7R, 1812	1812Y1K00473KST	Knowles Syfer
2	1	C2	4700 pF $\pm$ 5% 200V Ceramic C0G, NP0 1206	CGJ5H3C0G2D472J115AA	TDK
3	1	C3	22 $\mu$ F, $\pm$ 20%, 25V, Ceramic, X5R, 1206	12063D226MAT2A	AVX
4	1	C4	0.47 $\mu$ F, $\pm$ 10%, 50 V, Ceramic, X7R, 0805, -55°C ~ 125°C	CGA4J3X7R1H474K125AB	TDK
5	1	C5	2200 pF, $\pm$ 10%, 200V, Ceramic, X7R, 0805	08052C222K4T2A	AVX
6	1	C6	2.2 $\mu$ F, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
7	1	C7	330pF, $\pm$ 5%, 50V, Ceramic, C0G, NP0, 0603	C0603C331J5GACAUTO	KEMET
8	1	C8	10 nF, 50 V, Ceramic, X7R, 0805	C0805C103K5RACTU	Kemet
9	3	C9 C10 C11	220 $\mu$ F, 25 V, Electrolytic, 0.260" L x 0.260" W (6.60mm x 6.60mm) x 0.315" H (8.00mm), SMD	EMZR250ARA221MF80G	United Chemi-Con
10	1	C13	100 $\mu$ F, $\pm$ 20%, 25 V, Z=320 m $\Omega$ , Electrolytic, 0.260" L x 0.260" W (6.60mm x 6.60mm) x 0.315" H (8.00mm), SMD	UCD1E101MCL1GS	Nichicon
11	1	C14	1 $\mu$ F, 25 V, Ceramic, X7R, 1206	C3216X7R1E105K	TDK
12	1	C16	330 pF $\pm$ 5%, 200 V, Ceramic, C0G, NP0, 0603	CGJ3E3C0G2D331J080AA	TDK
13	1	D1	1000 V, 1 A, Ultrafast Recovery, GPP, DO-214AC SMA	US1M-13-F	Diodes, Inc.
14	1	D2	Diode, General Purpose, Power, Switching, SS SWCH DIO, 250V, SC-76, SOD-323	BAS21HT1G	ON Semi
15	1	L1	1.5 $\mu$ H, $\pm$ 20%, Shielded, Wirewound, Inductor, 4.5 A, 4 m $\Omega$ Max, Automotive, AEC-Q200, 2-SMD	SRP4020TA-1R5M	Bourns
16	1	Q1	MOSFET, N-Channel, 200 V, 13 A (Tc), 68 W (Tc), Automotive, AEC-Q101, PowerPAK <sup>®</sup> SO-8, PowerPAK SO-8	SQJ454EP-T1_GE3	Vishay
17	2	R1 R2	RES, 100 k, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ104V	Panasonic
18	2	R3 R4	RES, 82 $\Omega$ , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ820V	Panasonic
19	1	R5	RES, 12.1 k $\Omega$ , 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1212V	Panasonic
20	1	R6	RES, 100 R, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ101V	Panasonic
21	2	R7 R8	RES, 20 R, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ200V	Panasonic
22	1	R9	RES, 11.8 k $\Omega$ , 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1182V	Panasonic
23	1	R10	RES, 100 k $\Omega$ , 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1003V	Panasonic
24	1	R11	RES, 15 k $\Omega$ , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ153V	Panasonic
25	1	R12	0.011 $\Omega$ , $\pm$ 1%, $\pm$ 75ppm/ $^{\circ}$ C, 1 W, 1206 Automotive AEC-Q200, Current Sense, -55°C ~ 155°C	ERJ-8CWFR011V	Panasonic
26	1	T1	Transformer, Planar, Customer, Payton, 30W	25-01176-00	Power Integrations
27	1	U1	InnoSwitch3-AQ, InSOP-24D	INN3977CQ	Power Integrations



## 7 Transformer Design

### 7.1 Electrical and Mechanical Specification

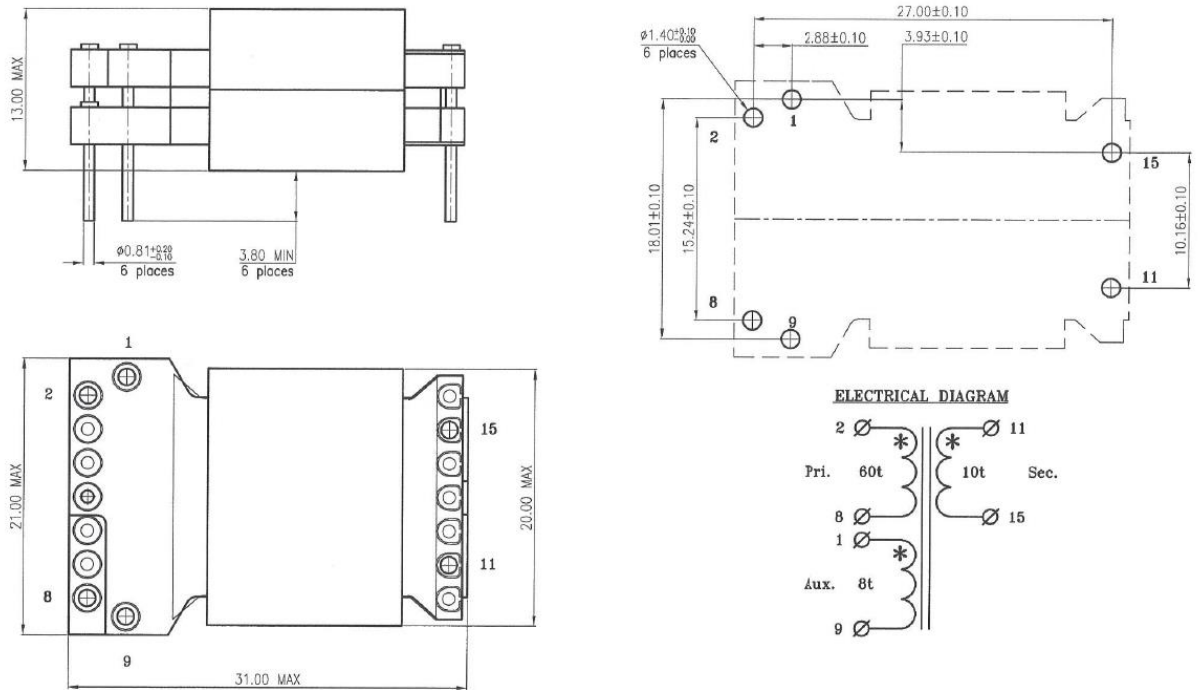


Figure 8 – Transformer Mechanical and Electrical Specification.

### 7.2 Electrical Specifications

Parameter	Condition	Spec.
<b>Nominal Primary Inductance</b>	Measured at 1 V <sub>PK-PK</sub> , 100 kHz switching frequency, between pin 3 and 6, with all other windings open.	590 $\mu$ H $\pm$ 5%
<b>Resonant Frequency</b>	Between pin 3 and 6, other windings open.	1,400 kHz (Min.)
<b>Primary Leakage Inductance</b>	Between pin 3 and 6, with pins:FL1-FL2 shorted.	11.5 $\mu$ H (Max.)

7.3 **Design Spreadsheet 20 W Continuous Power**

ACDC_InnoSwitch3-EP_Flyback_031620; Rev.1.5; Copyright Power Integrations 2020	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3 EP Flyback Design Spreadsheet
<b>APPLICATION VARIABLES</b>					
VIN_MIN	90		90	V	Minimum AC input voltage
VIN_MAX	389	Info	389	V	Input voltage too high: Decrease the maximum AC input voltage or verify the voltage rating of the input capacitor
VIN_RANGE			UNIVERSAL		Range of AC input voltage
LINEFREQ			60	Hz	AC Input voltage frequency
CAP_INPUT	1000.0		1000.0	uF	Input capacitor
VOUT	12.00		12.00	V	Output voltage at the board
CDC			0.00	mV	Cable drop compensation desired at full load
IOUT	1.670		1.670	A	Output current
POUT			20.04	W	Output power
EFFICIENCY	0.87		0.87		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
FACTOR_Z			0.50		Z-factor estimate
ENCLOSURE	OPEN FRAME		OPEN FRAME		Power supply enclosure
<b>PRIMARY CONTROLLER SELECTION</b>					
ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
DEVICE_GENERIC	INN36X7		INN36X7		Generic device code
DEVICE_CODE			INN3677C		Actual device code
POUT_MAX			40	W	Power capability of the device based on thermal performance
RDSON_100DEG			2.14	$\Omega$	Primary switch on time drain resistance at 100 degC
ILIMIT_MIN			1.255	A	Minimum current limit of the primary switch
ILIMIT_TYP			1.350	A	Typical current limit of the primary switch
ILIMIT_MAX			1.445	A	Maximum current limit of the primary switch
VDRAIN_BREAKDOWN			725	V	Device breakdown voltage
VDRAIN_ON_PRSW			0.37	V	Primary switch on time drain voltage
VDRAIN_OFF_PRSW		Warning	708.7	V	The peak drain voltage on the switch is higher than 650V: Decrease the device VOR
<b>WORST CASE ELECTRICAL PARAMETERS</b>					
FSWITCHING_MAX	56500		56500	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
VOR	90.0		90.0	V	Secondary voltage reflected to the primary when the primary switch turns off
VMIN			124.66	V	Valley of the minimum input AC voltage at full load
KP			1.67		Measure of continuous/discontinuous mode of operation
MODE_OPERATION			DCM		Mode of operation
DUTYCYCLE			0.302		Primary switch duty cycle
TIME_ON			6.34	us	Primary switch on-time
TIME_OFF			12.42	us	Primary switch off-time



LPRIMARY_MIN			563.7	uH	Minimum primary inductance
LPRIMARY_TYP			593.3	uH	Typical primary inductance
LPRIMARY_TOL			5.0	%	Primary inductance tolerance
LPRIMARY_MAX			623.0	uH	Maximum primary inductance
<b>PRIMARY CURRENT</b>					
IPEAK_PRIMARY			1.285	A	Primary switch peak current
IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
I AVG_PRIMARY			0.173	A	Primary switch average current
IRIPPLE_PRIMARY			1.285	A	Primary switch ripple current
IRMS_PRIMARY			0.385	A	Primary switch RMS current
<b>SECONDARY CURRENT</b>					
IPEAK_SECONDARY			9.638	A	Secondary winding peak current
IPEDESTAL_SECONDARY			0.000	A	Secondary winding current pedestal
IRMS_SECONDARY			3.396	A	Secondary winding RMS current
<b>TRANSFORMER CONSTRUCTION PARAMETERS</b>					
<b>CORE SELECTION</b>					
CORE	CUSTOM	Info	CUSTOM		The transformer windings may not fit: pick a bigger core or bobbin and refer to the Transformer Parameters tab for fit calculations
CORE CODE	Planar		Planar		Core code
AE	50.00		50.00	mm <sup>2</sup>	Core cross sectional area
LE	32.00		32.00	mm	Core magnetic path length
AL	10000		10000	nH/turns <sup>2</sup>	Ungapped core effective inductance
VE	156.0		156.0	mm <sup>3</sup>	Core volume
BOBBIN	Planar		Planar		Bobbin
AW	20.00		20.00	mm <sup>2</sup>	Window area of the bobbin
BW	20.00		20.00	mm	Bobbin width
MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
<b>PRIMARY WINDING</b>					
NPRIMARY			60		Primary turns
BPEAK			3071	Gauss	Peak flux density
BMAX			2625	Gauss	Maximum flux density
BAC			1313	Gauss	AC flux density (0.5 x Peak to Peak)
ALG			165	nH/turns <sup>2</sup>	Typical gapped core effective inductance
LG			0.375	mm	Core gap length
LAYERS_PRIMARY			1		Number of primary layers
AWG_PRIMARY			30	AWG	Primary winding wire AWG
OD_PRIMARY_INSULATED			0.303	mm	Primary winding wire outer diameter with insulation
OD_PRIMARY_BARE			0.255	mm	Primary winding wire outer diameter without insulation
CMA_PRIMARY			261	Cmil/A	Primary winding wire CMA
<b>SECONDARY WINDING</b>					
NSECONDARY	8		8		Secondary turns
AWG_SECONDARY			21	AWG	Secondary winding wire AWG
OD_SECONDARY_INSULATED			1.029	mm	Secondary winding wire outer diameter with insulation
OD_SECONDARY_BARE			0.723	mm	Secondary winding wire outer diameter without insulation
CMA_SECONDARY			239	Cmil/A	Secondary winding wire CMA
<b>BIAS WINDING</b>					
NBIAS			9		Bias turns
<b>PRIMARY COMPONENTS SELECTION</b>					
<b>LINE UNDERVOLTAGE</b>					
BROWN-IN REQUIRED			72.0	V	Required AC RMS line voltage

					brown-in threshold
RLS			3.64	MΩ	Connect two 1.82 MOhm resistors to the V-pin for the required UV/OV threshold
BROWN-IN ACTUAL			73.0	V	Actual AC RMS brown-in threshold
BROWN-OUT ACTUAL			66.0	V	Actual AC RMS brown-out threshold
<b>LINE OVERVOLTAGE</b>					
OVERVOLTAGE_LINE		Info	304.2	V	The line over-voltage threshold is lower than the maximum input AC RMS voltage
<b>BIAS DIODE</b>					
VBIAS			12.0	V	Rectified bias voltage
VF_BIAS			0.70	V	Bias winding diode forward drop
VREVERSE_BIASDIODE			94.31	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
CBIAS			22	uF	Bias winding rectification capacitor
CBPP			0.47	uF	BPP pin capacitor
<b>SECONDARY COMPONENTS</b>					
RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the first output voltage)
RFB_LOWER			11.80	kΩ	Lower feedback resistor
CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
<b>MULTIPLE OUTPUT PARAMETERS</b>					
<b>OUTPUT 1</b>					
VOUT1			12.00	V	Output 1 voltage
IOUT1			1.67	A	Output 1 current
POUT1			20.04	W	Output 1 power
IRMS_SECONDARY1			3.396	A	Root mean squared value of the secondary current for output 1
IRIPPLE_CAP_OUTPUT1			2.957	A	Current ripple on the secondary waveform for output 1
AWG_SECONDARY1			21	AWG	Wire size for output 1
OD_SECONDARY1_INSULATED			1.029	mm	Secondary winding wire outer diameter with insulation for output 1
OD_SECONDARY1_BARE			0.723	mm	Secondary winding wire outer diameter without insulation for output 1
CM_SECONDARY1			679	Cmils	Bare conductor effective area in circular mils for output 1
NSECONDARY1			8		Number of turns for output 1
VREVERSE_RECTIFIER1			85.16	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
SRFET1			SQJA62EP		Secondary rectifier (Logic MOSFET) for output 1
VF_SRFET1			0.790	V	SRFET on-time drain voltage for output 1
VBREAKDOWN_SRFET1			200	V	SRFET breakdown voltage for output 1
RDSON_SRFET1			62.0	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1



7.4 **Design Spreadsheet 25 W Peak Power**

1	ACDC_InnoSwitch3-EP_Flyback_031620; Rev.1.5; Copyright Power Integrations 2020	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3 EP Flyback Design Spreadsheet
2	<b>APPLICATION VARIABLES</b>					
3	VIN_MIN	90		90	V	Minimum AC input voltage
4	VIN_MAX	389	Info	389	V	Input voltage too high: Decrease the maximum AC input voltage or verify the voltage rating of the input capacitor
5	VIN_RANGE			UNIVERSAL		Range of AC input voltage
6	LINEFREQ			60	Hz	AC Input voltage frequency
7	CAP_INPUT	1000.0		1000.0	uF	Input capacitor
8	VOUT	12.00		12.00	V	Output voltage at the board
9	CDC			0.00	mV	Cable drop compensation desired at full load
10	IOUT	2.080		2.080	A	Output current
11	POUT			24.96	W	Output power
12	EFFICIENCY	0.87		0.87		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
13	FACTOR_Z			0.50		Z-factor estimate
14	ENCLOSURE	OPEN FRAME		OPEN FRAME		Power supply enclosure
18	<b>PRIMARY CONTROLLER SELECTION</b>					
19	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
20	DEVICE_GENERIC	INN36X7		INN36X7		Generic device code
21	DEVICE_CODE			INN3677C		Actual device code
22	POUT_MAX			40	W	Power capability of the device based on thermal performance
23	RDSON_100DEG			2.14	Ω	Primary switch on time drain resistance at 100 degC
24	ILIMIT_MIN			1.255	A	Minimum current limit of the primary switch
25	ILIMIT_TYP			1.350	A	Typical current limit of the primary switch
26	ILIMIT_MAX			1.445	A	Maximum current limit of the primary switch
27	VDRAIN_BREAKDOWN			725	V	Device breakdown voltage
28	VDRAIN_ON_PRSW			0.46	V	Primary switch on time drain voltage
29	VDRAIN_OFF_PRSW		Warning	708.7	V	The peak drain voltage on the switch is higher than 650V: Decrease the device VOR
33	<b>WORST CASE ELECTRICAL PARAMETERS</b>					
34	FSWITCHING_MAX	66500		66500	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
35	VOR	90.0		90.0	V	Secondary voltage reflected to the primary when the primary switch turns off
36	VMIN			124.35	V	Valley of the minimum input AC voltage at full load
37	KP			1.25		Measure of continuous/discontinuous mode of operation
38	MODE_OPERATION			DCM		Mode of operation

39	DUTYCYCLE			0.367		Primary switch duty cycle
40	TIME_ON			6.59	us	Primary switch on-time
41	TIME_OFF			9.59	us	Primary switch off-time
42	LPRIMARY_MIN			565.0	uH	Minimum primary inductance
43	LPRIMARY_TYP			594.8	uH	Typical primary inductance
44	LPRIMARY_TOL			5.0	%	Primary inductance tolerance
45	LPRIMARY_MAX			624.5	uH	Maximum primary inductance
<b>47</b>	<b>PRIMARY CURRENT</b>					
48	IPEAK_PRIMARY			1.327	A	Primary switch peak current
49	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
50	IAVG_PRIMARY			0.217	A	Primary switch average current
51	IRIPPLE_PRIMARY			1.327	A	Primary switch ripple current
52	IRMS_PRIMARY			0.438	A	Primary switch RMS current
<b>54</b>	<b>SECONDARY CURRENT</b>					
55	IPEAK_SECONDARY			9.954	A	Secondary winding peak current
56	IPEDESTAL_SECONDARY			0.000	A	Secondary winding current pedestal
57	IRMS_SECONDARY			3.852	A	Secondary winding RMS current
<b>61</b>	<b>TRANSFORMER CONSTRUCTION PARAMETERS</b>					
<b>62</b>	<b>CORE SELECTION</b>					
63	CORE	CUSTOM	Info	CUSTOM		The transformer windings may not fit: pick a bigger core or bobbin and refer to the Transformer Parameters tab for fit calculations
64	CORE CODE	Planar		Planar		Core code
65	AE	50.00		50.00	mm <sup>2</sup>	Core cross sectional area
66	LE	32.00		32.00	mm	Core magnetic path length
67	AL	10000		10000	nH/turns <sup>2</sup>	Ungapped core effective inductance
68	VE	156.0		156.0	mm <sup>3</sup>	Core volume
69	BOBBIN	Planar		Planar		Bobbin
70	AW	20.00		20.00	mm <sup>2</sup>	Window area of the bobbin
71	BW	20.00		20.00	mm	Bobbin width
72	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
<b>74</b>	<b>PRIMARY WINDING</b>					
75	NPRIMARY			60		Primary turns
76	BPEAK			3079	Gauss	Peak flux density
77	BMAX			2723	Gauss	Maximum flux density
78	BAC			1362	Gauss	AC flux density (0.5 x Peak to Peak)
79	ALG			165	nH/turns <sup>2</sup>	Typical gapped core effective inductance
80	LG			0.374	mm	Core gap length
81	LAYERS_PRIMARY			1		Number of primary layers
82	AWG_PRIMARY			30	AWG	Primary winding wire AWG
83	OD_PRIMARY_INSULATED			0.303	mm	Primary winding wire outer diameter with insulation
84	OD_PRIMARY_BARE			0.255	mm	Primary winding wire outer diameter without insulation
85	CMA_PRIMARY			230	Cmil/A	Primary winding wire CMA
<b>87</b>	<b>SECONDARY WINDING</b>					
88	NSECONDARY	8		8		Secondary turns
89	AWG_SECONDARY			21	AWG	Secondary winding wire AWG
90	OD_SECONDARY_INSULATED			1.029	mm	Secondary winding wire outer diameter with insulation





91	OD_SECONDARY_BARE			0.723	mm	Secondary winding wire outer diameter without insulation
92	CMA_SECONDARY			210	Cmil/A	Secondary winding wire CMA
<b>94</b>	<b>BIAS WINDING</b>					
95	NBIAS			9		Bias turns
<b>99</b>	<b>PRIMARY COMPONENTS SELECTION</b>					
<b>100</b>	<b>LINE UNDERVOLTAGE</b>					
101	BROWN-IN REQUIRED			72.0	V	Required AC RMS line voltage brown-in threshold
102	RLS			3.64	MΩ	Connect two 1.82 MOhm resistors to the V-pin for the required UV/OV threshold
103	BROWN-IN ACTUAL			73.0	V	Actual AC RMS brown-in threshold
104	BROWN-OUT ACTUAL			66.0	V	Actual AC RMS brown-out threshold
<b>106</b>	<b>LINE OVERVOLTAGE</b>					
107	OVERVOLTAGE_LINE		Info	304.2	V	The line over-voltage threshold is lower than the maximum input AC RMS voltage
<b>109</b>	<b>BIAS DIODE</b>					
110	VBIAS			12.0	V	Rectified bias voltage
111	VF_BIAS			0.70	V	Bias winding diode forward drop
112	VREVERSE_BIASDIODE			94.31	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
113	CBIAS			22	uF	Bias winding rectification capacitor
114	CBPP			0.47	uF	BPP pin capacitor
<b>118</b>	<b>SECONDARY COMPONENTS</b>					
119	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the first output voltage)
120	RFB_LOWER			11.80	kΩ	Lower feedback resistor
121	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
<b>125</b>	<b>MULTIPLE OUTPUT PARAMETERS</b>					
<b>126</b>	<b>OUTPUT 1</b>					
127	VOUT1			12.00	V	Output 1 voltage
128	IOUT1			2.08	A	Output 1 current
129	POUT1			24.96	W	Output 1 power
130	IRMS_SECONDARY1			3.852	A	Root mean squared value of the secondary current for output 1
131	IRIPPLE_CAP_OUTPUT1			3.242	A	Current ripple on the secondary waveform for output 1
132	AWG_SECONDARY1			21	AWG	Wire size for output 1
133	OD_SECONDARY1_INSULATED			1.029	mm	Secondary winding wire outer diameter with insulation for output 1
134	OD_SECONDARY1_BARE			0.723	mm	Secondary winding wire outer diameter without insulation for output 1
135	CM_SECONDARY1			770	Cmils	Bare conductor effective area in circular mils for output 1
136	NSECONDARY1			8		Number of turns for output 1
137	VREVERSE_RECTIFIER1			85.16	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
138	SRFET1	AUTO		SQJA62EP		Secondary rectifier (Logic

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						MOSFET) for output 1
139	VF_SRFET1			0.79	V	SRFET on-time drain voltage for output 1
140	VBREAKDOWN_SRFET1			200	V	SRFET breakdown voltage for output 1
141	RDSON_SRFET1			62.0	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1



## 8 Performance Data

All measurements performed with room ambient temperature. Measured at PCB output terminal.

### 8.1 Efficiency at 25%, 50%, 75% and 100% Load

#### 8.1.1 30 VDC, 12 V 0.85 A (10 W)

<b>Input: 30 VDC; Output: 12 V / 0.85 A (10 W)</b>					
<b>Load (%)</b>	<b>P<sub>IN</sub> (W)</b>	<b>V<sub>OUT</sub> (V)</b>	<b>I<sub>OUT</sub> (A)</b>	<b>P<sub>OUT</sub> (W)</b>	<b>Efficiency (%)</b>
100	11.89	11.51	0.85	9.79	82.32
75	8.91	11.62	0.64	7.41	83.13
50	6.10	11.88	0.42	5.05	82.72
25	3.18	11.96	0.21	2.54	79.73

#### 8.1.2 60 VDC, 12 V 1.25 A (15 W)

<b>Input: 60 VDC; Output: 12 V / 1.25 A (15 W)</b>					
<b>Load (%)</b>	<b>P<sub>IN</sub> (W)</b>	<b>V<sub>OUT</sub> (V)</b>	<b>I<sub>OUT</sub> (A)</b>	<b>P<sub>OUT</sub> (W)</b>	<b>Efficiency (%)</b>
100	17.57	11.79	1.25	14.73	83.83
75	13.44	11.97	0.94	11.22	83.47
50	9.01	12.01	0.63	7.51	83.41
25	4.51	11.99	0.31	3.75	83.06

#### 8.1.3 130 VDC, 12 V 1.67 A (20 W)

<b>Input: 130 VDC; Output: 12 V / 1.67 A (20 W)</b>					
<b>Load (%)</b>	<b>P<sub>IN</sub> (W)</b>	<b>V<sub>OUT</sub> (V)</b>	<b>I<sub>OUT</sub> (A)</b>	<b>P<sub>OUT</sub> (W)</b>	<b>Efficiency (%)</b>
100	23.47	12.01	1.67	20.05	85.46
75	17.67	12.04	1.25	15.08	85.35
50	11.80	12.04	0.84	10.05	85.20
25	5.90	12.01	0.42	5.01	84.92

## 8.1.4 400 VDC, 12 V 1.67 A (20 W)

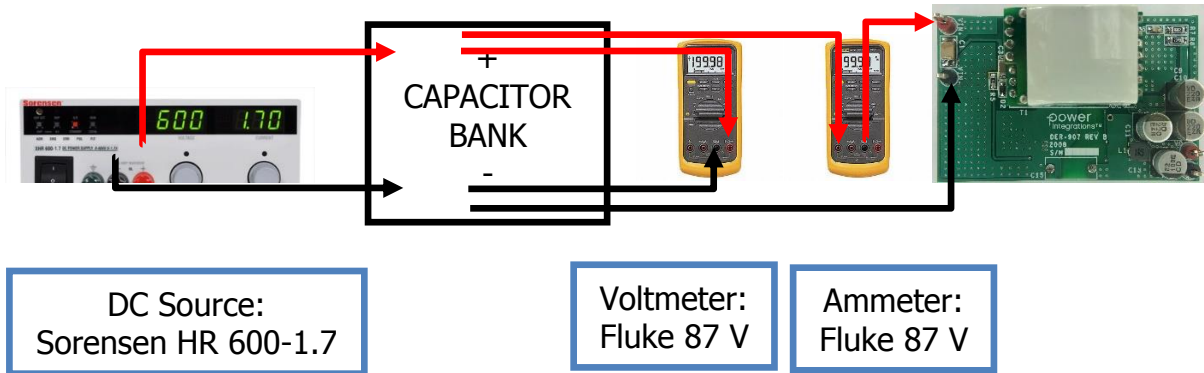
<b>Input: 400 VDC; Output: 12 V / 1.67 A (20 W)</b>					
<b>Load (%)</b>	<b>P<sub>IN</sub> (W)</b>	<b>V<sub>OUT</sub> (V)</b>	<b>I<sub>OUT</sub> (A)</b>	<b>P<sub>OUT</sub> (W)</b>	<b>Efficiency (%)</b>
100	23.95	12.10	1.67	20.20	84.34
75	17.99	12.08	1.25	15.12	84.04
50	12.08	12.05	0.84	10.07	83.37
25	6.20	12.01	0.42	5.01	80.95

## 8.1.5 550 VDC, 12 V 1.67 A (20 W)

<b>Input: 550 VDC; Output: 12 V / 1.67 A (20 W)</b>					
<b>Load (%)</b>	<b>P<sub>IN</sub> (W)</b>	<b>V<sub>OUT</sub> (V)</b>	<b>I<sub>OUT</sub> (A)</b>	<b>P<sub>OUT</sub> (W)</b>	<b>Efficiency (%)</b>
100	24.81	12.16	1.67	20.29	81.81
75	18.62	12.11	1.25	15.16	81.41
50	12.56	12.07	0.84	10.09	80.32
25	6.56	12.01	0.42	5.01	76.40

## 8.2 No-Load Input Power

### 8.2.1 Test Set-up



### 8.2.2 Test Data

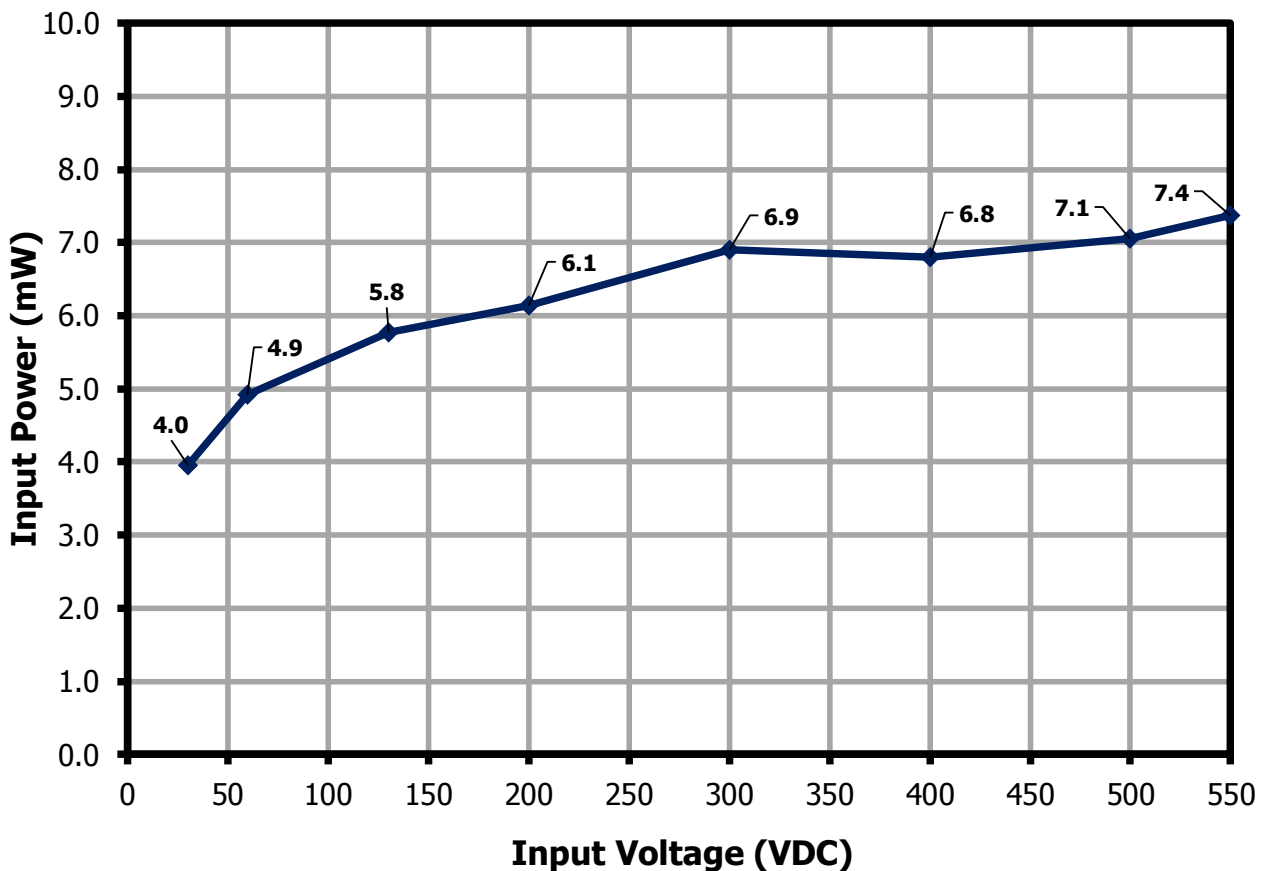


Figure 9 – No Load Input Power vs. Input Voltage at Room Temperature.



### 8.3 Full Load Efficiency vs. Input Voltage

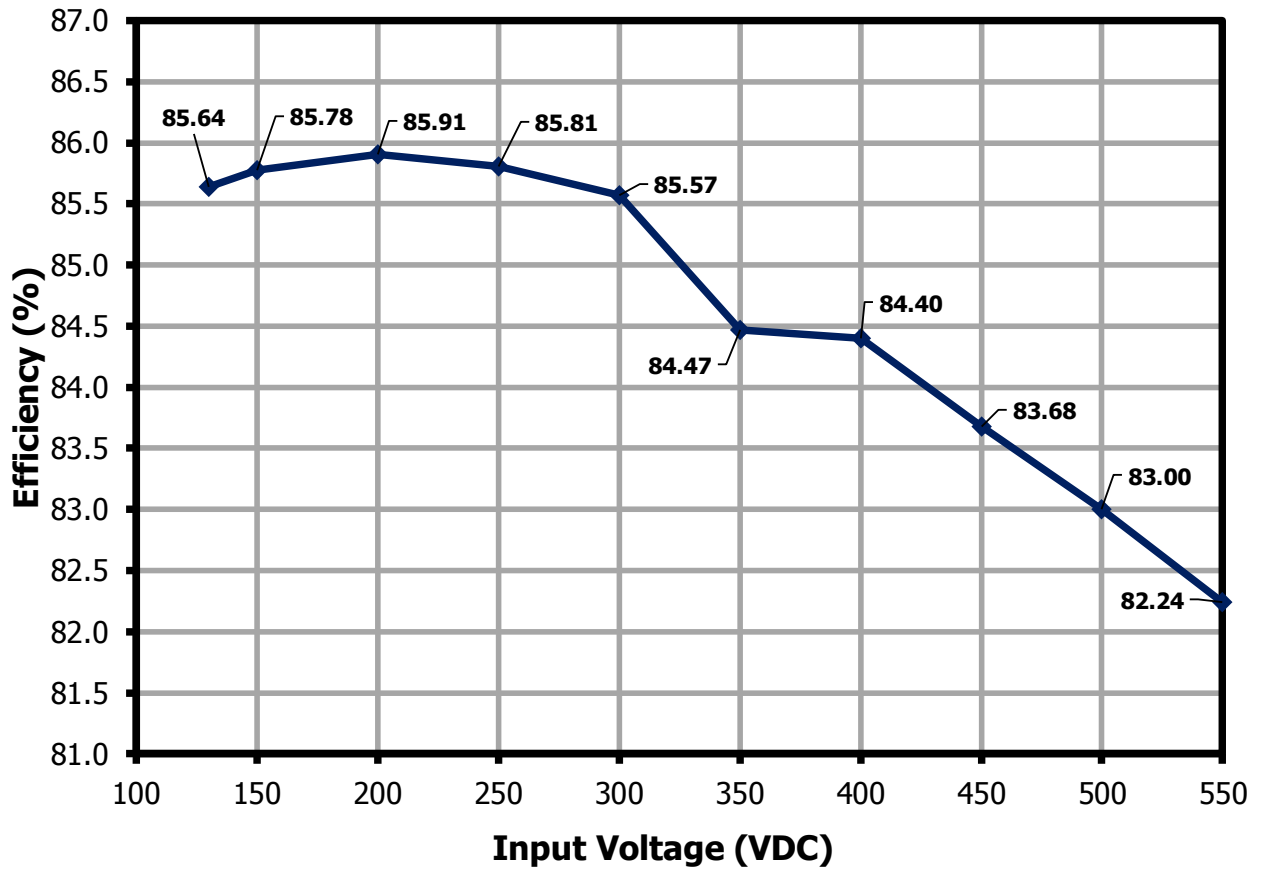


Figure 10 – Full Load Efficiency vs. Input Voltage at Room Temperature.



### 8.4 Efficiency vs. Load

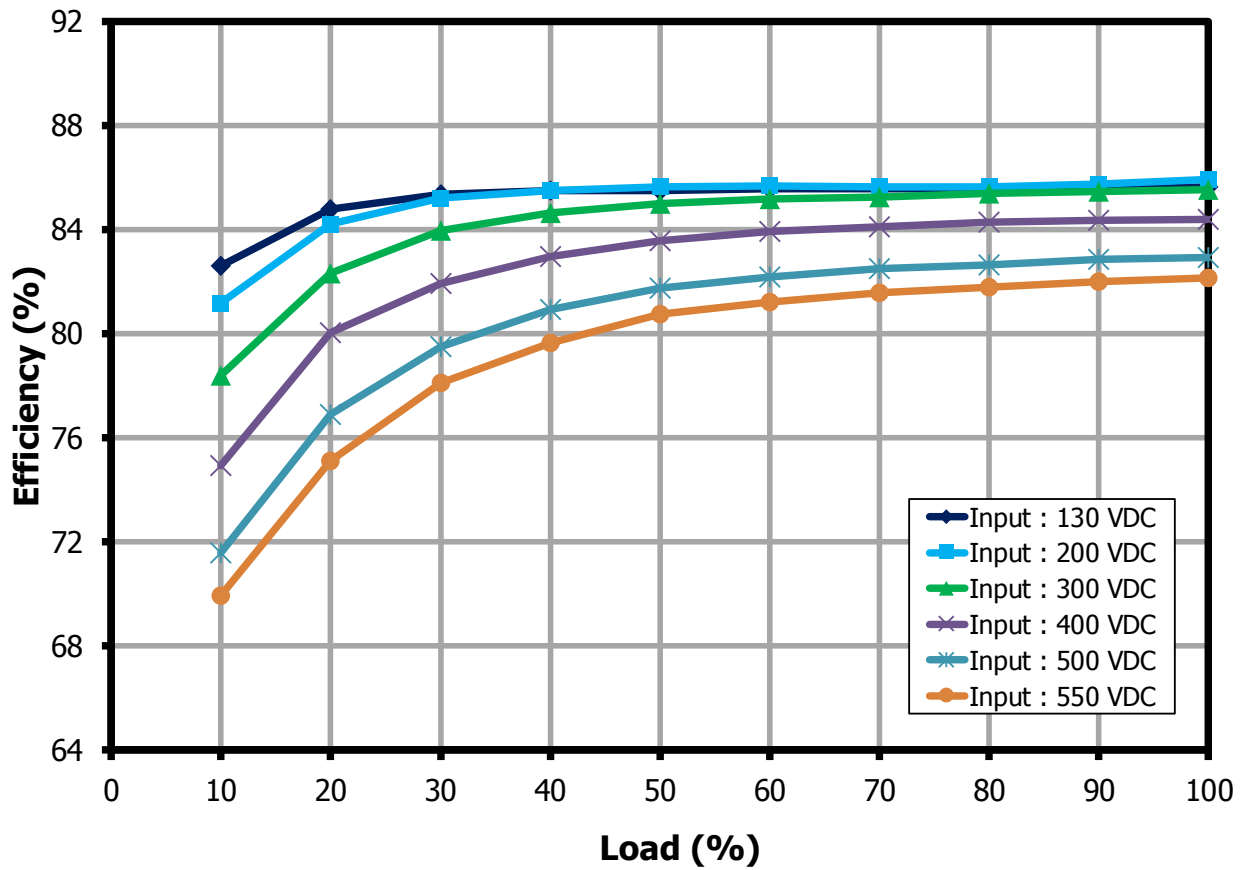


Figure 11 – Efficiency vs Load, Room Temperature.



### 8.5 Output Voltage Regulation

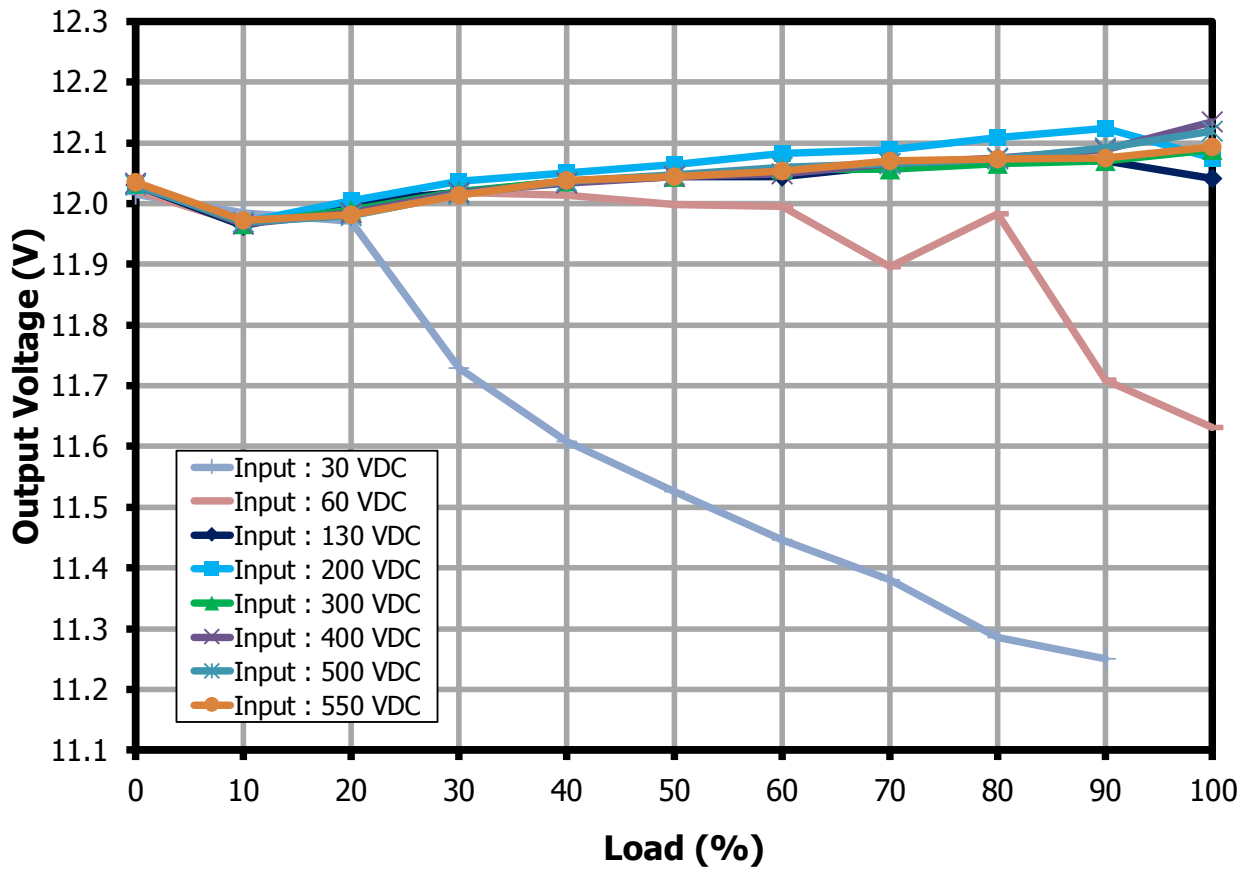


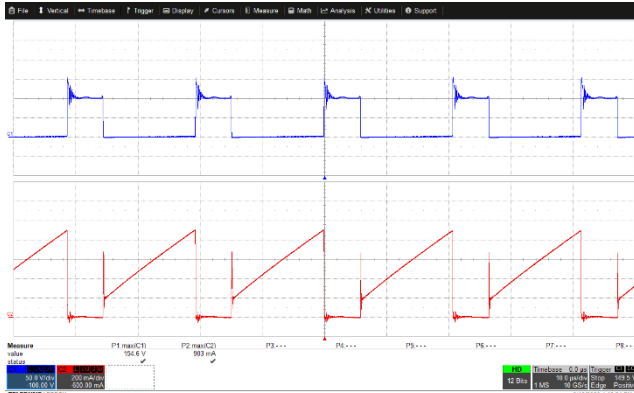
Figure 12 – Output Voltage Regulation, Room Temperature.



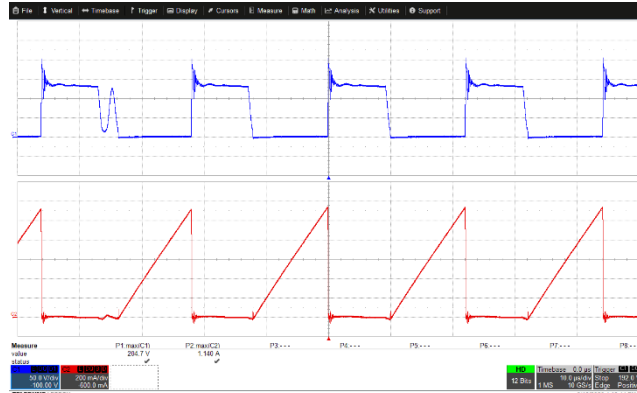
## 9 Waveforms

### 9.1 Switching Waveforms at 20 W

#### 9.1.1 InnoSwitch Drain Voltage and Current, Steady-State



**Figure 13 – Drain Voltage and Current.**  
 $V_{IN} = 30 \text{ VDC}$ ,  $I_{OUT} = 0.833 \text{ A}$ .  
**CH1:**  $V_{DRAIN-SOURCE}$ , 50 V, 10  $\mu\text{s}$  / div.  
**CH2:**  $I_{DRAIN}$ , 200 mA, 10  $\mu\text{s}$  / div.  
 $V_{DS(MAX)} = 154.6 \text{ V}$ ,  $I_{DRAIN(MAX)} = 903 \text{ mA}$ .  
 $V_{DS}$  derating: 20.61 %.



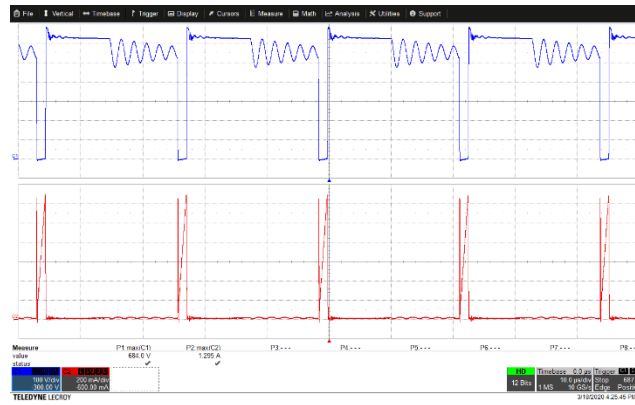
**Figure 14 – Drain Voltage and Current.**  
 $V_{IN} = 60 \text{ VDC}$ ,  $I_{OUT} = 1.25 \text{ A}$ .  
**CH1:**  $V_{DRAIN-SOURCE}$ , 50 V, 10  $\mu\text{s}$  / div.  
**CH2:**  $I_{DRAIN}$ , 200 mA, 10  $\mu\text{s}$  / div.  
 $V_{DS(MAX)} = 204.7 \text{ V}$ ,  $I_{DRAIN(MAX)} = 1.140 \text{ A}$ .  
 $V_{DS}$  derating: 27.29 %.



**Figure 15 – Drain Voltage and Current.**  
 $V_{IN} = 130 \text{ VDC}$ ,  $I_{OUT} = 1.67 \text{ A}$ .  
**CH1:**  $V_{DRAIN-SOURCE}$ , 50 V, 10  $\mu\text{s}$  / div.  
**CH2:**  $I_{DRAIN}$ , 200 mA, 10  $\mu\text{s}$  / div.  
 $V_{DS(MAX)} = 280.1 \text{ V}$ ,  $I_{DRAIN(MAX)} = 1.254 \text{ A}$ .  
 $V_{DS}$  derating: 37.35 %.



**Figure 16 – Drain Voltage and Current.**  
 $V_{IN} = 400 \text{ VDC}$ ,  $I_{OUT} = 1.67 \text{ A}$ .  
**CH1:**  $V_{DRAIN-SOURCE}$ , 100 V, 10  $\mu\text{s}$  / div.  
**CH2:**  $I_{DRAIN}$ , 200 mA, 10  $\mu\text{s}$  / div.  
 $V_{DS(MAX)} = 527.6 \text{ V}$ ,  $I_{DRAIN(MAX)} = 1.241 \text{ A}$ .  
 $V_{DS}$  derating: 70.35 %.



**Figure 17** – Drain Voltage and Current.

$V_{IN} = 550 \text{ VDC}$ ,  $I_{OUT} = 1.67 \text{ A}$ .

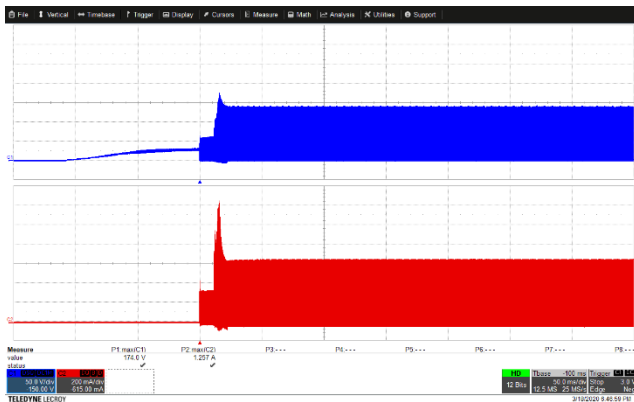
**CH1:**  $V_{DRAIN-SOURCE}$ , 100 V, 10  $\mu\text{s}$  / div.

**CH2:**  $I_{DRAIN}$ , 200 mA, 10  $\mu\text{s}$  / div.

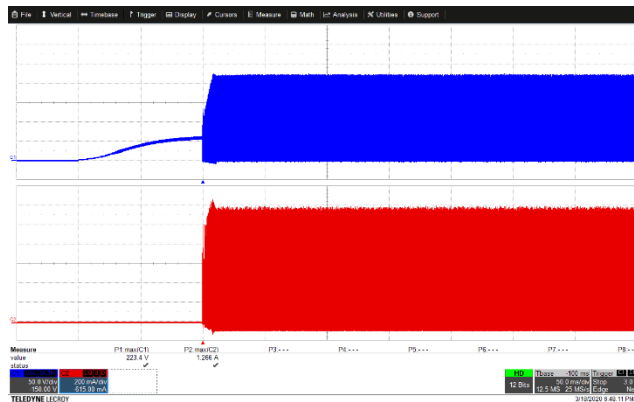
$V_{DS(MAX)} = 684 \text{ V}$ ,  $I_{DRAIN(MAX)} = 1.295 \text{ A}$ .

$V_{DS}$  derating: 91.2 %.

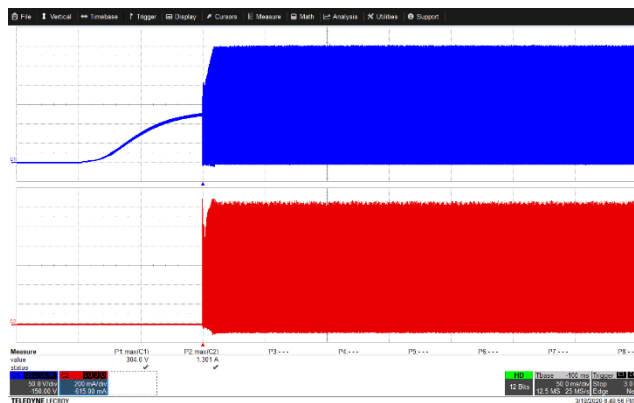
### 9.1.2 InnoSwitch Drain Voltage and Current, Start-up



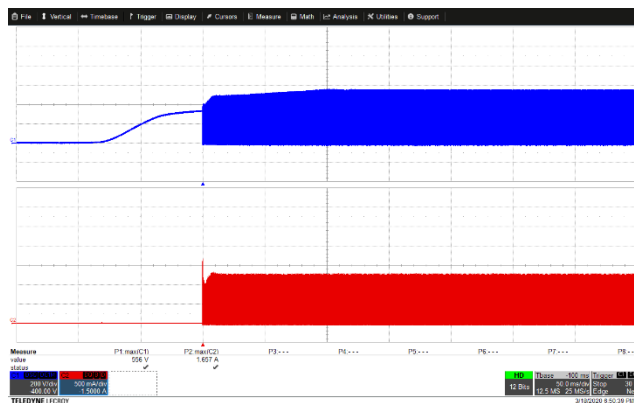
**Figure 18 – Drain Voltage and Current.**  
 $V_{IN} = 30 \text{ VDC}$ ,  $I_{OUT} = 0.5 \text{ A}$ .  
**CH1:**  $V_{DRAIN-SOURCE}$ , 50 V, 50 ms / div.  
**CH2:**  $I_{DRAIN}$ , 200 mA, 50 ms / div.  
 $V_{DS(MAX)} = 174 \text{ V}$ ,  $I_{DRAIN(MAX)} = 1.257 \text{ A}$ .  
 $V_{DS}$  derating: 23.2 %.



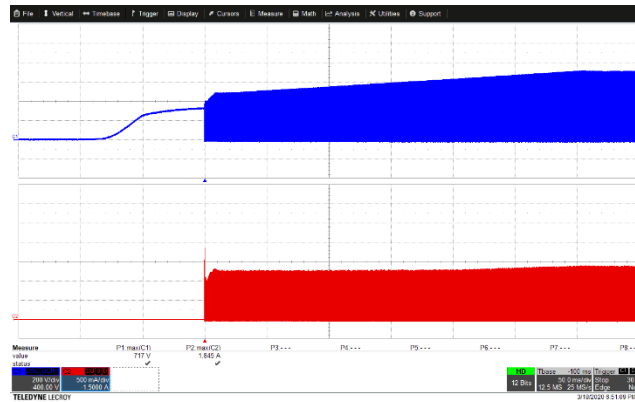
**Figure 19 – Drain Voltage and Current.**  
 $V_{IN} = 60 \text{ VDC}$ ,  $I_{OUT} = 1.25 \text{ A}$ .  
**CH1:**  $V_{DRAIN-SOURCE}$ , 50 V, 50 ms / div.  
**CH2:**  $I_{DRAIN}$ , 200 mA, 50 ms / div.  
 $V_{DS(MAX)} = 223.4 \text{ V}$ ,  $I_{DRAIN(MAX)} = 1.266 \text{ A}$ .  
 $V_{DS}$  derating: 29.79 %.



**Figure 20 – Drain Voltage and Current.**  
 $V_{IN} = 130 \text{ VDC}$ ,  $I_{OUT} = 1.67 \text{ A}$ .  
**CH1:**  $V_{DRAIN-SOURCE}$ , 50 V, 50 ms / div.  
**CH2:**  $I_{DRAIN}$ , 200 mA, 50 ms / div.  
 $V_{DS(MAX)} = 304 \text{ V}$ ,  $I_{DRAIN(MAX)} = 1.301 \text{ A}$ .  
 $V_{DS}$  derating: 40.53 %.



**Figure 21 – Drain Voltage and Current.**  
 $V_{IN} = 400 \text{ VDC}$ ,  $I_{OUT} = 1.25 \text{ A}$ .  
**CH1:**  $V_{DRAIN-SOURCE}$ , 200 V, 50 ms / div.  
**CH2:**  $I_{DRAIN}$ , 200 mA, 50 ms / div.  
 $V_{DS(MAX)} = 556 \text{ V}$ ,  $I_{DRAIN(MAX)} = 1.657 \text{ A}$ .  
 $V_{DS}$  derating: 74.13 %.



**Figure 22** – Drain Voltage and Current.

$V_{IN} = 550 \text{ VDC}$ ,  $I_{OUT} = 1.67 \text{ A}$ .

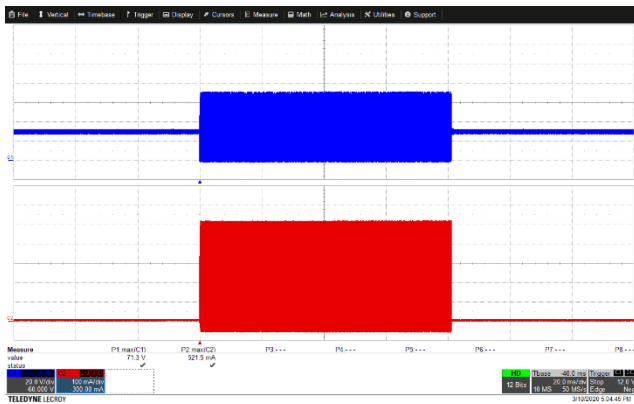
**CH1:**  $V_{DRAIN-SOURCE}$ , 200 V, 50 ms / div.

**CH2:**  $I_{DRAIN}$ , 500 mA, 50 ms / div.

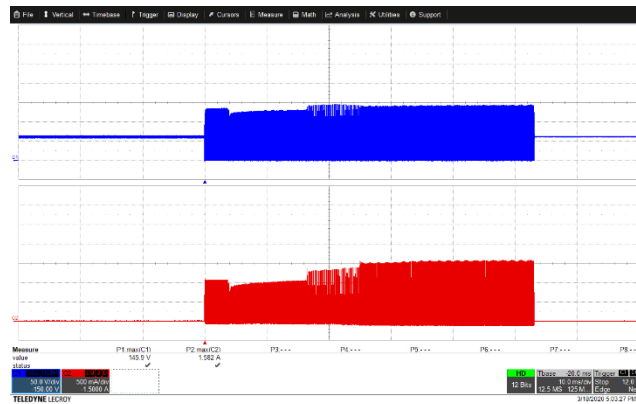
$V_{DS(MAX)} = 717 \text{ V}$ ,  $I_{DRAIN(MAX)} = 1.845 \text{ A}$ .

$V_{DS}$  derating: 95.6 %.

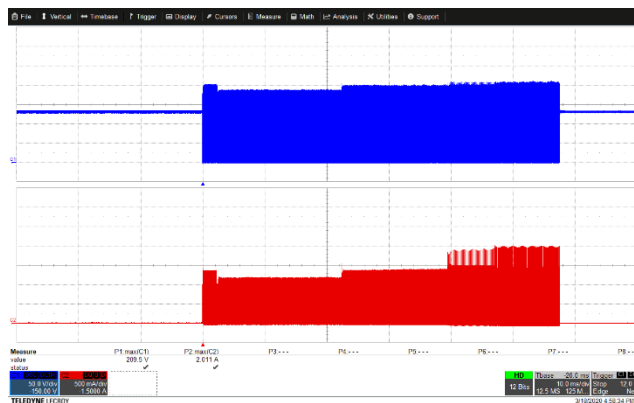
### 9.1.3 InnoSwitch Drain Voltage and Current, Output Shorted



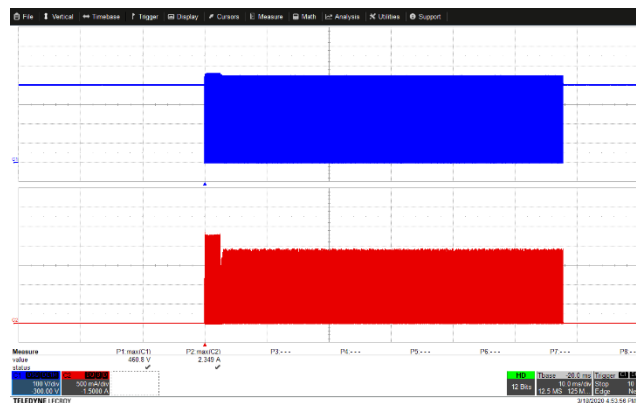
**Figure 23 – Drain Voltage and Current.**  
 $V_{IN} = 30 \text{ VDC}$ , Output Shorted.  
**CH1:**  $V_{DRAIN-SOURCE}$ , 20 V, 20 ms / div.  
**CH2:**  $I_{DRAIN}$ , 100 mA, 20 ms / div.  
 $V_{DS(MAX)} = 71.3 \text{ V}$ ,  $I_{DRAIN(MAX)} = 521.5 \text{ mA}$ .  
 $V_{DS}$  derating: 9.51 %.



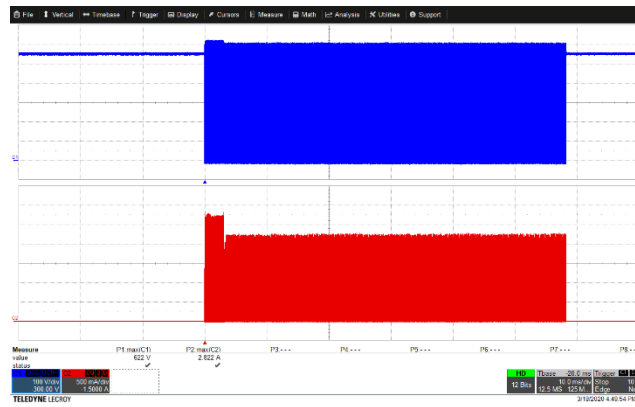
**Figure 24 – Drain Voltage and Current.**  
 $V_{IN} = 60 \text{ VDC}$ , Output Shorted.  
**CH1:**  $V_{DRAIN-SOURCE}$ , 50 V, 10 ms / div.  
**CH2:**  $I_{DRAIN}$ , 500 mA, 10 ms / div.  
 $V_{DS(MAX)} = 145.9 \text{ V}$ ,  $I_{DRAIN(MAX)} = 1.582 \text{ A}$ .  
 $V_{DS}$  derating: 19.45 %.



**Figure 25 – Drain Voltage and Current.**  
 $V_{IN} = 130 \text{ VDC}$ , Output Shorted.  
**CH1:**  $V_{DRAIN-SOURCE}$ , 50 V, 10 ms / div.  
**CH2:**  $I_{DRAIN}$ , 500 mA, 10 ms / div.  
 $V_{DS(MAX)} = 209.5 \text{ V}$ ,  $I_{DRAIN(MAX)} = 2.011 \text{ A}$ .  
 $V_{DS}$  derating: 27.93 %.



**Figure 26 – Drain Voltage and Current.**  
 $V_{IN} = 400 \text{ VDC}$ , Output Shorted.  
**CH1:**  $V_{DRAIN-SOURCE}$ , 100 V, 10 ms / div.  
**CH2:**  $I_{DRAIN}$ , 500 mA, 10 ms / div.  
 $V_{DS(MAX)} = 460.8 \text{ V}$ ,  $I_{DRAIN(MAX)} = 2.349 \text{ A}$ .  
 $V_{DS}$  derating: 61.44 %.



**Figure 27** – Drain Voltage and Current.

$V_{IN} = 550$  VDC, Output Shorted.

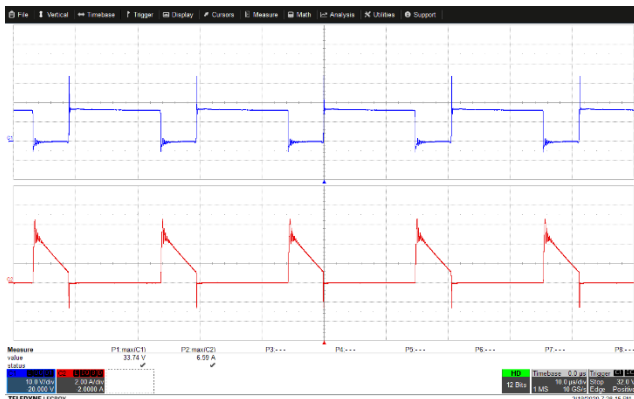
CH1:  $V_{DRAIN-SOURCE}$ , 100 V, 10 ms / div.

CH2:  $I_{DRAIN}$ , 500 mA, 10 ms / div.

$V_{DS(MAX)} = 622$  V,  $I_{DRAIN(MAX)} = 2.822$  A.

$V_{DS}$  derating: 82.93 %.

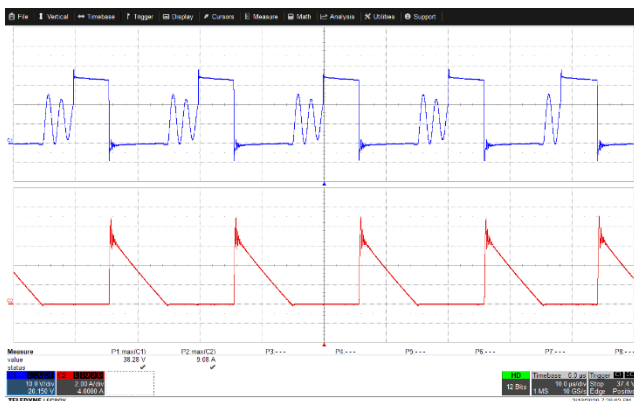
9.1.4 SR FET Waveforms, Steady-State



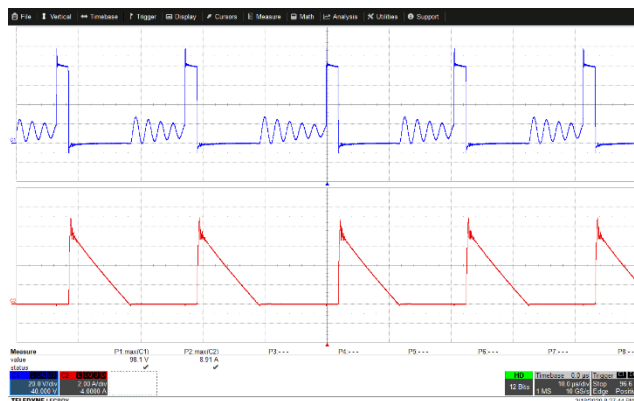
**Figure 28 – Drain Voltage and Current.**  
 $V_{IN} = 30 \text{ VDC}$ ,  $I_{OUT} = 0.833 \text{ A}$ .  
**CH1:**  $V_{DRAIN-SOURCE}$ , 10 V, 10  $\mu\text{s}$  / div.  
**CH2:**  $I_{DRAIN}$ , 2 A, 10  $\mu\text{s}$  / div.  
 $V_{DS(MAX)} = 33.74 \text{ V}$ ,  $I_{DRAIN(MAX)} = 6.59 \text{ A}$ .  
 $V_{DS}$  derating: 16.87 %.



**Figure 29 – Drain Voltage and Current.**  
 $V_{IN} = 60 \text{ VDC}$ ,  $I_{OUT} = 1.25 \text{ A}$ .  
**CH1:**  $V_{DRAIN-SOURCE}$ , 10 V, 10  $\mu\text{s}$  / div.  
**CH2:**  $I_{DRAIN}$ , 2 A, 10  $\mu\text{s}$  / div.  
 $V_{DS(MAX)} = 23.29 \text{ V}$ ,  $I_{DRAIN(MAX)} = 8.26 \text{ A}$ .  
 $V_{DS}$  derating: 11.64 %.

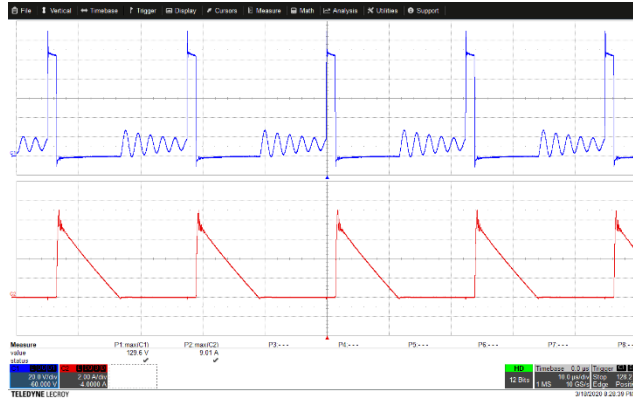


**Figure 30 – Drain Voltage and Current.**  
 $V_{IN} = 130 \text{ VDC}$ ,  $I_{OUT} = 1.67 \text{ A}$ .  
**CH1:**  $V_{DRAIN-SOURCE}$ , 10 V, 10  $\mu\text{s}$  / div.  
**CH2:**  $I_{DRAIN}$ , 2 A, 10  $\mu\text{s}$  / div.  
 $V_{DS(MAX)} = 38.28 \text{ V}$ ,  $I_{DRAIN(MAX)} = 9.08 \text{ A}$ .  
 $V_{DS}$  derating: 19.14 %.



**Figure 31 – Drain Voltage and Current.**  
 $V_{IN} = 400 \text{ VDC}$ ,  $I_{OUT} = 1.67 \text{ A}$ .  
**CH1:**  $V_{DRAIN-SOURCE}$ , 20 V, 10  $\mu\text{s}$  / div.  
**CH2:**  $I_{DRAIN}$ , 2 A, 10  $\mu\text{s}$  / div.  
 $V_{DS(MAX)} = 98.1 \text{ V}$ ,  $I_{DRAIN(MAX)} = 8.91 \text{ A}$ .  
 $V_{DS}$  derating: 49.05 %.





**Figure 32** – Drain Voltage and Current.

$V_{IN} = 550 \text{ VDC}$ ,  $I_{OUT} = 1.67 \text{ A}$ .

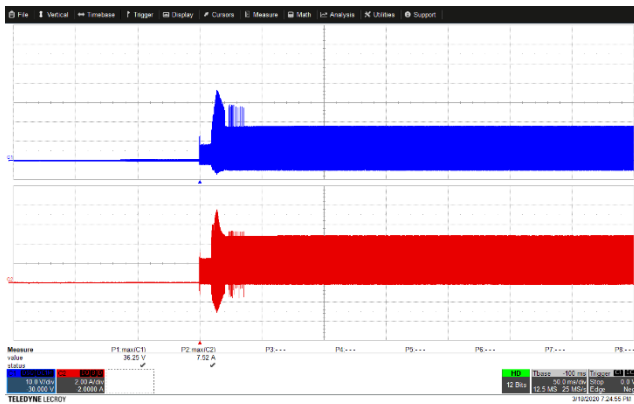
**CH1:**  $V_{DRAIN-SOURCE}$ , 20 V, 10  $\mu\text{s}$  / div.

**CH2:**  $I_{DRAIN}$ , 2 A, 10  $\mu\text{s}$  / div.

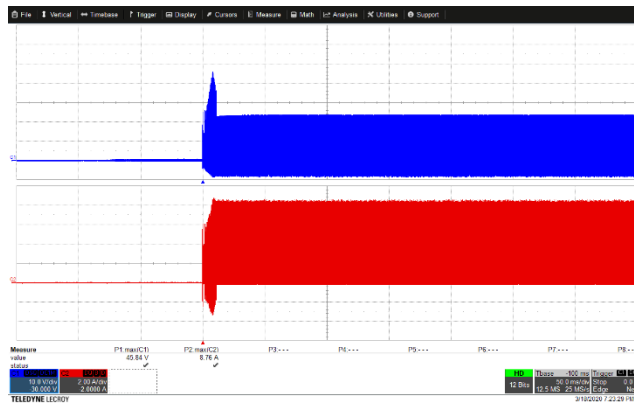
$V_{DS(MAX)} = 129.6 \text{ V}$ ,  $I_{DRAIN(MAX)} = 9.01 \text{ A}$ .

$V_{DS}$  derating: 64.8 %.

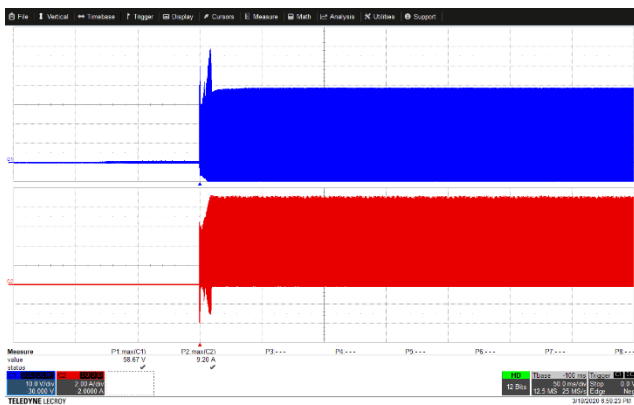
### 9.1.5 SR FET Waveforms, Start-Up



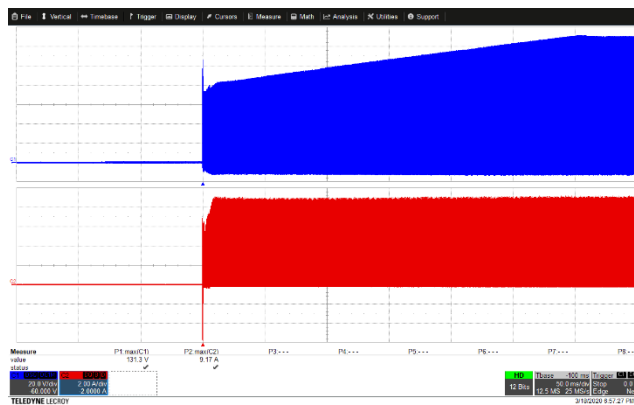
**Figure 33 – Drain Voltage and Current.**  
 $V_{IN} = 30 \text{ VDC}$ ,  $I_{OUT} = 0.5 \text{ A}$ .  
**CH1:**  $V_{DRAIN-SOURCE}$ , 10 V, 50 ms / div.  
**CH2:**  $I_{DRAIN}$ , 2 A, 50 ms / div.  
 $V_{DS(MAX)} = 36.25 \text{ V}$ ,  $I_{DRAIN(MAX)} = 7.52 \text{ A}$ .  
 $V_{DS}$  derating: 18.13 %.



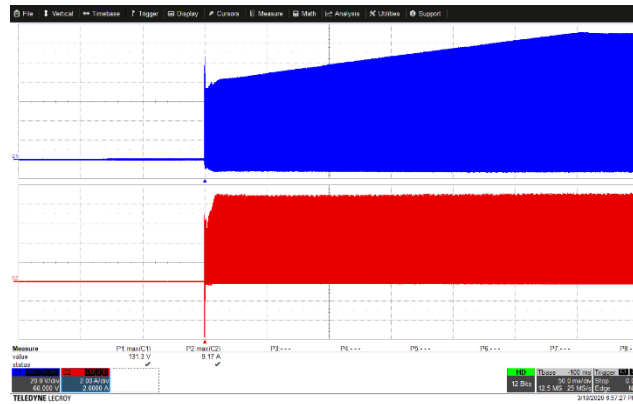
**Figure 34 – Drain Voltage and Current.**  
 $V_{IN} = 60 \text{ VDC}$ ,  $I_{OUT} = 1.25 \text{ A}$ .  
**CH1:**  $V_{DRAIN-SOURCE}$ , 10 V, 50 ms / div.  
**CH2:**  $I_{DRAIN}$ , 2 A, 50 ms / div.  
 $V_{DS(MAX)} = 45.84 \text{ V}$ ,  $I_{DRAIN(MAX)} = 8.76 \text{ A}$ .  
 $V_{DS}$  derating: 22.92 %.



**Figure 35 – Drain Voltage and Current.**  
 $V_{IN} = 130 \text{ VDC}$ ,  $I_{OUT} = 1.67 \text{ A}$ .  
**CH1:**  $V_{DRAIN-SOURCE}$ , 10 V, 50 ms / div.  
**CH2:**  $I_{DRAIN}$ , 2 A, 50 ms / div.  
 $V_{DS(MAX)} = 58.67 \text{ V}$ ,  $I_{DRAIN(MAX)} = 9.20 \text{ A}$ .  
 $V_{DS}$  derating: 29.34 %.



**Figure 36 – Drain Voltage and Current.**  
 $V_{IN} = 400 \text{ VDC}$ ,  $I_{OUT} = 1.67 \text{ A}$ .  
**CH1:**  $V_{DRAIN-SOURCE}$ , 20 V, 50 ms / div.  
**CH2:**  $I_{DRAIN}$ , 2 A, 50 ms / div.  
 $V_{DS(MAX)} = 107.6 \text{ V}$ ,  $I_{DRAIN(MAX)} = 9.08 \text{ A}$ .  
 $V_{DS}$  derating: 53.8 %.



**Figure 37** – Drain Voltage and Current.

$V_{IN} = 550 \text{ VDC}$ ,  $I_{OUT} = 1.67 \text{ A}$ .

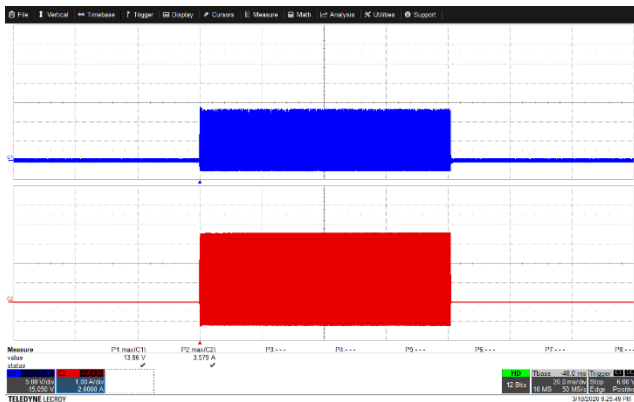
**CH1:**  $V_{DRAIN-SOURCE}$ , 20 V, 50 ms / div.

**CH2:**  $I_{DRAIN}$ , 2 A, 50 ms / div.

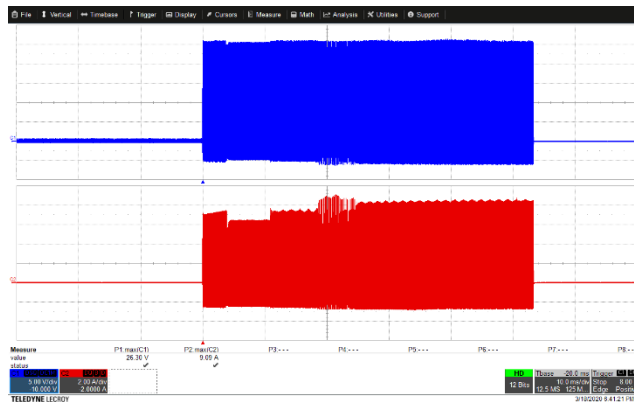
$V_{DS(MAX)} = 131.3 \text{ V}$ ,  $I_{DRAIN(MAX)} = 9.17 \text{ A}$ .

$V_{DS}$  derating: 65.65 %.

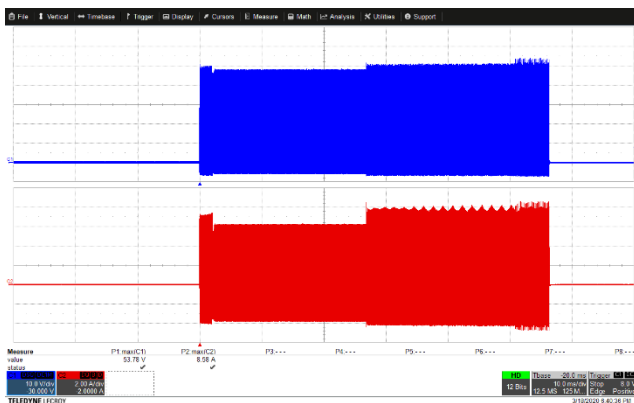
9.1.6 SR FET Waveforms, Output Shorted



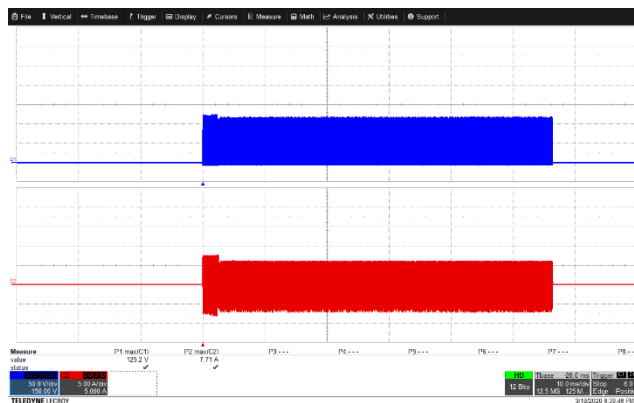
**Figure 38** – Drain Voltage and Current.  
 $V_{IN} = 30$  VDC, Output Shorted.  
 CH1:  $V_{DRAIN-SOURCE}$ , 5 V, 20 ms / div.  
 CH2:  $I_{DRAIN}$ , 1 A, 20 ms / div.  
 $V_{DS(MAX)} = 13.86$  V,  $I_{DRAIN(MAX)} = 3.579$  A.  
 $V_{DS}$  derating: 6.93 %.



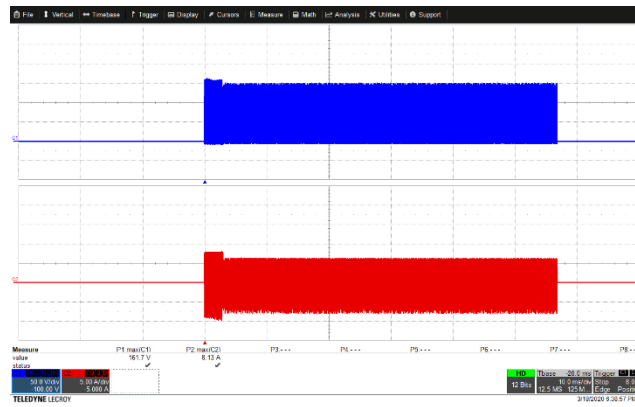
**Figure 39** – Drain Voltage and Current.  
 $V_{IN} = 60$  VDC, Output Shorted.  
 CH1:  $V_{DRAIN-SOURCE}$ , 5 V, 10 ms / div.  
 CH2:  $I_{DRAIN}$ , 2 A, 10 ms / div.  
 $V_{DS(MAX)} = 26.30$  V,  $I_{DRAIN(MAX)} = 9.09$  A.  
 $V_{DS}$  derating: 13.15 %.



**Figure 40** – Drain Voltage and Current.  
 $V_{IN} = 130$  VDC, Output Shorted.  
 CH1:  $V_{DRAIN-SOURCE}$ , 10 V, 10 ms / div.  
 CH2:  $I_{DRAIN}$ , 2 A, 10 ms / div.  
 $V_{DS(MAX)} = 53.78$  V,  $I_{DRAIN(MAX)} = 8.58$  A.  
 $V_{DS}$  derating: 26.89 %.



**Figure 41** – Drain Voltage and Current.  
 $V_{IN} = 400$  VDC, Output Shorted.  
 CH1:  $V_{DRAIN-SOURCE}$ , 50 V, 10 ms / div.  
 CH2:  $I_{DRAIN}$ , 5 A, 10 ms / div.  
 $V_{DS(MAX)} = 125.2$  V,  $I_{DRAIN(MAX)} = 7.71$  A.  
 $V_{DS}$  derating: 62.6 %.



**Figure 42** – Drain Voltage and Current.

$V_{IN} = 550 \text{ VDC}$ ,  $I_{OUT} = \text{Output Shorted}$ .

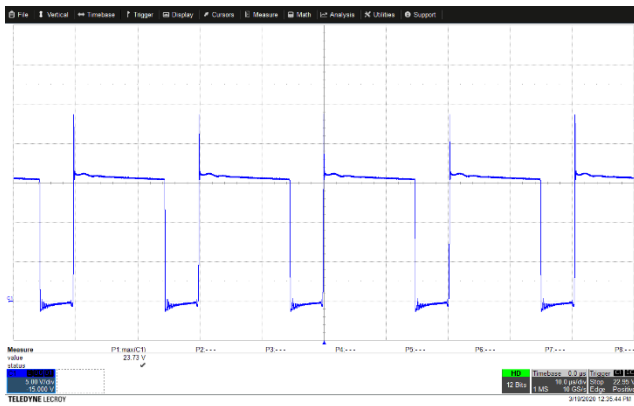
**CH1:**  $V_{DRAIN-SOURCE}$ , 50 V, 10 ms / div.

**CH2:**  $I_{DRAIN}$ , 5 A, 10 ms / div.

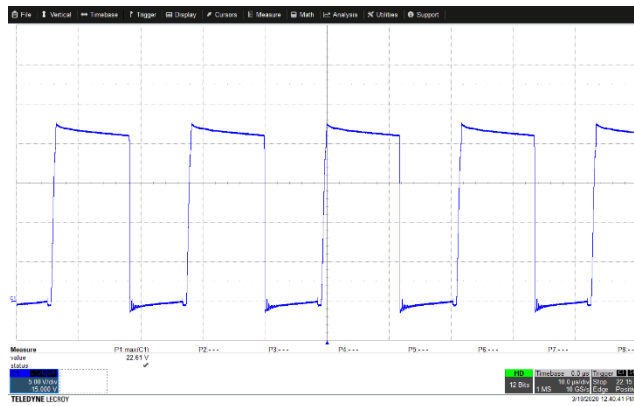
$V_{DS(MAX)} = 161.7 \text{ V}$ ,  $I_{DRAIN(MAX)} = 8.13 \text{ A}$ .

$V_{DS}$  derating: 80.85 %.

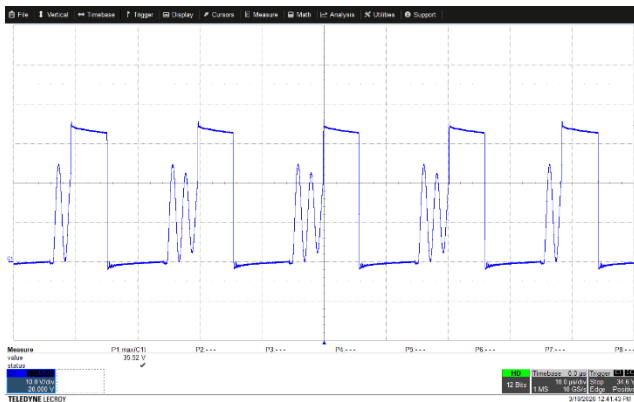
### 9.1.7 FWD Pin Waveform, Steady-State



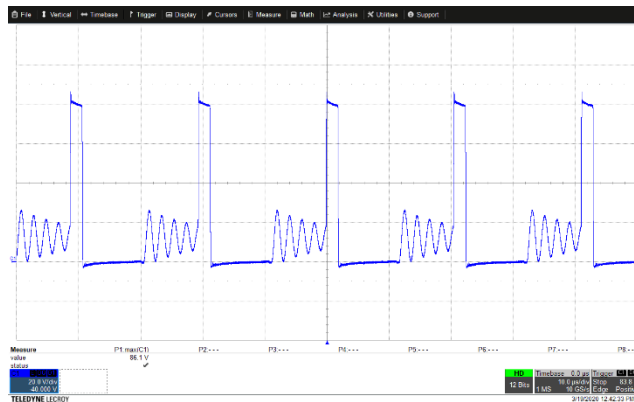
**Figure 43 – FWD Pin Voltage.**  
 $V_{IN} = 30 \text{ VDC}, I_{OUT} = 0.833 \text{ A}.$   
**CH1:**  $V_{FWD}, 5 \text{ V}, 10 \mu\text{s} / \text{div}.$   
 $V_{FWD(\text{MAX})} = 23.73 \text{ V} (<150 \text{ V}).$



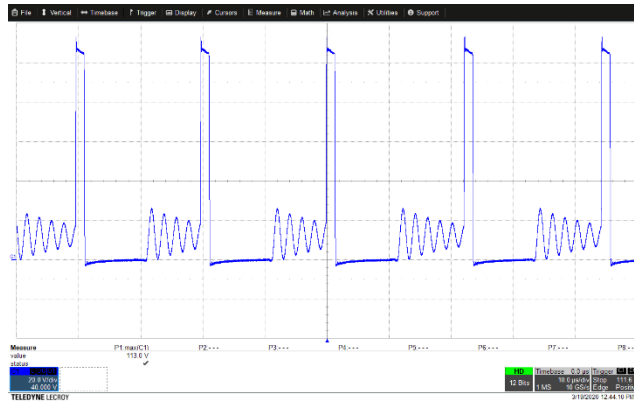
**Figure 44 – FWD Pin Voltage.**  
 $V_{IN} = 60 \text{ VDC}, I_{OUT} = 1.25 \text{ A}.$   
**CH1:**  $V_{FWD}, 5 \text{ V}, 10 \mu\text{s} / \text{div}.$   
 $V_{FWD(\text{MAX})} = 22.61 \text{ V} (<150 \text{ V}).$



**Figure 45 – FWD Pin Voltage.**  
 $V_{IN} = 130 \text{ VDC}, I_{OUT} = 1.67 \text{ A}.$   
**CH1:**  $V_{FWD}, 10 \text{ V}, 10 \mu\text{s} / \text{div}.$   
 $V_{FWD(\text{MAX})} = 35.52 \text{ V} (<150 \text{ V}).$



**Figure 46 – FWD Pin Voltage.**  
 $V_{IN} = 400 \text{ VDC}, I_{OUT} = 1.67 \text{ A}.$   
**CH1:**  $V_{FWD}, 20 \text{ V}, 10 \mu\text{s} / \text{div}.$   
 $V_{FWD(\text{MAX})} = 86.1 \text{ V} (<150 \text{ V}).$



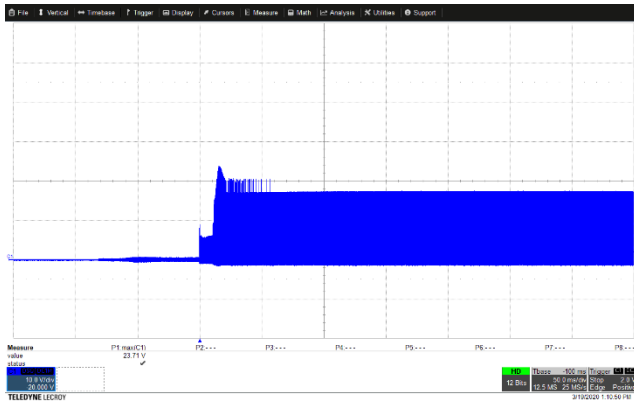
**Figure 47** – FWD Pin Voltage.

$V_{IN} = 550 \text{ VDC}$ ,  $I_{OUT} = 1.67 \text{ A}$ .

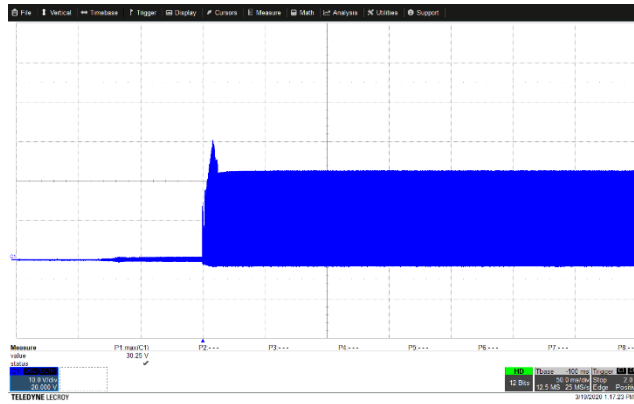
**CH1:**  $V_{FWD}$ , 20 V, 10  $\mu\text{s}$  / div.

$V_{FWD(MAX)} = 113.0 \text{ V}$  (<150 V).

### 9.1.8 FWD Pin Waveform, Start-Up



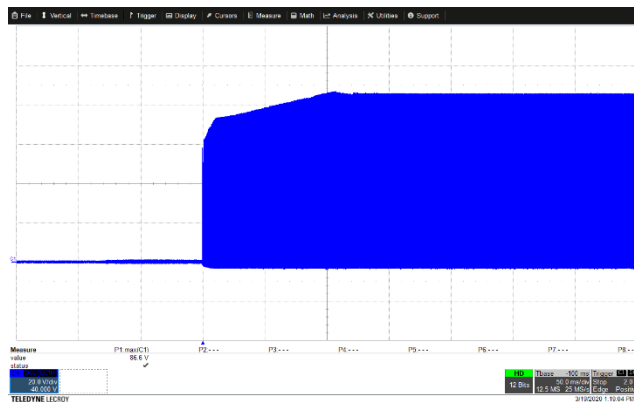
**Figure 48 – FWD Pin Voltage.**  
 $V_{IN} = 30 \text{ VDC}$ ,  $I_{OUT} = 0.5 \text{ A}$ .  
 CH1:  $V_{FWD}$ , 5 V, 50 ms / div.  
 $V_{FWD(MAX)} = 23.71 \text{ V} (<150 \text{ V})$ .



**Figure 49 – FWD Pin Voltage.**  
 $V_{IN} = 60 \text{ VDC}$ ,  $I_{OUT} = 1.25 \text{ A}$ .  
 CH1:  $V_{FWD}$ , 10 V, 50 ms / div.  
 $V_{FWD(MAX)} = 30.25 \text{ V} (<150 \text{ V})$ .

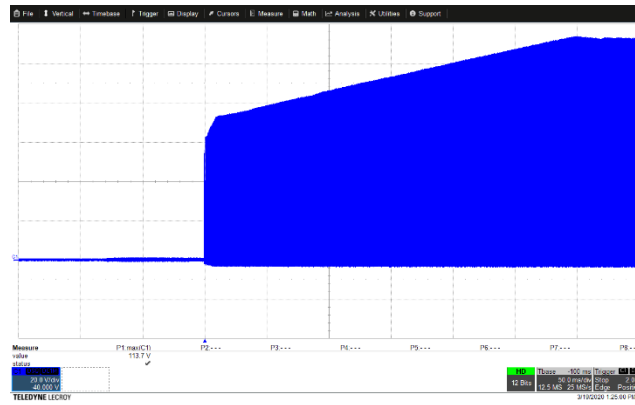


**Figure 50 – FWD Pin Voltage.**  
 $V_{IN} = 130 \text{ VDC}$ ,  $I_{OUT} = 1.67 \text{ A}$ .  
 CH1:  $V_{FWD}$ , 10 V, 50 ms / div.  
 $V_{FWD(MAX)} = 39.91 \text{ V} (<150 \text{ V})$ .



**Figure 51 – FWD Pin Voltage.**  
 $V_{IN} = 400 \text{ VDC}$ ,  $I_{OUT} = 1.67 \text{ A}$ .  
 CH1:  $V_{FWD}$ , 20 V, 50 ms / div.  
 $V_{FWD(MAX)} = 86.6 \text{ V} (<150 \text{ V})$ .





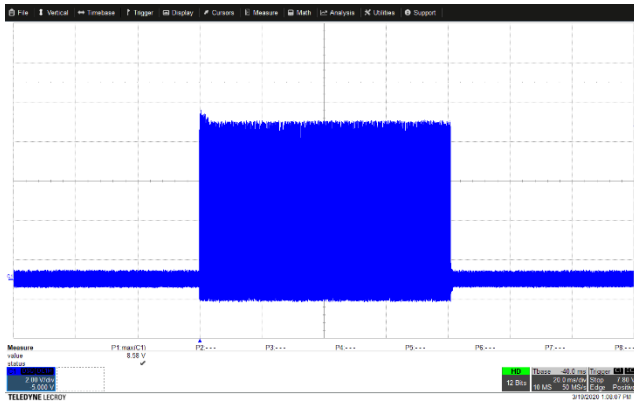
**Figure 52** – FWD Pin Voltage.

$V_{IN} = 550 \text{ VDC}$ ,  $I_{OUT} = 1.67 \text{ A}$ .

CH1:  $V_{FWD}$ , 20 V, 50 ms / div.

$V_{FWD(MAX)} = 113.7 \text{ V}$  (<150 V).

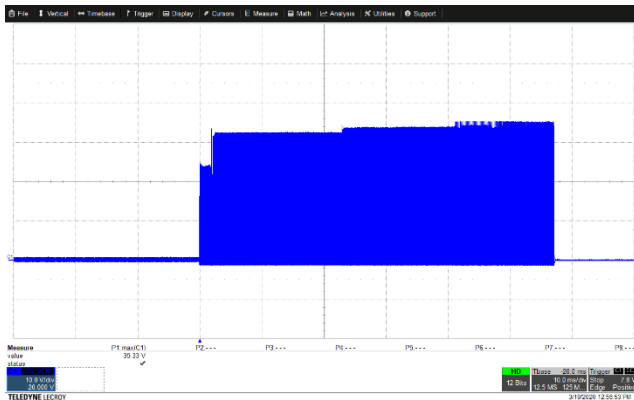
### 9.1.9 FWD Pin Waveform, Output Shorted



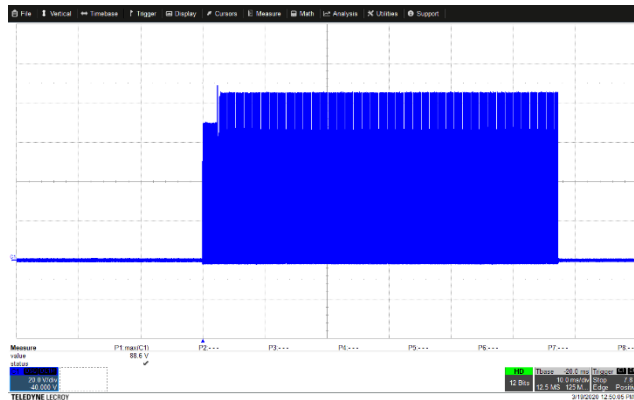
**Figure 53 – FWD Pin Voltage.**  
 $V_{IN} = 30 \text{ VDC}$ , Output Shorted.  
 CH1:  $V_{FWD}$ , 2 V, 20 ms / div.  
 $V_{FWD(MAX)} = 8.58 \text{ V} (<150 \text{ V})$ .



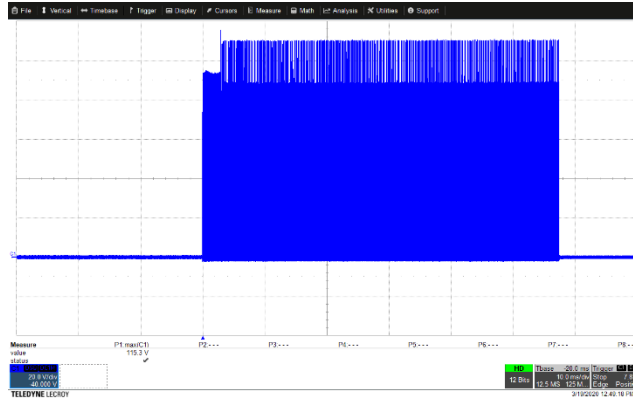
**Figure 54 – FWD Pin Voltage.**  
 $V_{IN} = 60 \text{ VDC}$ , Output Shorted.  
 CH1:  $V_{FWD}$ , 5 V, 10 ms / div.  
 $V_{FWD(MAX)} = 17.21 \text{ V} (<150 \text{ V})$ .



**Figure 55 – FWD Pin Voltage.**  
 $V_{IN} = 130 \text{ VDC}$ , Output Shorted.  
 CH1:  $V_{FWD}$ , 10 V, 10 ms / div.  
 $V_{FWD(MAX)} = 35.33 \text{ V} (<150 \text{ V})$ .



**Figure 56 – FWD Pin Voltage.**  
 $V_{IN} = 400 \text{ VDC}$ , Output Shorted.  
 CH1:  $V_{FWD}$ , 20 V, 10 ms / div.  
 $V_{FWD(MAX)} = 88.6 \text{ V} (<150 \text{ V})$ .



**Figure 57** – FWD Pin Voltage.

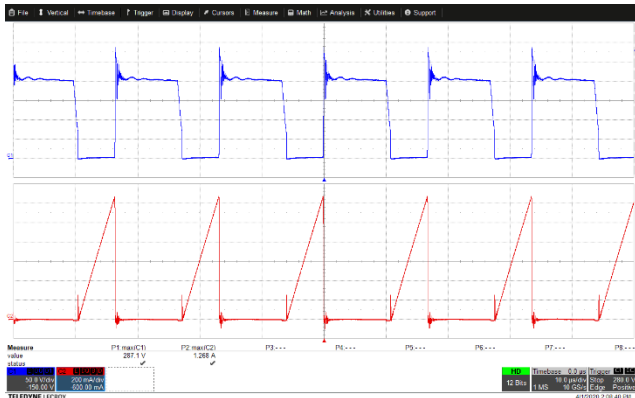
$V_{IN} = 550$  VDC, Output Shorted.

CH1:  $V_{FWD}$ , 20 V, 50 ms / div.

$V_{FWD(MAX)} = 115.3$  V (<150 V).

## 9.2 Switching Waveforms at 25 W Peak Power

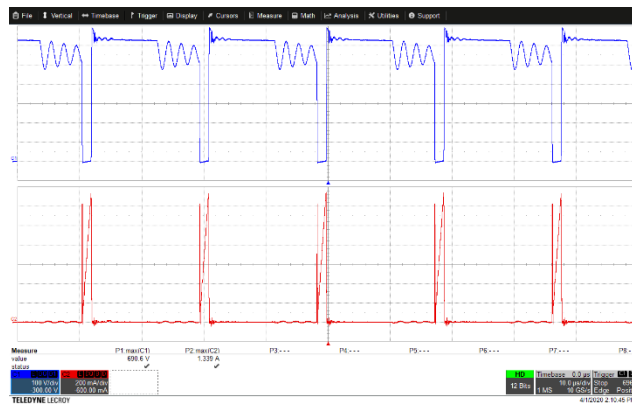
### 9.2.1 InnoSwitch Drain Voltage and Current, Steady-State



**Figure 58** – Drain Voltage and Current.  
 $V_{IN} = 130 \text{ VDC}$ ,  $I_{OUT} = 2.08 \text{ A}$ .  
**CH1:**  $V_{DRAIN-SOURCE}$ , 50 V, 10  $\mu\text{s}$  / div.  
**CH2:**  $I_{DRAIN}$ , 200 mA, 10  $\mu\text{s}$  / div.  
 $V_{DS(MAX)} = 287.1 \text{ V}$ ,  $I_{DRAIN(MAX)} = 1.268 \text{ A}$ .  
 $V_{DS}$  derating: 38.28 %.

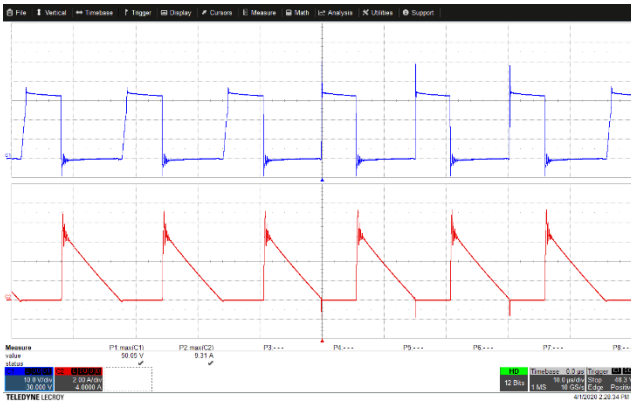


**Figure 59** – Drain Voltage and Current.  
 $V_{IN} = 400 \text{ VDC}$ ,  $I_{OUT} = 2.08 \text{ A}$ .  
**CH1:**  $V_{DRAIN-SOURCE}$ , 100 V, 10  $\mu\text{s}$  / div.  
**CH2:**  $I_{DRAIN}$ , 200 mA, 10  $\mu\text{s}$  / div.  
 $V_{DS(MAX)} = 537.1 \text{ V}$ ,  $I_{DRAIN(MAX)} = 1.307 \text{ A}$ .  
 $V_{DS}$  derating: 71.61 %.

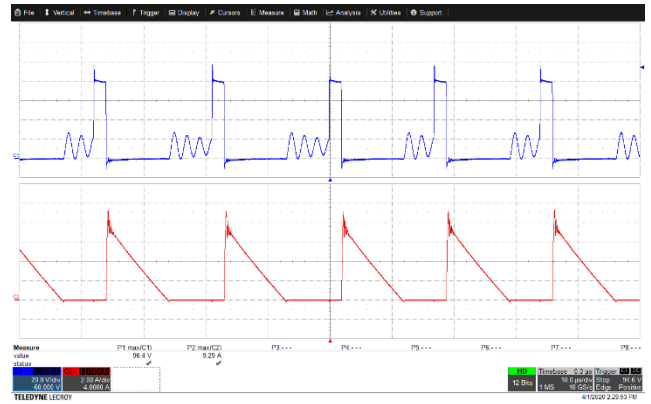


**Figure 60** – Drain Voltage and Current.  
 $V_{IN} = 550 \text{ VDC}$ ,  $I_{OUT} = 2.08 \text{ A}$ .  
**CH1:**  $V_{DRAIN-SOURCE}$ , 100 V, 10  $\mu\text{s}$  / div.  
**CH2:**  $I_{DRAIN}$ , 200 mA, 10  $\mu\text{s}$  / div.  
 $V_{DS(MAX)} = 690.6 \text{ V}$ ,  $I_{DRAIN(MAX)} = 1.339 \text{ A}$ .  
 $V_{DS}$  derating: 92.08 %.

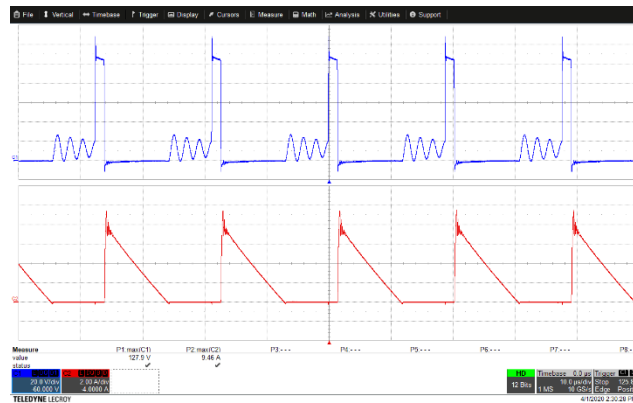
9.2.2 SRFET Drain Voltage and Current, Steady-State



**Figure 61 – Drain Voltage and Current.**  
 $V_{IN} = 130 \text{ VDC}$ ,  $I_{OUT} = 2.08 \text{ A}$ .  
**CH1:**  $V_{DRAIN-SOURCE}$ , 10 V, 10  $\mu\text{s}$  / div.  
**CH2:**  $I_{DRAIN}$ , 2 A, 10  $\mu\text{s}$  / div.  
 $V_{DS(MAX)} = 50.05 \text{ V}$ ,  $I_{DRAIN(MAX)} = 9.31 \text{ A}$ .  
 $V_{DS}$  derating: 25.03 %.



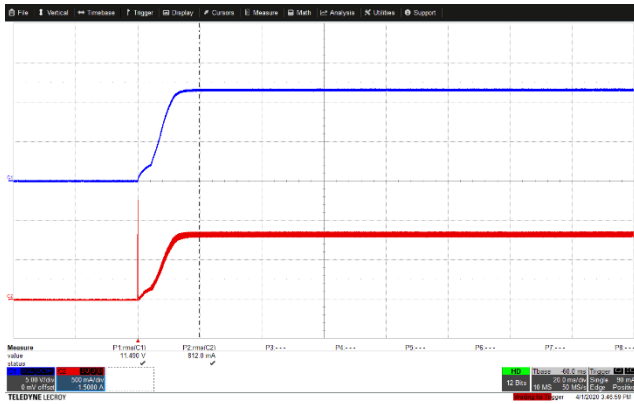
**Figure 62 – Drain Voltage and Current.**  
 $V_{IN} = 400 \text{ VDC}$ ,  $I_{OUT} = 2.08 \text{ A}$ .  
**CH1:**  $V_{DRAIN-SOURCE}$ , 20 V, 10  $\mu\text{s}$  / div.  
**CH2:**  $I_{DRAIN}$ , 2 A, 10  $\mu\text{s}$  / div.  
 $V_{DS(MAX)} = 96.4 \text{ V}$ ,  $I_{DRAIN(MAX)} = 9.29 \text{ A}$ .  
 $V_{DS}$  derating: 48.2 %.



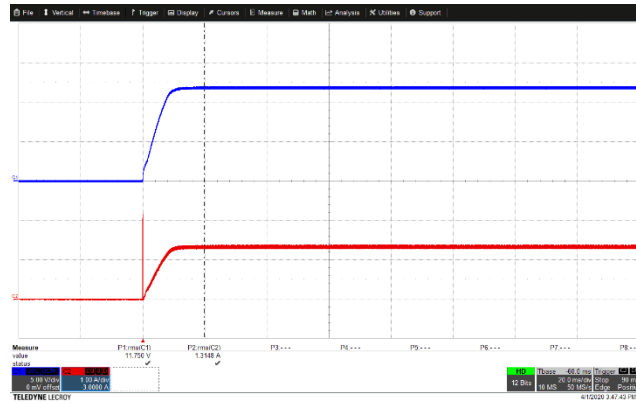
**Figure 63 – Drain Voltage and Current.**  
 $V_{IN} = 550 \text{ VDC}$ ,  $I_{OUT} = 2.08 \text{ A}$ .  
**CH1:**  $V_{DRAIN-SOURCE}$ , 1000 V, 10  $\mu\text{s}$  / div.  
**CH2:**  $I_{DRAIN}$ , 200 mA, 10  $\mu\text{s}$  / div.  
 $V_{DS(MAX)} = 127.9 \text{ V}$ ,  $I_{DRAIN(MAX)} = 9.46 \text{ A}$ .  
 $V_{DS}$  derating: 63.95 %.



### 9.3 Output Voltage and Current, Start-up CR Load



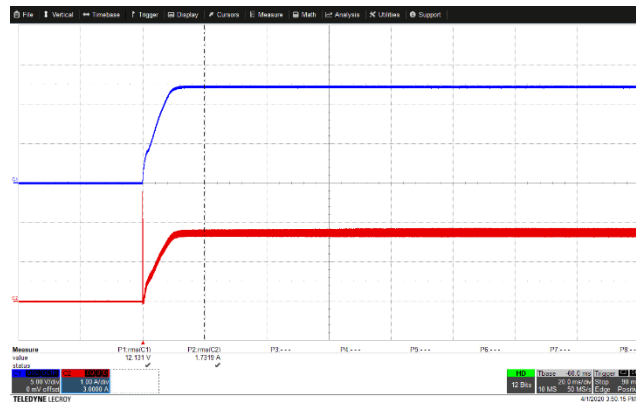
**Figure 64** – Output Voltage and Current.  
 $V_{IN} = 30$  VDC, Load =  $12.5 \Omega$ .  
 CH1:  $V_{OUTPUT}$ , 5 V, 20 ms / div.  
 CH2:  $I_{OUTPUT}$ , 500 mA, 20 ms / div.



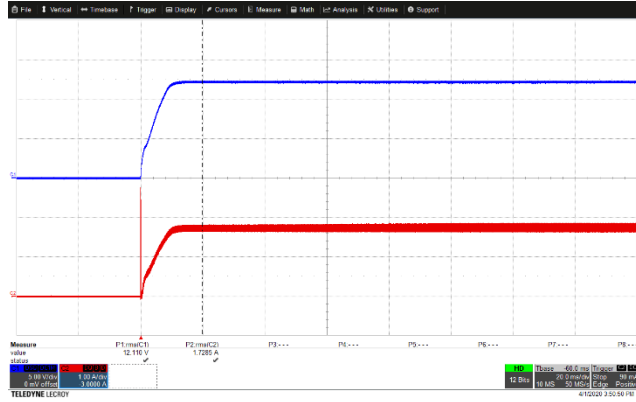
**Figure 65** – Output Voltage and Current.  
 $V_{IN} = 60$  VDC, Load =  $8.33 \Omega$ .  
 CH1:  $V_{OUTPUT}$ , 5 V, 20 ms / div.  
 CH2:  $I_{OUTPUT}$ , 1 A, 20 ms / div.



**Figure 66** – Output Voltage and Current.  
 $V_{IN} = 130$  VDC, Load =  $6.67 \Omega$ .  
 CH1:  $V_{OUTPUT}$ , 5 V, 20 ms / div.  
 CH2:  $I_{OUTPUT}$ , 1 A, 20 ms / div.



**Figure 67** – Output Voltage and Current.  
 $V_{IN} = 400$  VDC, Load =  $6.67 \Omega$ .  
 CH1:  $V_{OUTPUT}$ , 5 V, 20 ms / div.  
 CH2:  $I_{OUTPUT}$ , 1 A, 20 ms / div.



**Figure 68** – Output Voltage and Current.  
 $V_{IN} = 550$  VDC, Load =  $6.67 \Omega$ .  
CH1:  $V_{OUTPUT}$ , 5 V, 20 ms / div.  
CH2:  $I_{OUTPUT}$ , 1 A, 20 ms / div.

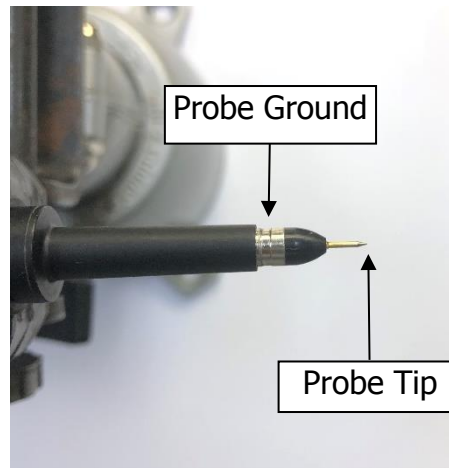


## 9.4 ***Output Ripple Measurements***

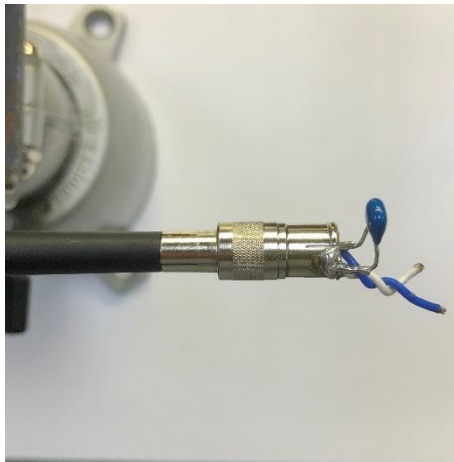
### 9.4.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The Teledyne Lecroy PP026 probe adapter is affixed with once capacitor tied in parallel across the probe tip. The capacitor include one (1) 1  $\mu$ F/50 V ceramic type.



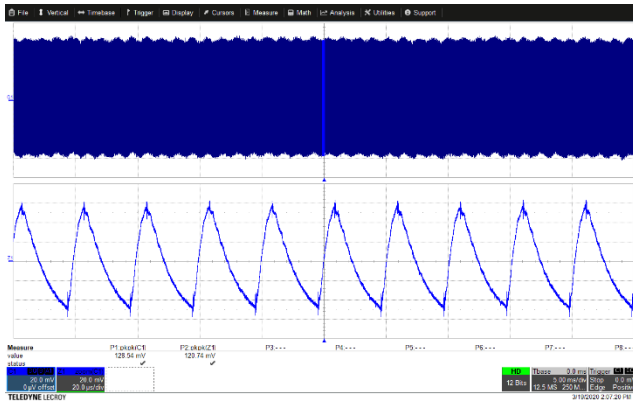
**Figure 69** – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)



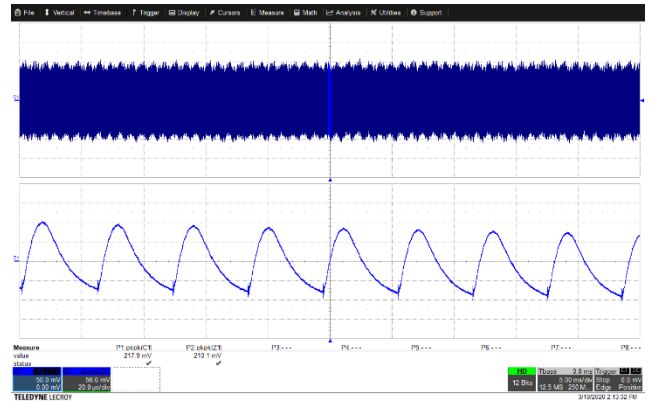
**Figure 70** – Oscilloscope Probe with BNC adapter.



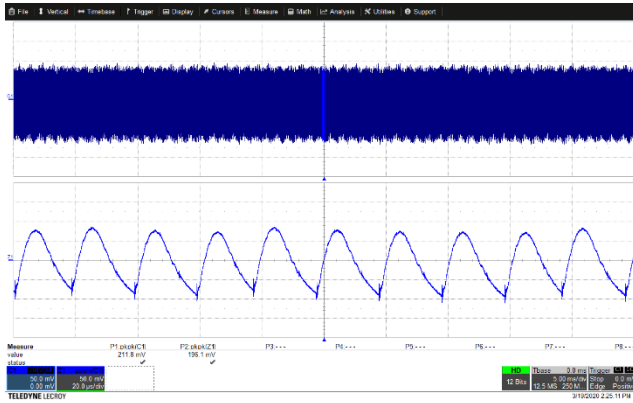
9.4.2 100% Loading Condition



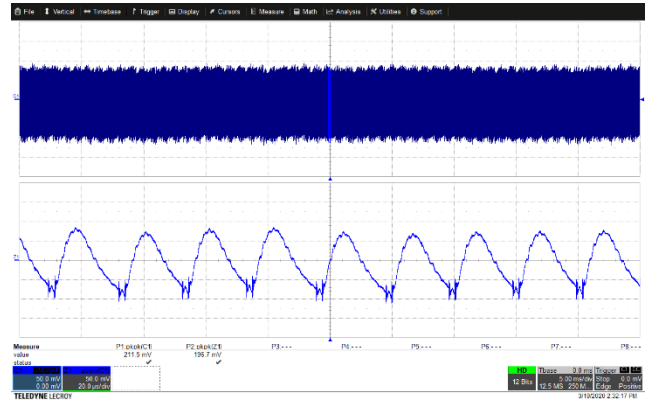
**Figure 71** – Output Voltage Ripple.  
 $V_{IN} = 30 \text{ VDC}$ ,  $I_{OUT} = 0.833 \text{ A}$ .  
 CH1:  $V_{OUT(mVpp)}$ , 20 mV, 5 ms / div.  
 Zoom: 20  $\mu\text{s}$  / div.  
 $V_{RIPPLE(PK-PK)} = 128.54 \text{ mV}_{pp}$ .



**Figure 72** – Output Voltage Ripple.  
 $V_{IN} = 60 \text{ VDC}$ ,  $I_{OUT} = 1.25 \text{ A}$ .  
 CH1:  $V_{OUT(mVpp)}$ , 50 mV, 5 ms / div.  
 Zoom: 20  $\mu\text{s}$  / div.  
 $V_{RIPPLE(PK-PK)} = 217.9 \text{ mV}_{pp}$ .

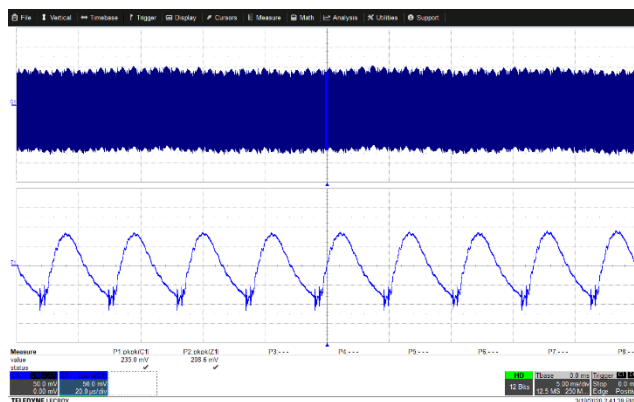


**Figure 73** – Output Voltage Ripple.  
 $V_{IN} = 130 \text{ VDC}$ ,  $I_{OUT} = 1.67 \text{ A}$ .  
 CH1:  $V_{OUT(mVpp)}$ , 50 mV, 5 ms / div.  
 Zoom: 20  $\mu\text{s}$  / div.  
 $V_{RIPPLE(PK-PK)} = 211.8 \text{ mV}_{pp}$ .



**Figure 74** – Output Voltage Ripple.  
 $V_{IN} = 400 \text{ VDC}$ ,  $I_{OUT} = 1.67 \text{ A}$ .  
 CH1:  $V_{OUT(mVpp)}$ , 50 mV, 5 ms / div.  
 Zoom: 20  $\mu\text{s}$  / div.  
 $V_{RIPPLE(PK-PK)} = 211.5 \text{ mV}_{pp}$ .





**Figure 75** – Output Voltage Ripple.

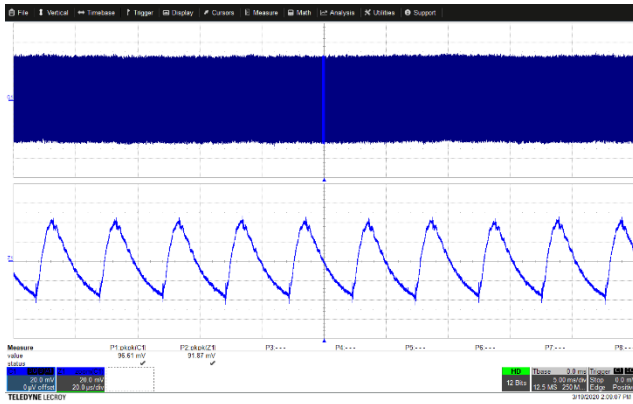
$V_{IN} = 550$  VDC,  $I_{OUT} = 1.67$  A.

CH1:  $V_{OUT(mVpp)}$ , 50 mV, 5 ms / div.

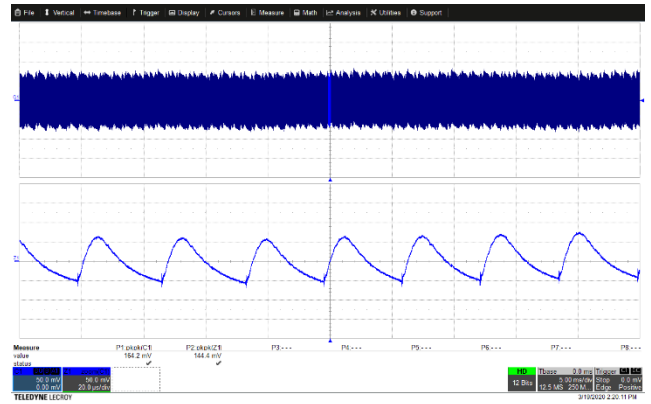
Zoom: 20  $\mu$ s / div.

$V_{RIPPLE(PK-PK)} = 235.0$  mV<sub>pp</sub>.

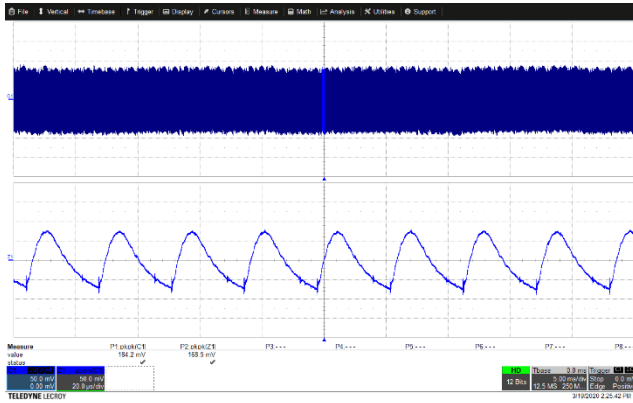
9.4.3 75% Loading Condition



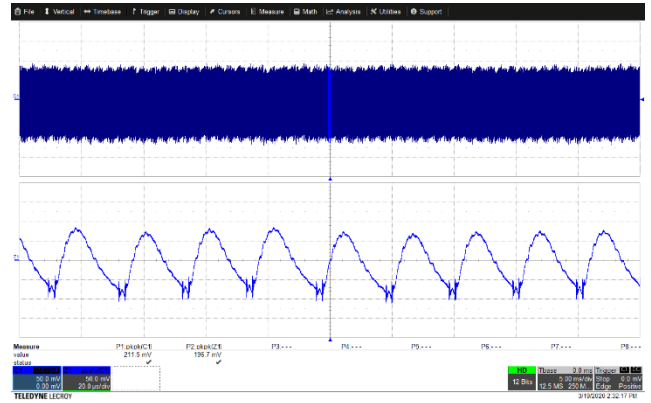
**Figure 76** – Output Voltage Ripple.  
 $V_{IN} = 30 \text{ VDC}$ ,  $I_{OUT} = 0.625 \text{ A}$ .  
**CH1:**  $V_{OUT(mVpp)}$ , 20 mV, 5 ms / div.  
 Zoom: 20  $\mu\text{s}$  / div.  
 $V_{RIPPLE(PK-PK)} = 96.61 \text{ mVpp}$ .



**Figure 77** – Output Voltage Ripple.  
 $V_{IN} = 60 \text{ VDC}$ ,  $I_{OUT} = 0.9375 \text{ A}$ .  
**CH1:**  $V_{OUT(mVpp)}$ , 50 mV, 5 ms / div.  
 Zoom: 20  $\mu\text{s}$  / div.  
 $V_{RIPPLE(PK-PK)} = 164.2 \text{ mVpp}$ .

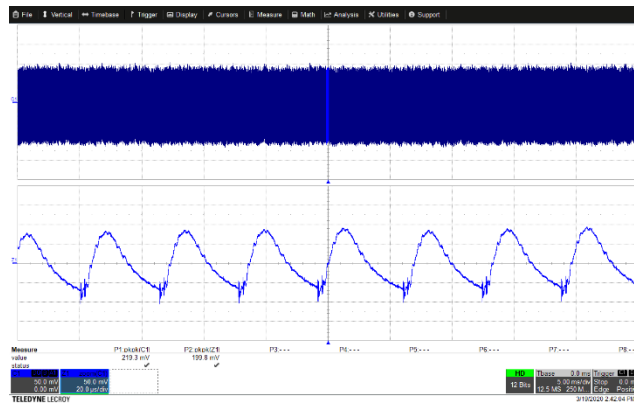


**Figure 78** – Output Voltage Ripple.  
 $V_{IN} = 130 \text{ VDC}$ ,  $I_{OUT} = 1.25 \text{ A}$ .  
**CH1:**  $V_{OUT(mVpp)}$ , 50 mV, 5 ms / div.  
 Zoom: 20  $\mu\text{s}$  / div.  
 $V_{RIPPLE(PK-PK)} = 184.2 \text{ mVpp}$ .



**Figure 79** – Output Voltage Ripple.  
 $V_{IN} = 400 \text{ VDC}$ ,  $I_{OUT} = 1.25 \text{ A}$ .  
**CH1:**  $V_{OUT(mVpp)}$ , 50 mV, 5 ms / div.  
 Zoom: 20  $\mu\text{s}$  / div.  
 $V_{RIPPLE(PK-PK)} = 190.9 \text{ mVpp}$ .





**Figure 80** – Output Voltage Ripple.

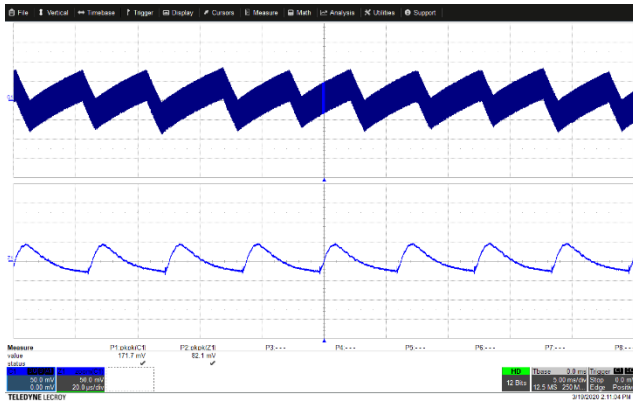
$V_{IN} = 550$  VDC,  $I_{OUT} = 1.25$  A.

CH1:  $V_{OUT(mVpp)}$ , 50 mV, 5 ms / div.

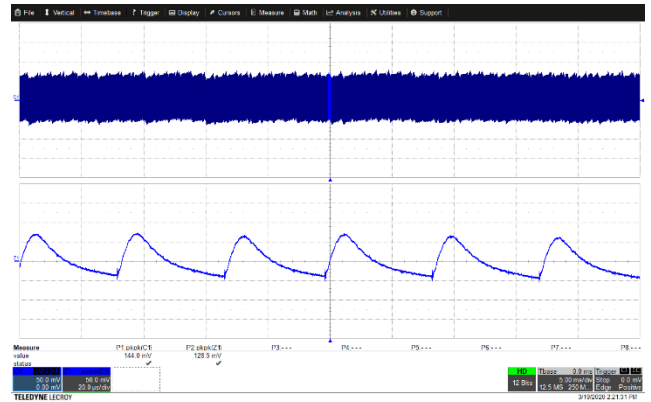
Zoom: 20  $\mu$ s / div.

$V_{RIPPLE(PK-PK)} = 219.3$  mV<sub>pp</sub>.

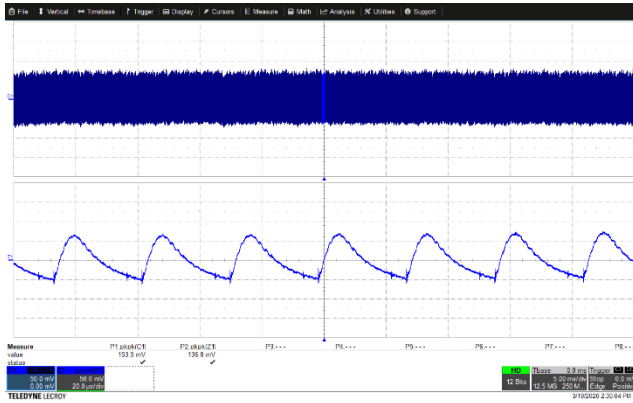
9.4.4 50% Loading Condition



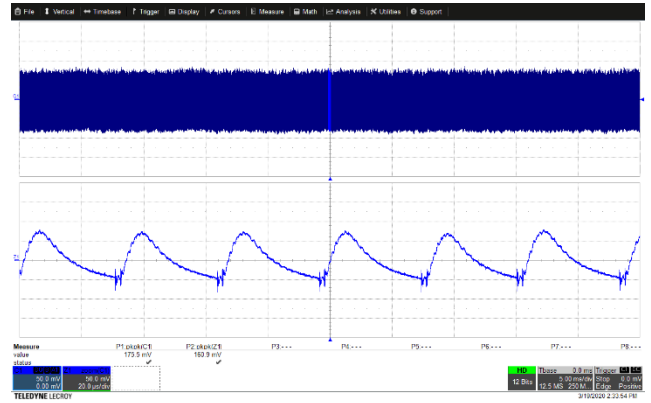
**Figure 81** – Output Voltage Ripple.  
 $V_{IN} = 30 \text{ VDC}$ ,  $I_{OUT} = 0.417 \text{ A}$ .  
 CH1:  $V_{OUT(mVpp)}$ , 50 mV, 5 ms / div.  
 Zoom: 20  $\mu\text{s}$  / div.  
 $V_{RIPPLE(PK-PK)} = 171.7 \text{ mVpp}$ .



**Figure 82** – Output Voltage Ripple.  
 $V_{IN} = 60 \text{ VDC}$ ,  $I_{OUT} = 0.625 \text{ A}$ .  
 CH1:  $V_{OUT(mVpp)}$ , 50 mV, 5 ms / div.  
 Zoom: 20  $\mu\text{s}$  / div.  
 $V_{RIPPLE(PK-PK)} = 144.0 \text{ mVpp}$ .

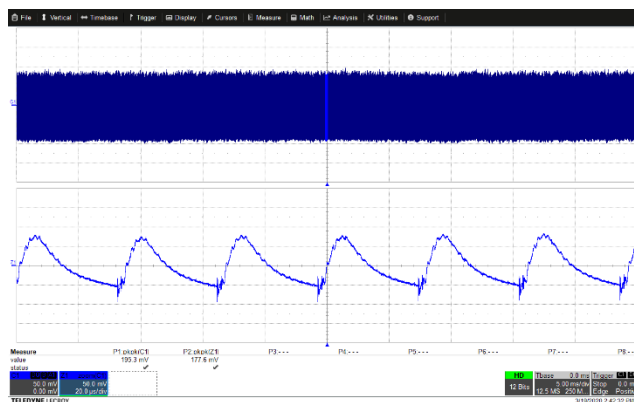


**Figure 83** – Output Voltage Ripple.  
 $V_{IN} = 130 \text{ VDC}$ ,  $I_{OUT} = 0.833 \text{ A}$ .  
 CH1:  $V_{OUT(mVpp)}$ , 50 mV, 5 ms / div.  
 Zoom: 20  $\mu\text{s}$  / div.  
 $V_{RIPPLE(PK-PK)} = 153.5 \text{ mVpp}$ .



**Figure 84** – Output Voltage Ripple.  
 $V_{IN} = 400 \text{ VDC}$ ,  $I_{OUT} = 0.833 \text{ A}$ .  
 CH1:  $V_{OUT(mVpp)}$ , 50 mV, 5 ms / div.  
 Zoom: 20  $\mu\text{s}$  / div.  
 $V_{RIPPLE(PK-PK)} = 175.5 \text{ mVpp}$ .





**Figure 85** – Output Voltage Ripple.

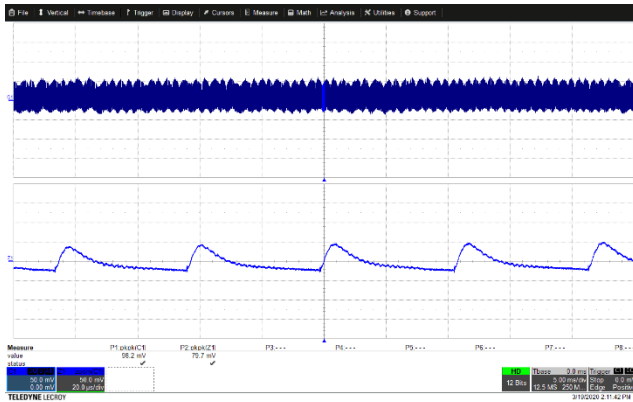
$V_{IN} = 550 \text{ VDC}$ ,  $I_{OUT} = 0.833 \text{ A}$ .

CH1:  $V_{OUT(mVpp)}$ , 50 mV, 5 ms / div.

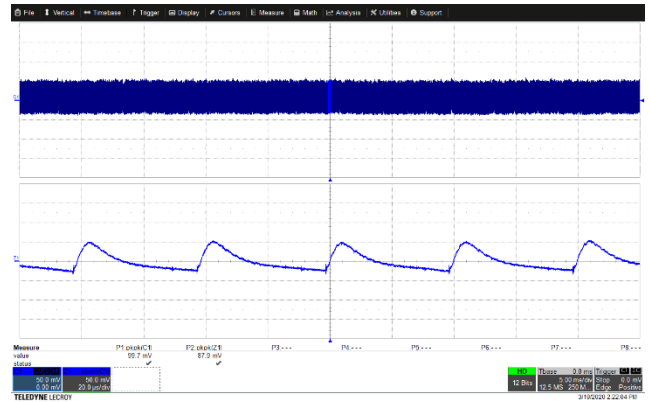
Zoom: 20  $\mu\text{s}$  / div.

$V_{RIPPLE(PK-PK)} = 195.3 \text{ mV}_{PP}$ .

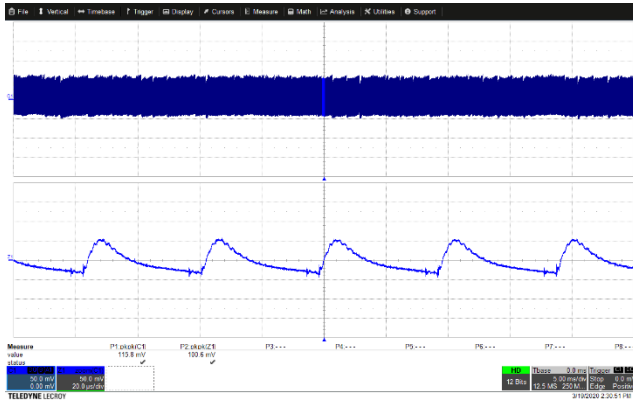
9.4.5 25% Loading Condition



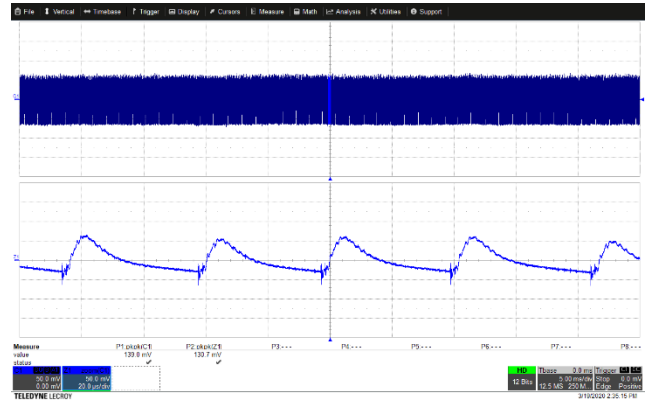
**Figure 86** – Output Voltage Ripple.  
 $V_{IN} = 30 \text{ VDC}$ ,  $I_{OUT} = 0.208 \text{ A}$ .  
 CH1:  $V_{OUT(mVpp)}$ , 50 mV, 5 ms / div.  
 Zoom: 20  $\mu\text{s}$  / div.  
 $V_{RIPPLE(PK-PK)} = 98.2 \text{ mVpp}$ .



**Figure 87** – Output Voltage Ripple.  
 $V_{IN} = 60 \text{ VDC}$ ,  $I_{OUT} = 0.3125 \text{ A}$ .  
 CH1:  $V_{OUT(mVpp)}$ , 50 mV, 5 ms / div.  
 Zoom: 20  $\mu\text{s}$  / div.  
 $V_{RIPPLE(PK-PK)} = 99.7 \text{ mVpp}$ .

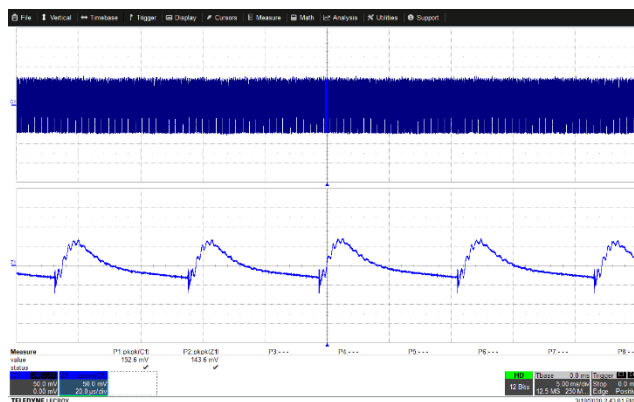


**Figure 88** – Output Voltage Ripple.  
 $V_{IN} = 130 \text{ VDC}$ ,  $I_{OUT} = 0.417 \text{ A}$ .  
 CH1:  $V_{OUT(mVpp)}$ , 50 mV, 5 ms / div.  
 Zoom: 20  $\mu\text{s}$  / div.  
 $V_{RIPPLE(PK-PK)} = 115.8 \text{ mVpp}$ .



**Figure 89** – Output Voltage Ripple.  
 $V_{IN} = 400 \text{ VDC}$ ,  $I_{OUT} = 0.417 \text{ A}$ .  
 CH1:  $V_{OUT(mVpp)}$ , 50 mV, 5 ms / div.  
 Zoom: 20  $\mu\text{s}$  / div.  
 $V_{RIPPLE(PK-PK)} = 139.0 \text{ mVpp}$ .





**Figure 90** – Output Voltage Ripple.

$V_{IN} = 550 \text{ VDC}$ ,  $I_{OUT} = 0.417 \text{ A}$ .

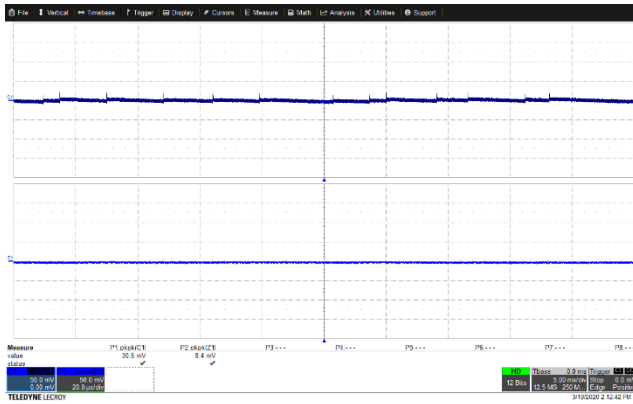
CH1:  $V_{OUT(mV_{pp})}$ , 50 mV, 5 ms / div.

Zoom: 20  $\mu\text{s}$  / div.

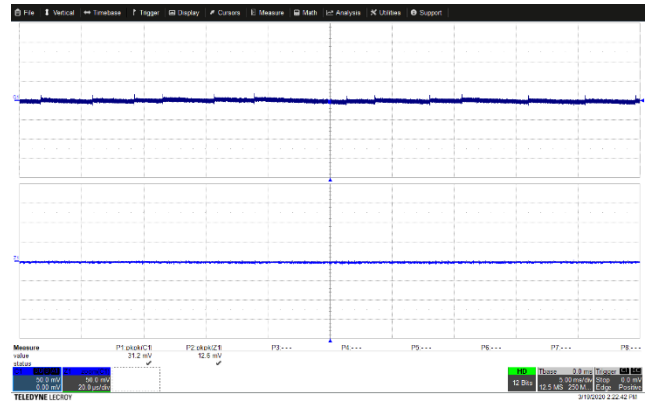
$V_{RIPPLE(PK-PK)} = 152.6 \text{ mV}_{PP}$ .



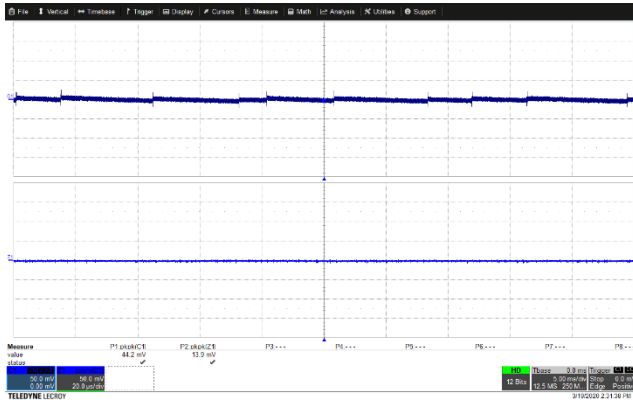
### 9.4.6 0% Loading Condition



**Figure 91** – Output Voltage Ripple.  
 $V_{IN} = 30 \text{ VDC}$ ,  $I_{OUT} = 0 \text{ A}$ .  
**CH1:**  $V_{OUT(mVpp)}$ , 50 mV, 5 ms / div.  
 Zoom: 20  $\mu\text{s}$  / div.  
 $V_{RIPPLE(PK-PK)} = 30.6 \text{ mV}_{pp}$ .



**Figure 92** – Output Voltage Ripple.  
 $V_{IN} = 60 \text{ VDC}$ ,  $I_{OUT} = 0 \text{ A}$ .  
**CH1:**  $V_{OUT(mVpp)}$ , 50 mV, 5 ms / div.  
 Zoom: 20  $\mu\text{s}$  / div.  
 $V_{RIPPLE(PK-PK)} = 31.2 \text{ mV}_{pp}$ .

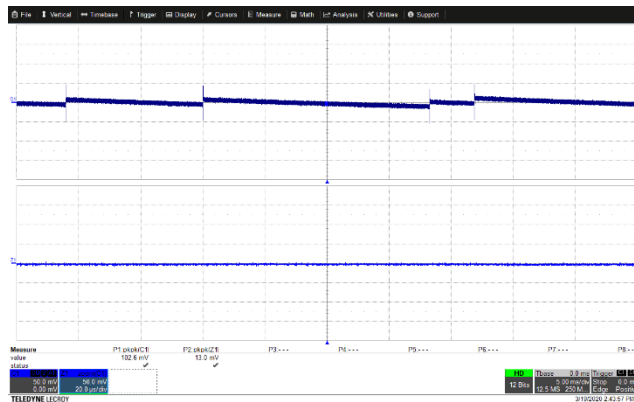


**Figure 93** – Output Voltage Ripple.  
 $V_{IN} = 130 \text{ VDC}$ ,  $I_{OUT} = 0 \text{ A}$ .  
**CH1:**  $V_{OUT(mVpp)}$ , 50 mV, 5 ms / div.  
 Zoom: 20  $\mu\text{s}$  / div.  
 $V_{RIPPLE(PK-PK)} = 44.2 \text{ mV}_{pp}$ .



**Figure 94** – Output Voltage Ripple.  
 $V_{IN} = 400 \text{ VDC}$ ,  $I_{OUT} = 0 \text{ A}$ .  
**CH1:**  $V_{OUT(mVpp)}$ , 50 mV, 5 ms / div.  
 Zoom: 20  $\mu\text{s}$  / div.  
 $V_{RIPPLE(PK-PK)} = 82.9 \text{ mV}_{pp}$ .





**Figure 95** – Output Voltage Ripple.

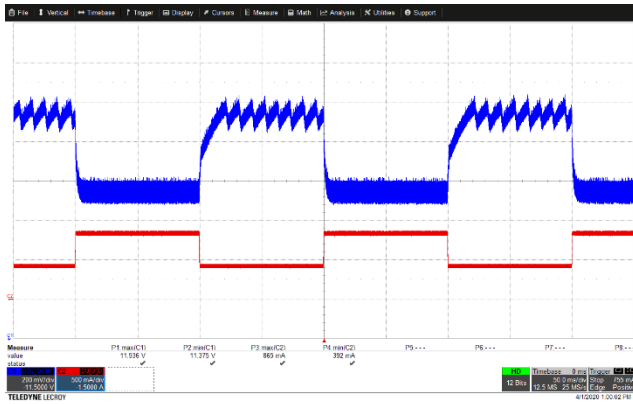
$V_{IN} = 550 \text{ VDC}$ ,  $I_{OUT} = 0 \text{ A}$ .

CH1:  $V_{OUT(mVpp)}$ , 50 mV, 5 ms / div.

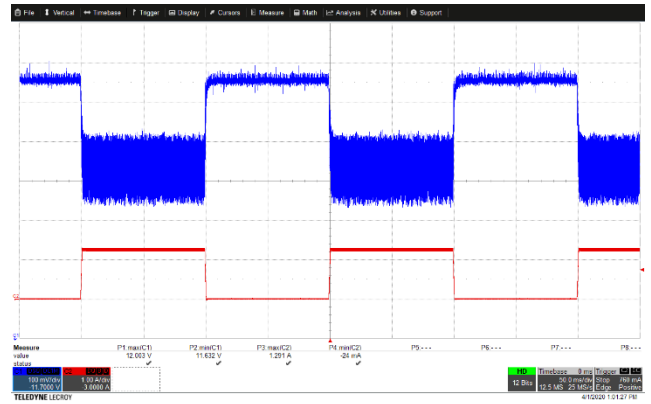
Zoom: 20  $\mu\text{s}$  / div.

$V_{RIPPLE(PK-PK)} = 102.6 \text{ mV}_{PP}$ .

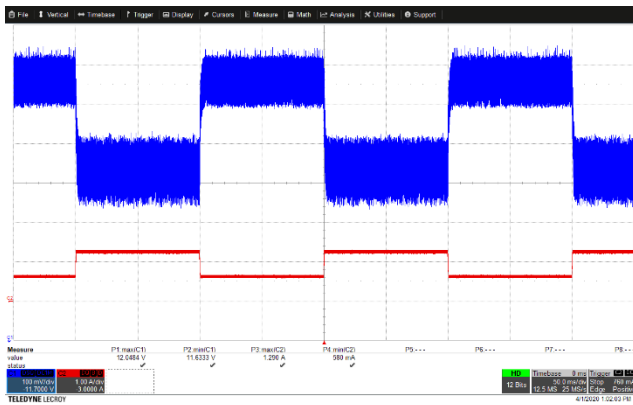
### 9.5 Output Load Transient



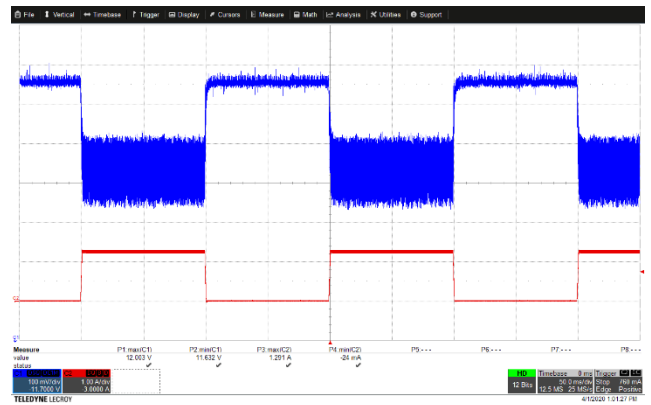
**Figure 96** – Transient Load: 50 – 100%.  
 $V_{IN} = 30 \text{ VDC}$ ,  $I_{OUT} = 0.417 \text{ A} - 0.83 \text{ A}$ .  
**CH1:**  $V_{OUTPUT}$ , 200 mV, 50 ms / div.  
**CH2:**  $I_{OUTPUT}$ , 500 mA, 50 ms / div.  
 $V_{OUTPUT(MAX)} = 11.936 \text{ V}$ .  
 $V_{OUTPUT(MIN)} = 11.375 \text{ V}$ .



**Figure 97** – Transient Load: 0 – 100%.  
 $V_{IN} = 30 \text{ VDC}$ ,  $I_{OUT} = 0 \text{ A} - 0.83 \text{ A}$ .  
**CH1:**  $V_{OUTPUT}$ , 200 mV, 50 ms / div.  
**CH2:**  $I_{OUTPUT}$ , 500 mA, 50 ms / div.  
 $V_{OUTPUT(MAX)} = 11.988 \text{ V}$ .  
 $V_{OUTPUT(MIN)} = 11.381 \text{ V}$ .

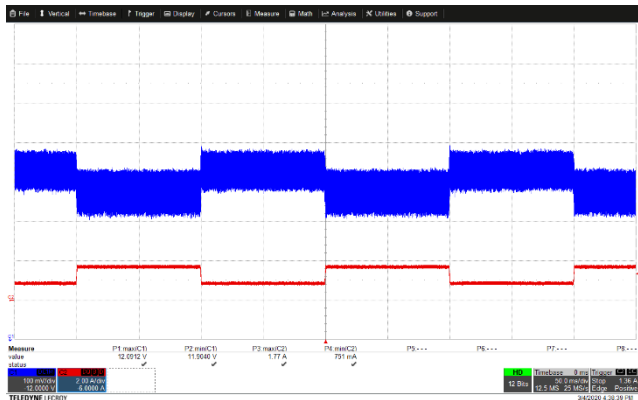


**Figure 98** – Transient Load : 50 – 100%.  
 $V_{IN} = 60 \text{ VDC}$ ,  $I_{OUT} = 0.625 \text{ A} - 1.25 \text{ A}$ .  
**CH1:**  $V_{OUTPUT}$ , 100 mV, 50 ms / div.  
**CH2:**  $I_{OUTPUT}$ , 1 A, 50 ms / div.  
 $V_{OUTPUT(MAX)} = 12.0484 \text{ V}$ .  
 $V_{OUTPUT(MIN)} = 11.6333 \text{ V}$ .

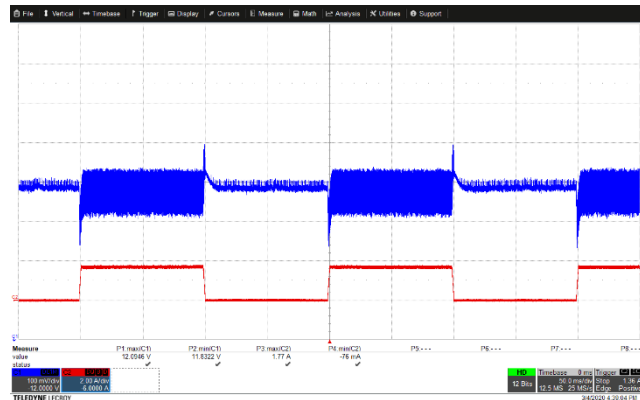


**Figure 99** – Transient Load : 0 – 100%.  
 $V_{IN} = 60 \text{ VDC}$ ,  $I_{OUT} = 0 \text{ A} - 1.25 \text{ A}$ .  
**CH1:**  $V_{OUTPUT}$ , 100 mV, 50 ms / div.  
**CH2:**  $I_{OUTPUT}$ , 1 A, 50 ms / div.  
 $V_{OUTPUT(MAX)} = 12.003 \text{ V}$ .  
 $V_{OUTPUT(MIN)} = 11.632 \text{ V}$ .

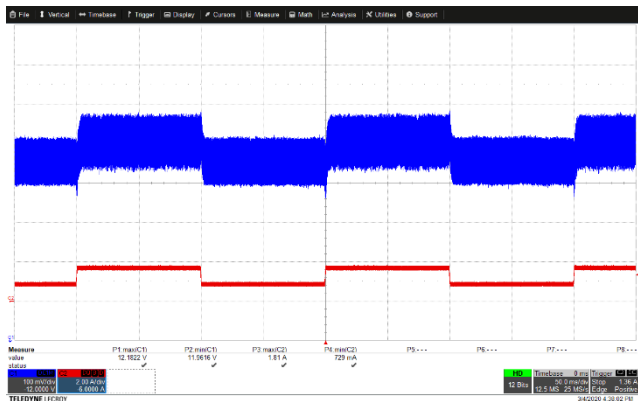




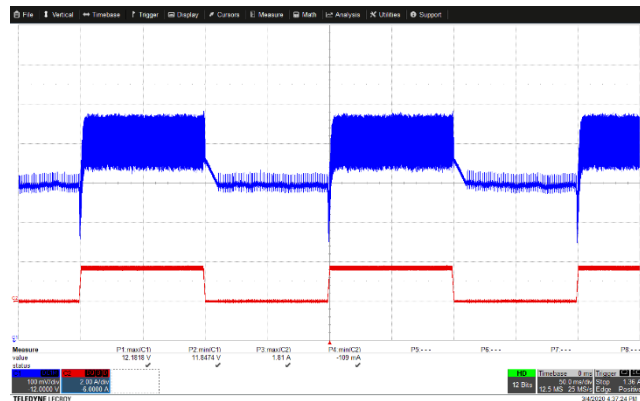
**Figure 100** – Transient Load : 50 – 100%.  
 $V_{IN} = 130 \text{ VDC}$ ,  $I_{OUT} = 0.83 \text{ A} - 1.67 \text{ A}$ .  
**CH1:**  $V_{OUTPUT}$ , 100 mV, 50 ms / div.  
**CH2:**  $I_{OUTPUT}$ , 2 A, 50 ms / div.  
 $V_{OUTPUT(MAX)} = 12.0912 \text{ V}$ .  
 $V_{OUTPUT(MIN)} = 11.9040 \text{ V}$ .



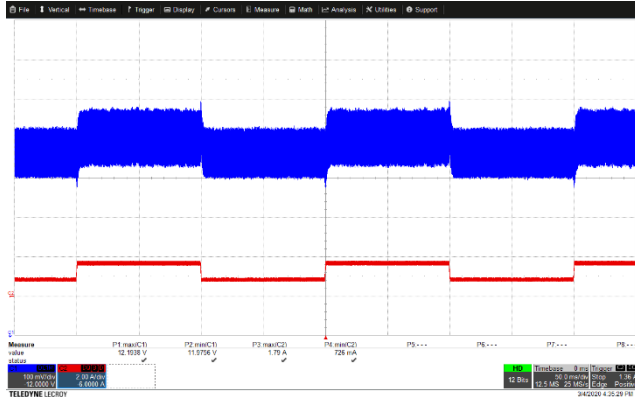
**Figure 101** – Transient Load : 0 – 100%.  
 $V_{IN} = 130 \text{ VDC}$ ,  $I_{OUT} = 0 \text{ A} - 1.67 \text{ A}$ .  
**CH1:**  $V_{OUTPUT}$ , 100 mV, 50 ms / div.  
**CH2:**  $I_{OUTPUT}$ , 2 A, 50 ms / div.  
 $V_{OUTPUT(MAX)} = 12.0946 \text{ V}$ .  
 $V_{OUTPUT(MIN)} = 11.8322 \text{ V}$ .



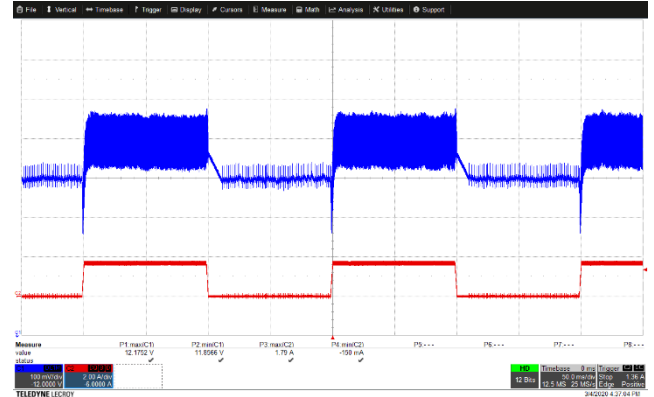
**Figure 102** – Transient Load: 50 – 100%.  
 $V_{IN} = 400 \text{ VDC}$ ,  $I_{OUT} = 0.83 \text{ A} - 1.67 \text{ A}$ .  
**CH1:**  $V_{OUTPUT}$ , 100 mV, 50 ms / div.  
**CH2:**  $I_{OUTPUT}$ , 2 A, 50 ms / div.  
 $V_{OUTPUT(MAX)} = 12.1822 \text{ V}$ .  
 $V_{OUTPUT(MIN)} = 11.9616 \text{ V}$ .



**Figure 103** – Transient Load: 0 – 100%.  
 $V_{IN} = 400 \text{ VDC}$ ,  $I_{OUT} = 0 \text{ A} - 1.67 \text{ A}$ .  
**CH1:**  $V_{OUTPUT}$ , 100 mV, 50 ms / div.  
**CH2:**  $I_{OUTPUT}$ , 2 A, 50 ms / div.  
 $V_{OUTPUT(MAX)} = 12.1818 \text{ V}$ .  
 $V_{OUTPUT(MIN)} = 11.8474 \text{ V}$ .



**Figure 104** –  $V_{IN} = 130 \text{ VDC}$ ,  $I_{OUT} = 0.83 \text{ A} - 1.67 \text{ A}$ .  
**CH1:**  $V_{OUTPUT}$ , 100 mV, 50 ms / div.  
**CH2:**  $I_{OUTPUT}$ , 2 A, 50 ms / div.  
 $V_{OUTPUT(MAX)} = 12.1938 \text{ V}$ .  
 $V_{OUTPUT(MIN)} = 11.9756 \text{ V}$ .



**Figure 105** –  $V_{IN} = 130 \text{ VDC}$ ,  $I_{OUT} = 0 \text{ A} - 1.67 \text{ A}$ .  
**CH1:**  $V_{OUTPUT}$ , 100 mV, 50 ms / div.  
**CH2:**  $I_{OUTPUT}$ , 2 A, 50 ms / div.  
 $V_{OUTPUT(MAX)} = 12.1752 \text{ V}$ .  
 $V_{OUTPUT(MIN)} = 11.8566 \text{ V}$ .

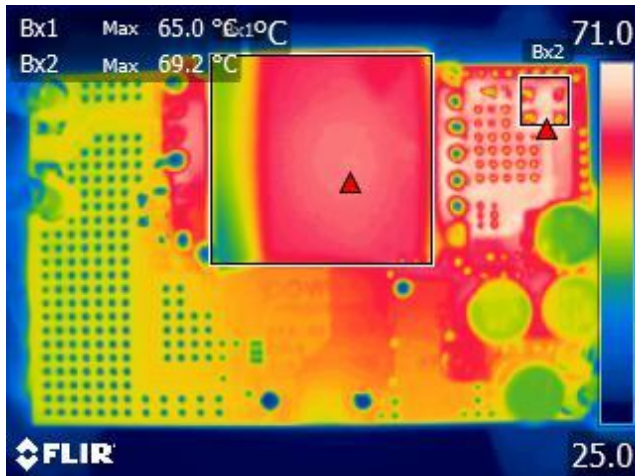


## 10 Thermal Performance

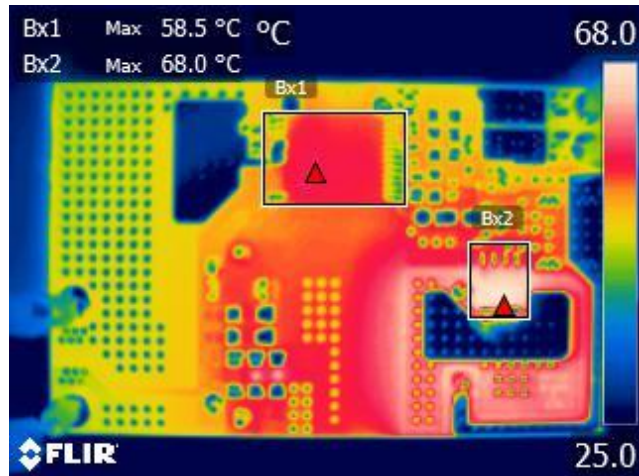
### 10.1 Thermals at Room Temperature

All measurements have been done at room ambient temperature after 2 hours of continuous operation.

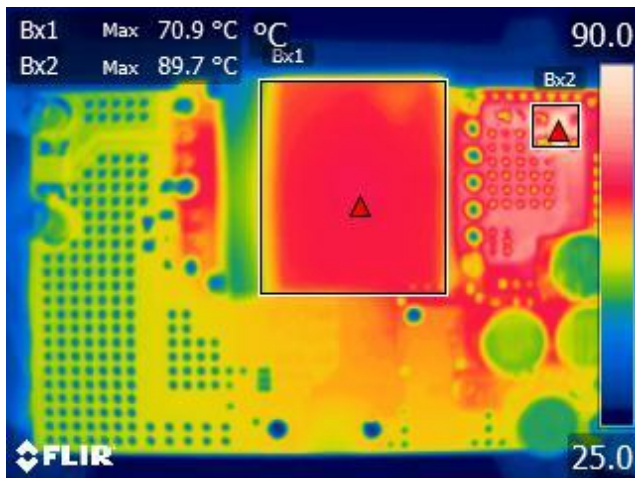
#### 10.1.1 20 W Continuous Output Power



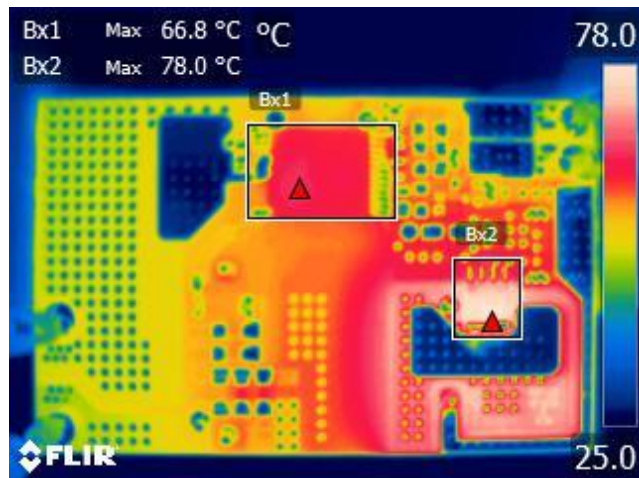
**Figure 106** – Component Side.  
 $V_{IN} = 130 \text{ VDC}$ ,  $I_{OUT} = 1.67 \text{ A}$ .  
 Ambient ( $^{\circ}\text{C}$ ): 25.7.  
 Transformer Core ( $^{\circ}\text{C}$ ): 65.0.  
 Secondary Snubber ( $^{\circ}\text{C}$ ): 69.2.



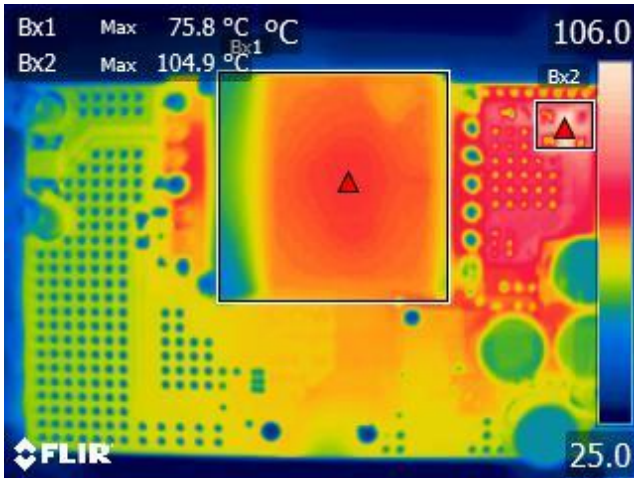
**Figure 107** – Solder Side.  
 $V_{IN} = 130 \text{ VDC}$ ,  $I_{OUT} = 1.67 \text{ A}$ .  
 Ambient ( $^{\circ}\text{C}$ ): 25.7.  
 InnoSwitch ( $^{\circ}\text{C}$ ): 58.5.  
 SRFET ( $^{\circ}\text{C}$ ): 68.0.



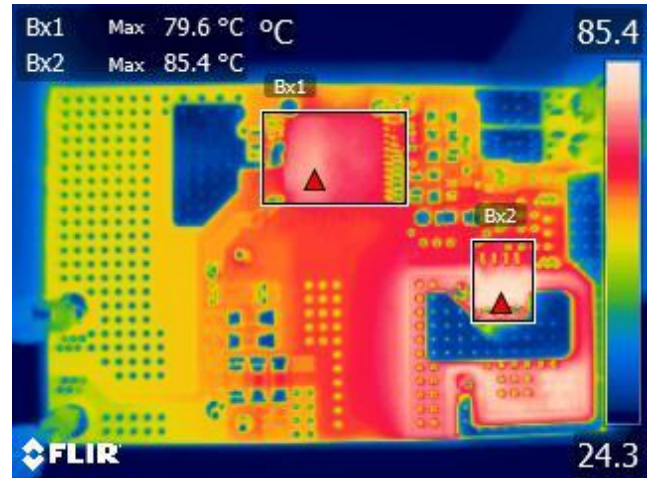
**Figure 108** – Component Side.  
 $V_{IN} = 400 \text{ VDC}$ ,  $I_{OUT} = 1.67 \text{ A}$ .  
 Ambient ( $^{\circ}\text{C}$ ): 27.8.  
 Transformer Core ( $^{\circ}\text{C}$ ): 70.9.  
 Secondary Snubber ( $^{\circ}\text{C}$ ): 89.7.



**Figure 109** – Solder Side.  
 $V_{IN} = 400 \text{ VDC}$ ,  $I_{OUT} = 1.67 \text{ A}$ .  
 Ambient ( $^{\circ}\text{C}$ ): 27.8.  
 InnoSwitch ( $^{\circ}\text{C}$ ): 66.8.  
 SRFET ( $^{\circ}\text{C}$ ): 78.0.

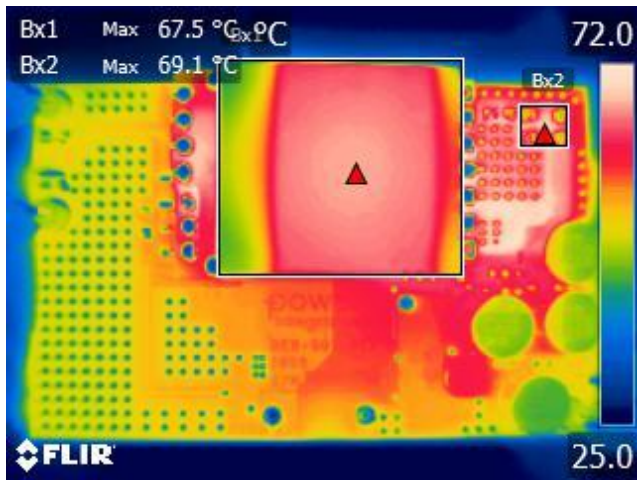


**Figure 110** – Component Side.  
 $V_{IN} = 550$  VDC,  $I_{OUT} = 1.67$  A.  
 Ambient: 28.7.  
 Transformer Core (°C): 75.8.  
 Secondary Snubber (°C): 104.9.

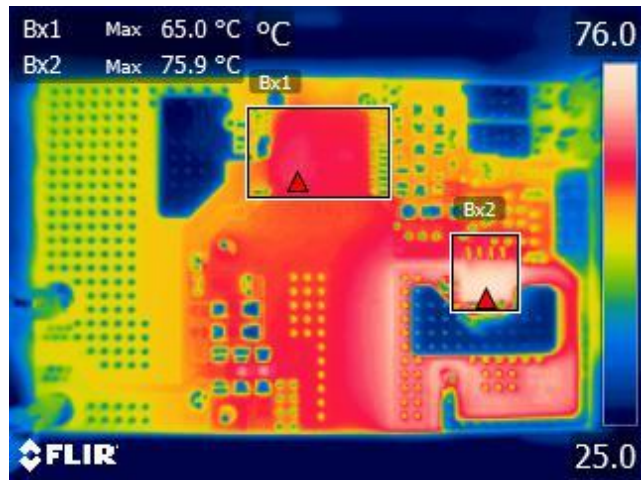


**Figure 111** – Solder Side.  
 $V_{IN} = 550$  VDC,  $I_{OUT} = 1.67$  A.  
 Ambient (°C): 28.7.  
 InnoSwitch (°C): 79.6.  
 SRFET (°C): 85.4.

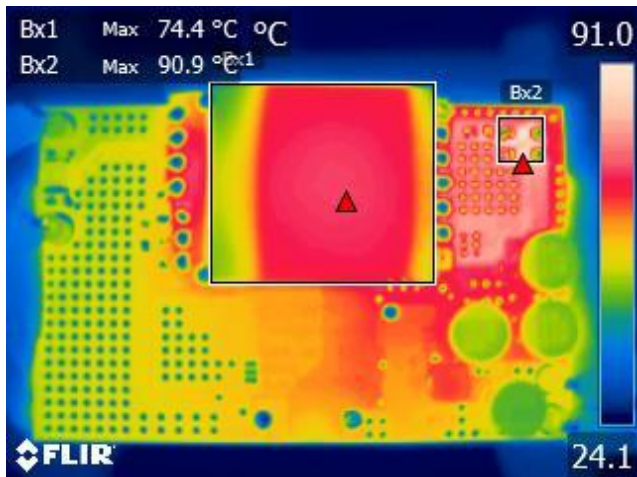
10.1.2 25 W Peak Power



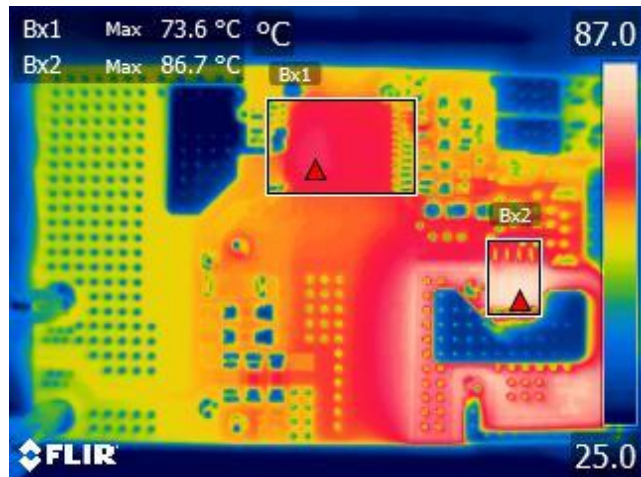
**Figure 112** – Component Side.  
 $V_{IN} = 130 \text{ VDC}$ ,  $I_{OUT} = 2.08 \text{ A}$ .  
 Ambient (°C): 24.2.  
 Transformer Core (°C): 67.5.  
 Secondary Snubber (°C): 69.1.



**Figure 113** – Solder Side.  
 $V_{IN} = 130 \text{ VDC}$ ,  $I_{OUT} = 2.08 \text{ A}$ .  
 Ambient (°C): 24.2.  
 InnoSwitch (°C): 65.0.  
 SRFET (°C): 75.9.

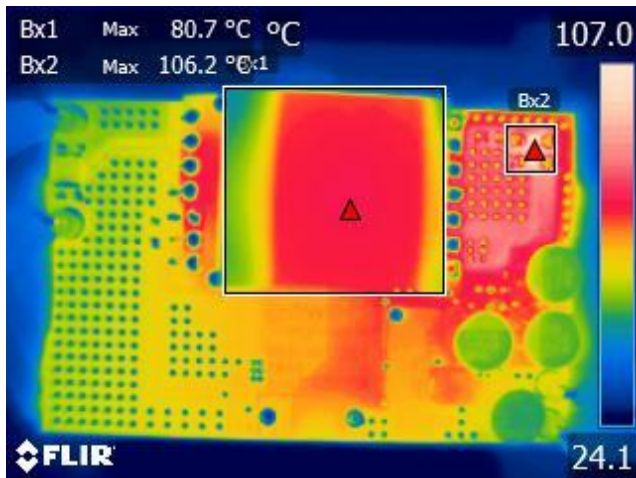


**Figure 114** – Component Side.  
 $V_{IN} = 400 \text{ VDC}$ ,  $I_{OUT} = 1.67 \text{ A}$ .  
 Ambient (°C): 25.5.  
 Transformer Core (°C): 74.4.  
 Secondary Snubber (°C): 90.9.

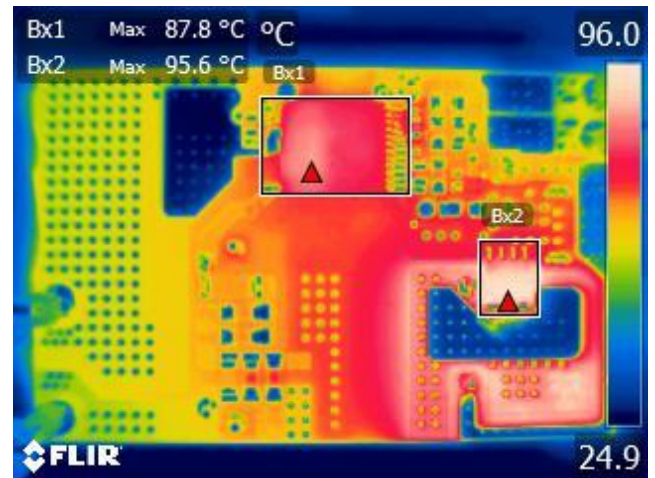


**Figure 115** – Solder Side.  
 $V_{IN} = 400 \text{ VDC}$ ,  $I_{OUT} = 1.67 \text{ A}$ .  
 Ambient (°C): 25.5.  
 InnoSwitch (°C): 73.6.  
 SRFET (°C): 86.7.





**Figure 116** – Component Side.  
 $V_{IN} = 550$  VDC,  $I_{OUT} = 1.67$  A.  
 Ambient: 25.8.  
 Transformer Core (°C): 80.7.  
 Secondary Snubber (°C): 106.2.



**Figure 117** – Solder Side.  
 $V_{IN} = 550$  VDC,  $I_{OUT} = 1.67$  A.  
 Ambient (°C): 25.8.  
 InnoSwitch (°C): 87.8.  
 SRFET (°C): 95.6.

10.2 **INN3977CQ Output Power Limit vs. Ambient Temperature**

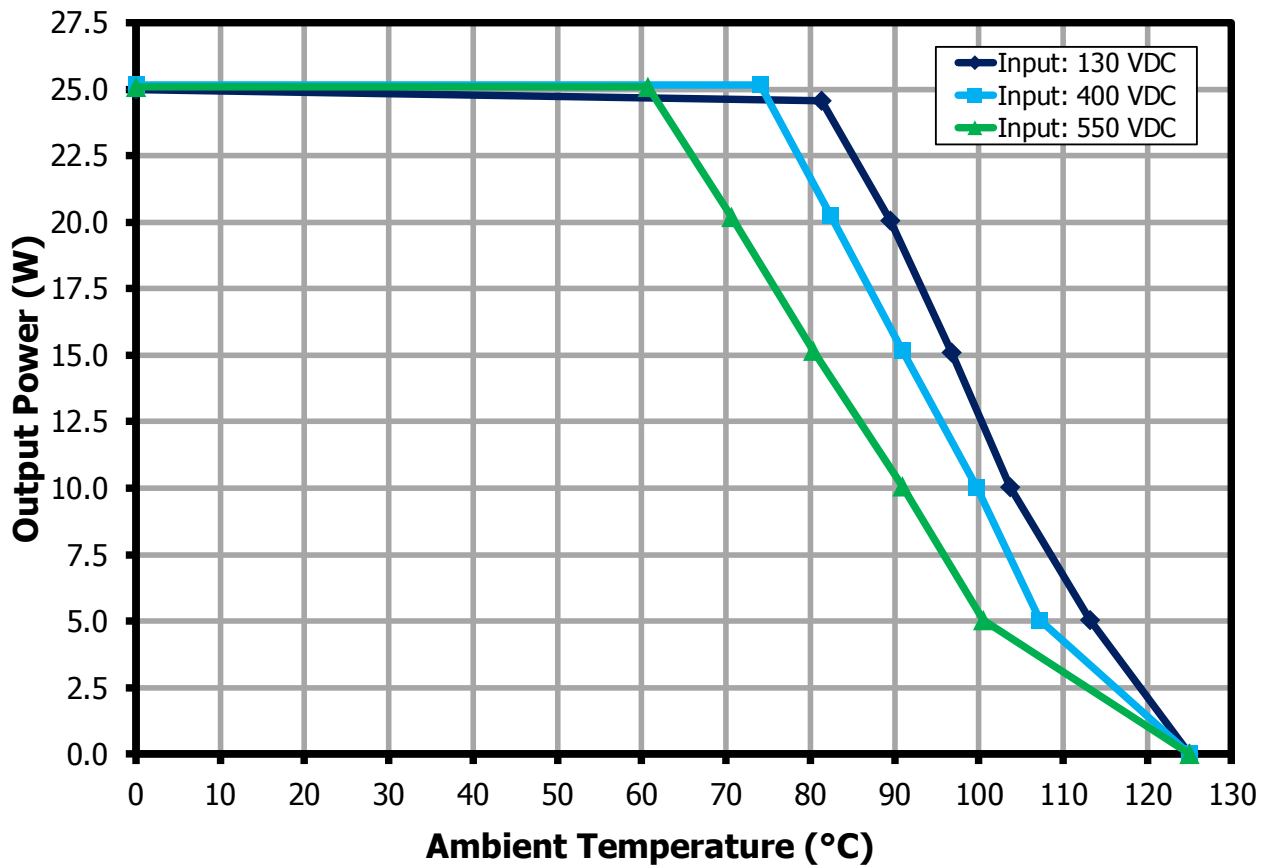


Figure 118 – Output Power vs. Ambient Temperature.

Input: 300 VDC				
Output Power (W)	Ambient (°C)	InnoSwitch Temp (°C)	InnoSwitch Temp – Ambient (°C)	Operating Ambient Temperature (125 °C - Trise)
0.0				125.0
5.0	26.60	44.30	17.70	107.3
10.0	27.30	52.60	25.30	99.7
15.2	27.60	61.70	34.10	90.9
20.3	28.10	70.70	42.60	82.4
25.2	28.40	79.30	50.90	74.1
25.2				0.0

Input: 800 VDC				
Output Power (W)	Ambient (°C)	InnoSwitch Temp (°C)	InnoSwitch Temp – Ambient (°C)	Operating Ambient Temperature (125 °C - Trise)
0.0				125.0
5.0	26.80	51.30	24.50	100.5
10.1	27.20	61.30	34.10	90.9
15.2	28.30	72.90	44.60	80.4
20.2	29.60	83.90	54.30	70.7
25.1	30.20	94.50	64.30	60.7
25.1				0.0

Input: 1000 VDC				
Output Power (W)	Ambient (°C)	InnoSwitch Temp (°C)	InnoSwitch Temp – Ambient (°C)	Operating Ambient Temperature (125 °C - Trise)
0.0				125.0
5.0	26.00	37.80	11.80	113.2
10.0	27.60	48.90	21.30	103.7
15.1	27.60	55.80	28.20	96.8
20.1	27.90	63.40	35.50	89.5
24.6	28.20	71.80	43.60	81.4
25.0				0.0

**12 -40 °C and +85 °C Operational Test**

<b>Start-Up at -40 °C, Full Load</b>						
<b>Ambient (°C)</b>	<b>V<sub>IN</sub> (VDC)</b>	<b>P<sub>IN</sub> (W)</b>	<b>V<sub>OUT</sub> (V)</b>	<b>I<sub>OUT</sub> (A)</b>	<b>P<sub>OUT</sub> (W)</b>	<b>Efficiency (%)</b>
-40	30	6.63	11.68	0.45	5.24	79.00
	60	18.64	11.89	1.25	14.87	79.79
	130	25.73	12.69	1.67	21.13	82.15
	400	26.81	13.37	1.67	22.27	83.05
	550	26.96	12.90	1.67	21.49	79.72
<b>After 1 hour running at full load, no OTP occurred</b>						
<b>Ambient (°C)</b>	<b>V<sub>IN</sub> (VDC)</b>	<b>P<sub>IN</sub> (W)</b>	<b>V<sub>OUT</sub> (V)</b>	<b>I<sub>OUT</sub> (A)</b>	<b>P<sub>OUT</sub> (W)</b>	<b>Efficiency (%)</b>
85	30	11.87	11.53	0.83	9.60	80.85
	60	17.63	11.76	1.25	14.70	83.34
	130	23.28	11.92	1.67	19.86	85.31
	400	23.81	12.01	1.67	20.02	84.06
	550	24.50	12.03	1.67	20.05	81.82

**14 Revision History**

<b>Date</b>	<b>Author</b>	<b>Revision</b>	<b>Description &amp; Changes</b>	<b>Reviewed</b>
19-May-20	JMR	1.0	Initial Release	Apps & Mktg



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**Power Integrations Worldwide Sales Support Locations****WORLD HEADQUARTERS**

5245 Hellyer Avenue  
San Jose, CA 95138, USA  
Main: +1-408-414-9200  
Customer Service:  
Worldwide: +1-65-635-64480  
Americas: +1-408-414-9621  
e-mail: [usasales@power.com](mailto:usasales@power.com)

**CHINA (SHANGHAI)**

Rm 2410, Charity Plaza, No. 88,  
North Caoxi Road,  
Shanghai, PRC 200030  
Phone: +86-21-6354-6323  
e-mail: [chinasales@power.com](mailto:chinasales@power.com)

**CHINA (SHENZHEN)**

17/F, Hivac Building, No. 2, Keji  
Nan 8th Road, Nanshan District,  
Shenzhen, China, 518057  
Phone: +86-755-8672-8689  
e-mail: [chinasales@power.com](mailto:chinasales@power.com)

**GERMANY (AC-DC/LED Sales)**

Einsteinring 24  
85609 Dornach/Aschheim  
Germany  
Tel: +49-89-5527-39100  
e-mail: [eurosales@power.com](mailto:eurosales@power.com)

**GERMANY (Gate Driver Sales)**

HellwegForum 1  
59469 Ense  
Germany  
Tel: +49-2938-64-39990  
e-mail: [igbt-driver.sales@power.com](mailto:igbt-driver.sales@power.com)

**INDIA**

#1, 14<sup>th</sup> Main Road  
Vasanthanagar  
Bangalore-560052  
India  
Phone: +91-80-4113-8020  
e-mail: [indiasales@power.com](mailto:indiasales@power.com)

**ITALY**

Via Milanese 20, 3<sup>rd</sup> Fl.  
20099 Sesto San Giovanni (MI) Italy  
Phone: +39-024-550-8701  
e-mail: [eurosales@power.com](mailto:eurosales@power.com)

**JAPAN**

Yusen Shin-Yokohama 1-chome Bldg.  
1-7-9, Shin-Yokohama, Kohoku-ku  
Yokohama-shi,  
Kanagawa 222-0033 Japan  
Phone: +81-45-471-1021  
e-mail: [japansales@power.com](mailto:japansales@power.com)

**KOREA**

RM 602, 6FL  
Korea City Air Terminal B/D,  
159-6  
Samsung-Dong, Kangnam-Gu,  
Seoul, 135-728 Korea  
Phone: +82-2-2016-6610  
e-mail: [koreasales@power.com](mailto:koreasales@power.com)

**SINGAPORE**

51 Newton Road,  
#19-01/05 Goldhill Plaza  
Singapore, 308900  
Phone: +65-6358-2160  
e-mail: [singaporesales@power.com](mailto:singaporesales@power.com)

**TAIWAN**

5F, No. 318, Nei Hu Rd.,  
Sec. 1  
Nei Hu District  
Taipei 11493, Taiwan R.O.C.  
Phone: +886-2-2659-4570  
e-mail: [taiwansales@power.com](mailto:taiwansales@power.com)

**UK**

Building 5, Suite 21  
The Westbrook Centre  
Milton Road  
Cambridge  
CB4 1YG  
Phone: +44 (0) 7823-557484  
e-mail: [eurosales@power.com](mailto:eurosales@power.com)

