Design Example Report

Title	***220 W Power Factor Corrected LLC Power Supply Using HiperPFS™-5 PFS5178F and HiperLCS™2-HB LCS7265C and HiperLCS2-SR LSR2000C***
Specification	90 VAC – 265 VAC Input; 24 V at 0 – 9.2 A Output
Application	TV and Computer Monitors
Author	Applications Engineering Department
Document Number	DER-672
Date	March 16, 2022
Revision	1.0

Summary and Features

- Integrated PFC and LLC stages for a very low component count design
- Quasi-resonant DCM control ensures low switching losses, small inductor size, and permits use of low-cost boost diode
- High frequency (up to 250 kHz) LLC for small transformer size.
- >96% full load PFC efficiency at 115 VAC
- >97% full load LLC efficiency
    - System efficiency 94% / 95.5% at 115 VAC / 230 VAC
- HiperLCS-2 provides initial start-up bias for the PFC stage
- Eliminates heat sinks for powers up to 220 W

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Important Notes:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. All testing should be performed using an isolation transformer to provide the AC input to the prototype board.
Since there is no separate bias converter in this design, ~280 VDC is present on bulk capacitor C19 immediately after the supply is powered down. For safety, this capacitor must be discharged with an appropriate resistor (10 k / 2 W is adequate), or the supply must be allowed to stand ~10 minutes before handling.

1 Introduction

This engineering report describes a 24 V, 220 W reference design power supply that can operate from 90 VAC to 265 VAC for TV and computer monitor applications. The power supply uses a CRM PFC front-end with a LLC DC-DC converter operating at 120 kHz for high efficiency power conversion.

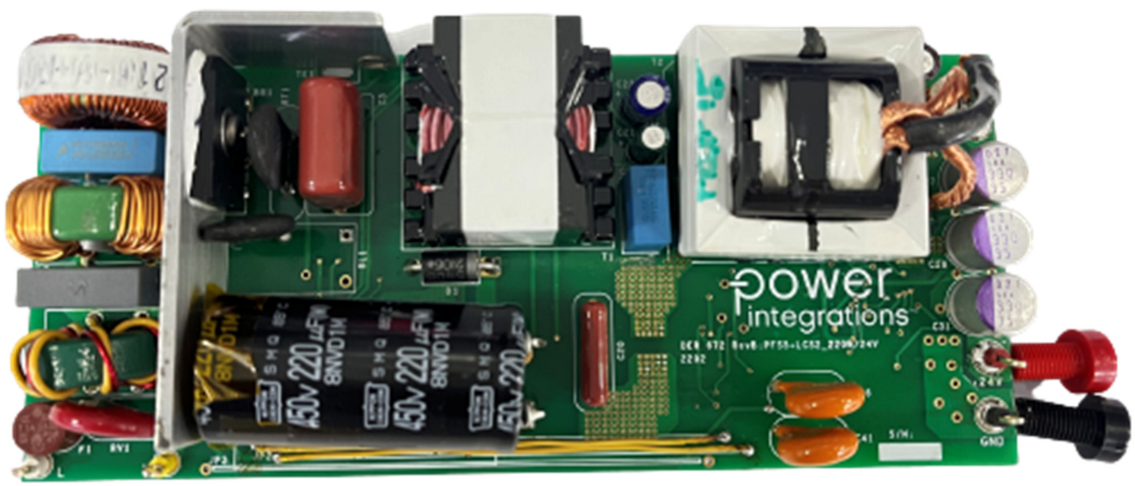


Figure 1 – DER-672, Top View.

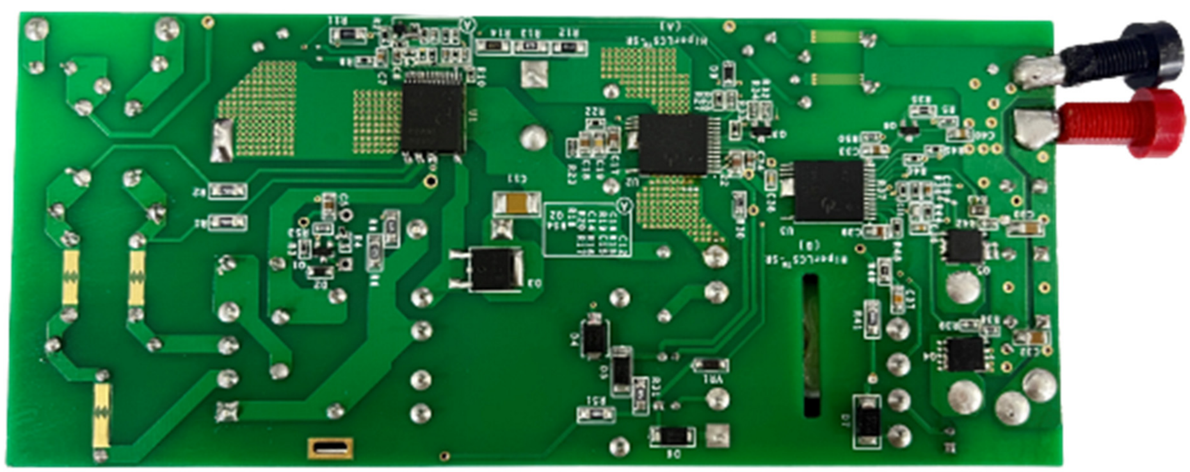


Figure 2 – DER-672, Bottom View.

2 Power Supply Specification

The table below represents the minimum acceptable performance for the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire Input.
Frequency	f_{LINE}	47	50/60	64	Hz	
Power Factor	PF	0.9				Full Load, 265 VAC.
Main Converter Output						
Output Voltage	V_{LG}		24		V	(220W) Full Load.
Output Ripple	$V_{RIPPLE(LG)}$			240	mV_{PK-PK}	20 MHz Bandwidth.
Output Current	I_{LG}	0.00		9.2	A	
Total Output Power						
Continuous Output Power	P_{OUT}		220		W	
Efficiency						
Total system at Full Load.	η_{Main}		94 95.5		%	Measured at 115 VAC, Full Load. Measured at 230 VAC, Full Load.
No Load Input Power Total system at No-Load.	$PIN_{No-Load}$		90 120		mW	Measured at 115 VAC. Measured at 230 VAC.
Ambient Temperature	T_{AMB}	-20		60	ºC	See Thermal Section for Conditions.

3 Schematic

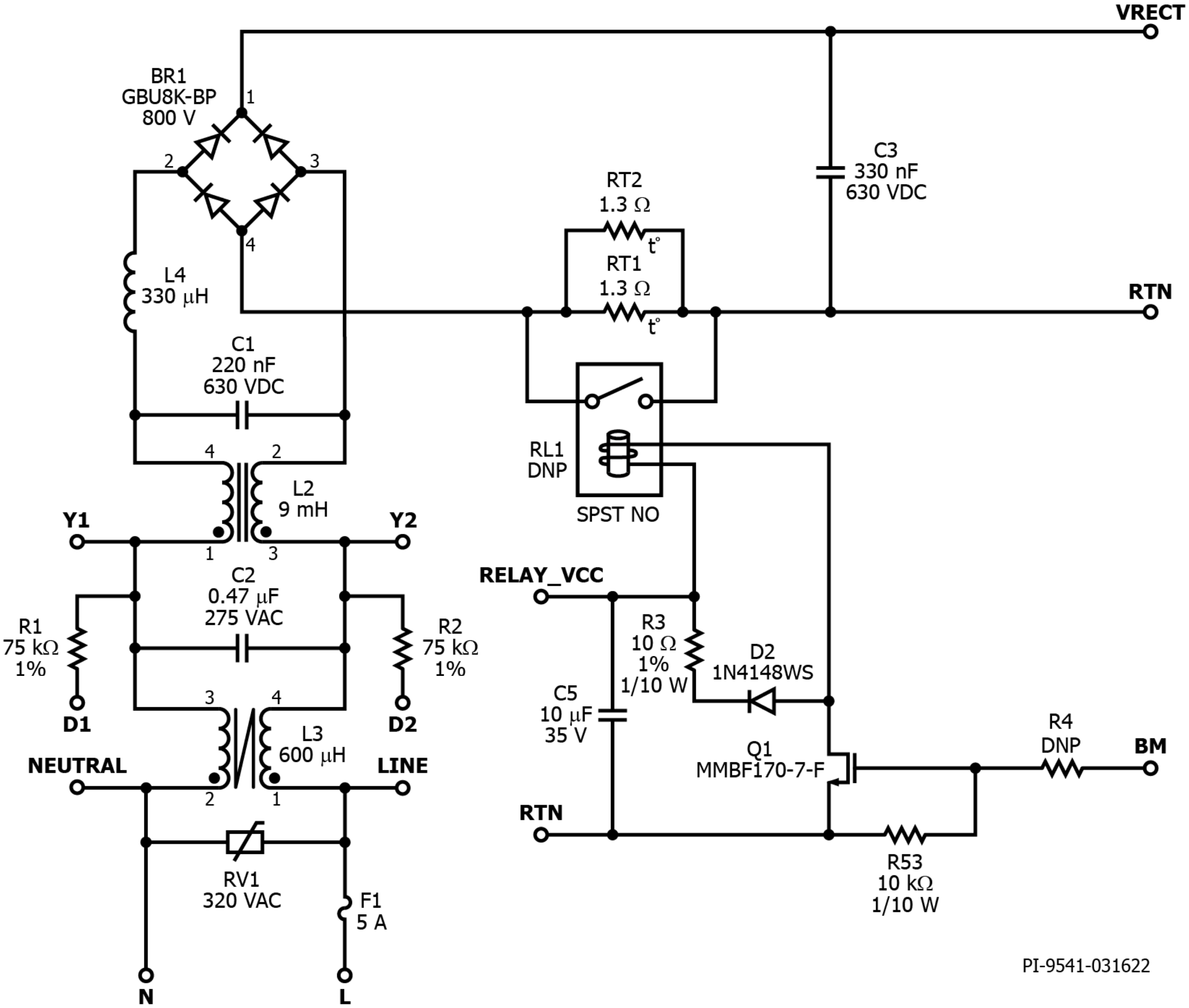


Figure 3 – Input Filter, PFC Choke.

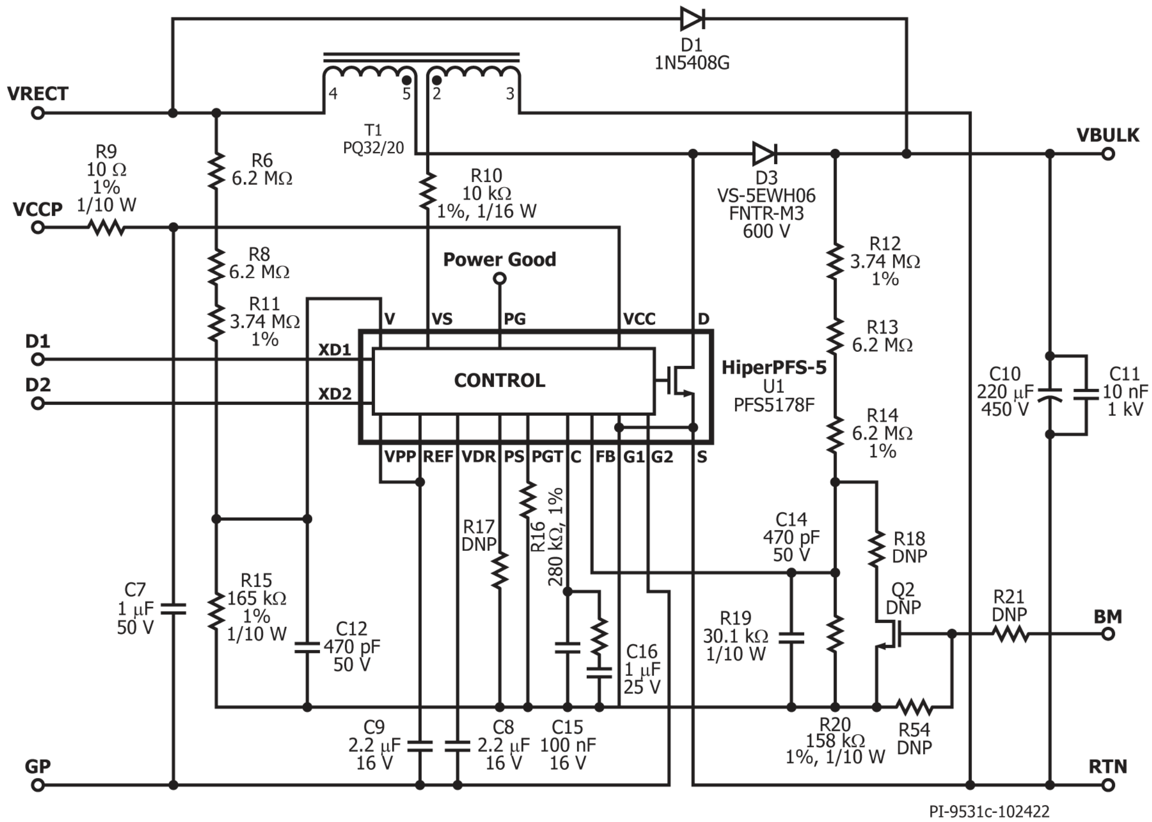


Figure 4 – PFC Stage.

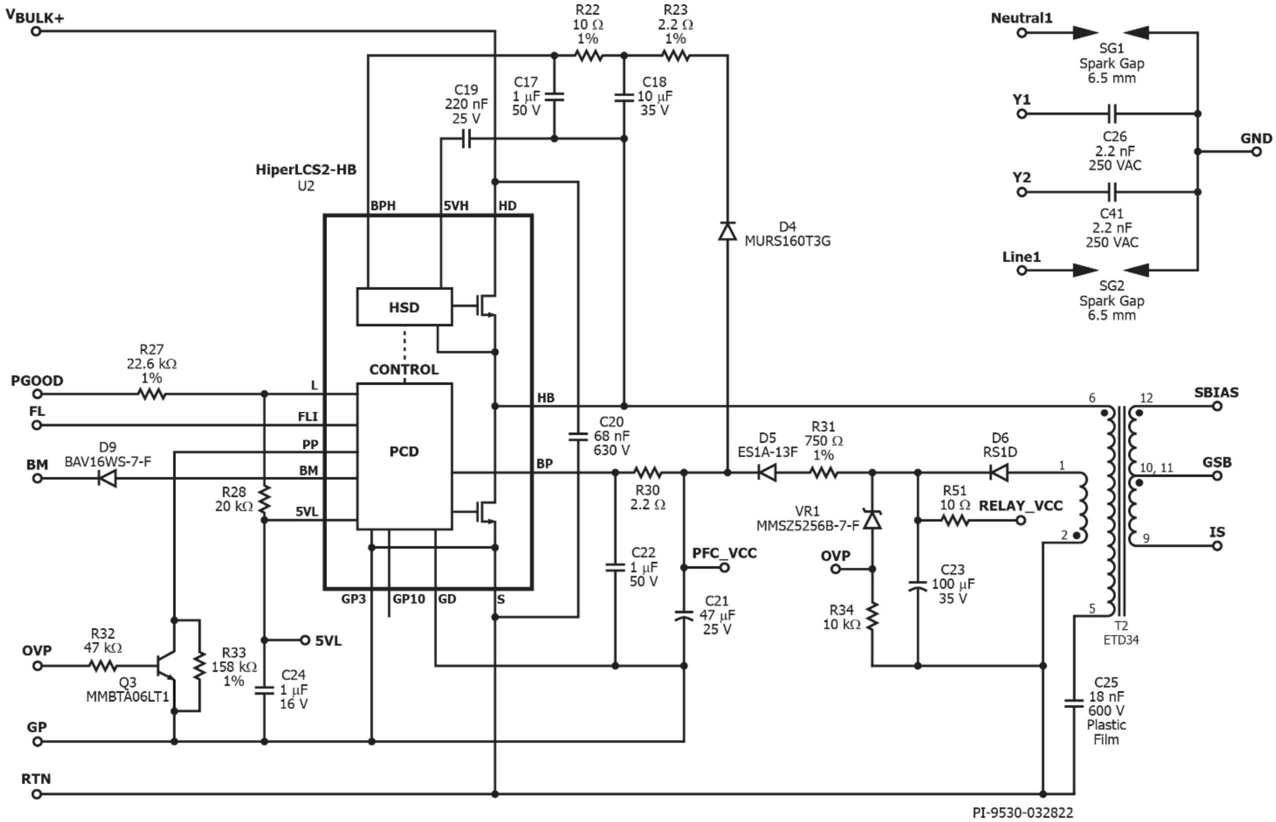


Figure 5– LLC Stage (Primary Section).

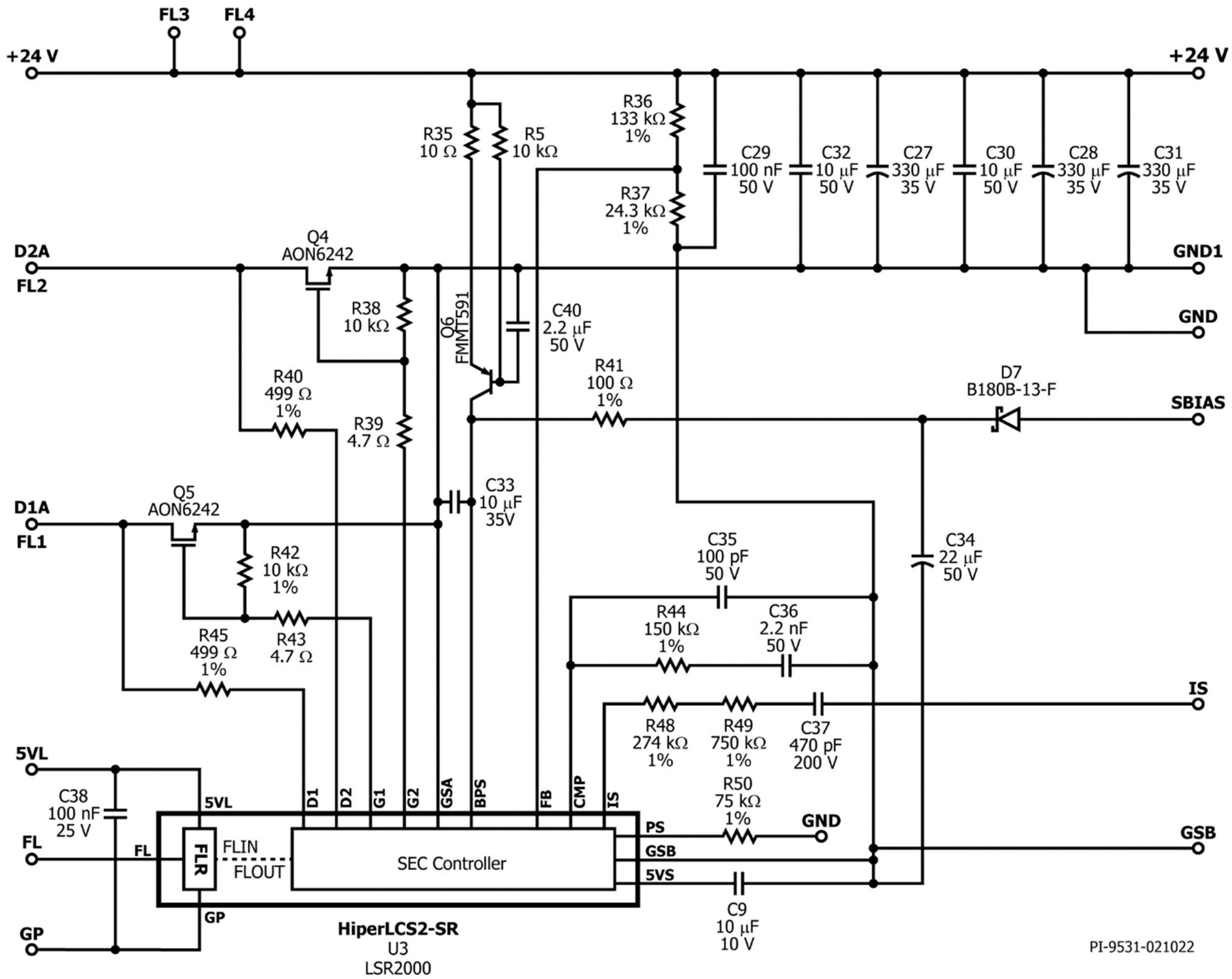


Figure 6– LLC Stage (Secondary Section).

4 Circuit Description

4.1 *EMI Filtering / Inrush Limiting*

Inductors L2 and L3 are used to control common mode noise, while C1, 2, 3 and L4 controls differential mode EMI. Fuse F1 protects in case of a primary side fault/failure. Resistors R1-2 is connected to the integrated x capacitor discharge in the HiperPFS-5 IC to bring down the voltage across C1 and C2 to safe levels when the PSU is disconnected from the AC mains. 2 x 1.3 Ω thermistor are connected in parallel are used for RT1 to limit inrush current during start-up. Capacitors C26 and C42 (Figure 5) serves as path for ESD and CM Surge. Varistor RV1 protect against differential mode line surge.

4.2 *Main PFC Stage*

Components R12-14 and R20 provide output voltage feedback to U1. PFC output voltage is set at 400 VDC (nominal). Components R19 and C15-16 are for loop compensation. Resistors R6, 8, 11 and R15 provides input voltage information to U2. ZVS is achieved by sensing the inductor voltage from an auxiliary winding in the PFC choke that is fed to U1 through resistor R10. Capacitor C9 is used as external bypass capacitor to supply control circuitry inside U1. Capacitor C8 is used as bypass capacitor to supply the driver section of U1. Resistor R16 is used to set the bulk voltage level in which the PG pin will be on high impedance state, this will signal the DC-DC stage to turn off when the bulk voltage is low. Resistor R17 is used to program the power delivery of HiperPFS-5 IC, if left open it will deliver 100% of the nominal power.

4.3 *LLC Converter*

The schematic in Figure 5 shows the primary power section of the LLC containing the integrated half-bridge MOSFETs while Figure 6 shows the main controller/ isolation device of the LLC which allows secondary side feedback sensing and SR management.

4.4 *LLC Primary*

The input bus voltage is filtered by capacitor C10. Resistors R27-28 acts as line sense resistor but instead of sensing the bulk voltage it is referenced to 5VL, LLC will initiate soft-start when PG pin of PFS is pulled low. Primary-side detected output overvoltage is sense from the primary bias-winding (T2-1/2), via Zener diode VR1 and resistor R34. This signal is then coupled to the PP pin via resistor R32 and transistor Q3. When Zener VR1 conducts, current will be pulled from PP pin to ground via transistor Q3. Resistor R33 selects the PP pin programming (primary frequency range and fault-response). Diode D9 may couple from BM pin to an external circuit which could drive an in-rush relay and/or change PFC voltage as a function (BM becomes active during burst mode).

The 5VL and BPL pins are decoupled by capacitors C24 and C22 respectively. Diode D6 rectifies primary bias winding voltage (T1 pin 5) and decouples to capacitor C21, the voltage is fed through resistor R30 to decoupling capacitor C22. Before switching during start-up charge, the bias current comes from the BPL pin and out to capacitor C21 via resistor R30. Capacitor C21 is also intended to supply start-up bias to external PFC stage. Resistor R30 limits output current from BPL in the event of a large current draw from external PFC stage. Diode D5 is used as blocking diode to prevent excessive current draw of the relay from the BP pin during start up charge sequence. During normal operation the bias current comes from the bias winding to capacitor C21. Resistor R31 limits the shunt-current that may be consumed by the BPL pin when clamp BPL internally to ground via shunt regulation, in the event of high bias-winding voltage. Note that the bias winding voltage may vary over a 25% range from zero to full output load. For best no-load performance, the bias winding is intended to deliver a minimum of 15 V to the bias winding at zero load conditions, while the shunt will engage if the bias winding grossly exceeds 21 V.

High-side bootstrap is charged via diode D4, then resistor R23 into capacitor C18 during low-side power MOSFET-on period. Resistor R23 limits the current into capacitor C18 if the capacitor voltage is fully-depleted. Since the C18 charge current flows through the low-side power MOSFET, the removal of resistor R42 may result in safety current limit being triggered under worst-case conditions. Resistor R22 and capacitor C17 provide further low-frequency rejection to the BPL pin. High-side 5VH is decoupled via capacitor C19. Note that all high-side decoupling is with reference to HB potential.

Resonant tank inductor components T2 pins 5/6 (integrated transformer includes resonance LR and magnetizing inductance LM), are connected from HB in series through resonant capacitor C25 to primary return RTN (primary ground).

4.5 *LLC Secondary*

Transformer output pins T2 FL3/FL4 provide the positive output voltage, which is rectified and filtered by capacitors C27, 28, 30, 31 and 32. These capacitors must combine to provide low ESR which mostly defines the output ripple of the system. Also, the C-value of these combined capacitors should be chosen to match the desired burst threshold. These capacitors are decoupled to secondary ground (GND). Transformer output pins T2 FL1/FL2 are the return path rectified via synchronous rectifier MOSFETS Q4 and Q5 to secondary ground. The secondary power path is from T2 FL3/FL4 through capacitors C27, 28, 30, 31 and 32 and returning via Q4, Q5 to transformer T2 FL1/FL2.

The LSR2000C (U3) IC is decoupled at BPS and 5VS pins by capacitors C33-34 and C39. The secondary bias winding T2 pin 12 is rectified via diode D7 and filtered by capacitor C33-34. Components Q6, R35, R5 and C40 acts as fast start-up circuit to provide initial bias to BPS while there is not enough voltage on the bias winding yet to wake up U3, this will prevent overshoot on the output during start-up sequence. Output voltage is sensed via resistor R36 and R37 with local capacitor decoupling C29 to remove any high-frequency noise.

Compensation is provided between CMP and GSB, via components R44/C36 which provide a pole and zero and C35 which adds another pole. The transformer IS winding T1 /9, provides a medium voltage signal which is capacitor coupled via C37 and then via resistors R48, R49 to the IS pin.

The D1/D2 pins sense the synchronous rectifier (Q4, Q5), drain voltages via resistors R40, R45. The resistors are required to limit below-ground current into the D1, D2 pins. These resistor values can be increased to offer adjustment to SR turn-off threshold. Increasing resistor value will cause SR to turn off at higher SR current.

Synchronous MOSFET Q4, Q5 drive is coupled from G1/G2 pins via resistors R39 and R43. The drive resistors are optional and intended to limit super high-frequency MOSFET drive ring. In the case of FMEA open-connection condition from G1/G2 to Q1/Q2 gate, local pull-down resistors R38, R42 are present to ensure the MOSFET Q1, Q2 remain off.

The PS pin resistor R50 selects secondary-side user functions (such as regulation accuracy, CC mode, etc.).

5 PCB Layout

The layouts below show the printed circuit board (PCB) layout used for the unit under test (UUT). Shown are the top and bottom side for reference and information on the connection and routing of the components used.

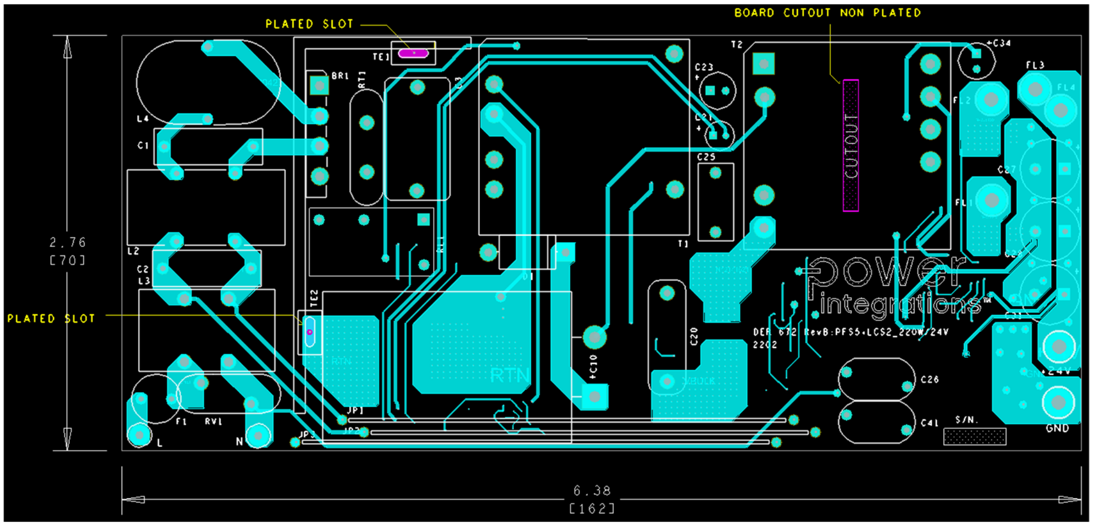


Figure 7 – Printed Circuit Layout, Top Side.

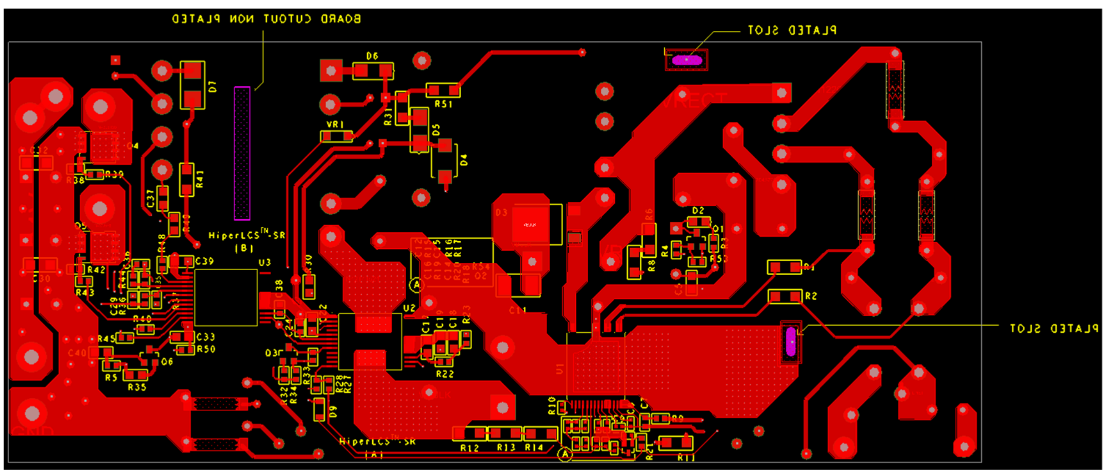


Figure 8 – Printed Circuit Layout, Bottom Side.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	800 V, 8 A, Bridge Rectifier, GBU Case	GBU8K-BP	Micro Commercial
2	1	C1	220 nF, 630 VDC, 20%, Film, X2	B32922C3224M	Epcos
3	1	C2	X2, FILM, 0.47 μF, 20%, 275 VAC, 560 VDC, Polypropylene (PP), Metallized Radial	R46KI347045P2M	Kemet
4	1	C3	FILM, 0.33 μF, 5%, 630 VDC, RADIAL	ECW-F6334JL	Panasonic
5	3	C5 C18 C33	10 μF ±10% 35 V Ceramic X5R 0805	C2012X5R1V106K125AC	TDK
6	1	C7	1 μF, ±10%, 50 V, Ceramic, X5R, -55 °C ~ 85 °C, 0603	CL10A105KB8NNNC	Samsung
7	2	C8 C9	2.2 μF, ±10%, 16 V, Ceramic, X7R, -55 °C ~ 85 °C, 0402	GRM155R61C225KE44D	Murata
8	1	C10	220 μF, 450 V, Electrolytic, (22 x 45)	ESMQ451VSN221MP45S	United Chemi-con
9	1	C11	10 nF, 1 kV, Ceramic, X7R, 1812	VJ1812Y103KXGAT	Vishay
10	2	C12 C14	470 pF, ±5%, 50 V, C0G, NP0, -55 °C ~ 125 °C, Low ESL, 0402	C0402C471J5GACTU	Kemet
11	1	C15	100 nF 16 V, Ceramic, X7R, 0402	L05B104KO5NNNC	Samsung
12	1	C16	1 μF 25 V, Ceramic, X5R, 0402	TMK105BJ105MV-F	Taiyo Yuden
13	2	C17 C22	1 μF, ±10% ,50 V, Ceramic, X7R, Boardflex Sensitive, 0805, -55 °C ~ 125 °C	CGA4J3X7R1H105K125AE	TDK
14	1	C19	220 nF, 25 V, Ceramic, X7R, 0805	CC0805KRX7R8BB224	Yageo
15	1	C20	68 nF, 630 V, Film	ECQ-E6683KF	Panasonic
16	1	C21	47 μF, 25 V, Electrolytic, Very Low ESR, 300 mΩ, (5 x 11)	EKZE250ELL470ME11D	Nippon Chemi-Con
17	1	C23	100 uF, 35 V, Electrolytic, Low ESR, 180 mΩ, (6.3 x 15)	ELXZ350ELL101MF15D	Nippon Chemi-Con
18	1	C24	1 μF 16 V, Ceramic, X7R, 0603	CL10B105KO8VPNC	Samsung
19	1	C25	18 nF, ±5%, 1000 VDC, 600 VAC, Polypropylene Film, -55 °C ~ 100 °C, 0.512" L x 0.236" W (13.00 mm x 6.00 mm) x 0.551" H (14.00 mm)	B32641B0183J	TDK
20	2	C26 C41	2200 pF ±20%, 500 VAC (Y1),760 VAC (X1), Ceramic, Y5U (E), RADIAL	440LD22-R	Vishay
21	3	C27 C28 C31	330 μF, ±20%, 35 V, Aluminum Polymer Radial, Can, 18 mΩ, 1000 Hrs @ 125 °C	35SEK330M	Panasonic
22	1	C29	0.1 μF ±10% 50 V Ceramic X7R 0603	GCM188R71H104KA57D	Murata
23	2	C30 C32	10 μF, 10%, 50 V, Ceramic, X7R, -55 °C ~ 125 °C, 1206, 0.126" L x 0.063" W (3.20 mm x 1.60 mm)	CL31B106KBHNNNE	Samsung
24	1	C34	100 μF, 25 V, Electrolytic, Gen. Purpose, (6.3 x 11)	EKMG250ELL101MF11D	Nippon Chemi-Con
25	1	C35	100 pF 50 V, Ceramic, NP0, 0603	CC0603JRNPO9BN101	Yageo
26	1	C36	2.2 nF 50 V, Ceramic, X7R, 0603	C0603C222K5RACTU	Yageo
27	1	C37	470 pF, 200 V, Ceramic, X7R, 0805	C0805C471K2RACTU	Kemet
28	1	C38	100 nF, 0.1 μF, ±10%, 25 V, Ceramic, X7R, General Purpose, -55 °C ~ 125 °C, 0603	CL10B104KA8NFNC	Samsung
29	1	C39	10 μF ±10% 10 V Ceramic X7R 0805	C2012X7R1A106K125AE	TDK
30	1	C40	2.2 μF, ±10%, 50 V, Ceramic, X7R, 0805	UMK212BB7225KG-T	Taiyo Yuden
31	1	D1	1000 V, 3 A, Recitifier, DO-201AD	1N5408G	ON Semi
32	1	D2	DIODE, GEN PURP, 75 V 150 mA, SOD323	1N4148WS-7-F	Diodes, Inc.
33	1	D3	Diode, Standard, 600 V, 5 A, SMT, D-PAK (TO-252AA), TO-252-3, DPak (2 Leads + Tab), SC-63	VS-5EWH06FNTR-M3	Vishay
34	1	D4	600 V, 1 A, Ultrafast Recovery, 35 ns, SMB Case	MURS160T3G	On Semi
35	1	D5	50 V, 1 A, General Purpose, DO-214AC	ES1A-13-F	Diodes, Inc.
36	1	D6	200 V, 1 A, Fast Recovery, 150 ns, SMA	RS1D-13-F	Diodes, Inc.
37	1	D7	80 V, 1 A, Schottky, SMD, DO-214AA	B180B-13-F	Diodes, Inc.
38	1	D9	75 V, 0.15 A, Switching, SOD-323	BAV16WS-7-F	Diodes, Inc.
39	1	F1	5 A, 250 V, Slow, TR5	37215000411	Wickman
40	1	HTSK1	Custom Bridge Rectifier Heat Sink		Power Integrations

41	2	JP1 JP2	Wire Jumper, Insulated, #24 AWG, 3.0 in	C2003A-12-02	Gen Cable
42	1	JP3	Wire Jumper, Non-insulated, #22 AWG, 3.2 in	298	Alpha
43	1	L2	9 mH, 5 A, Common Mode Choke	T22148-902S P.I. Custom	Fontaine
44	1	L3	Custom CMC, 0.6 mH, ±15%		Power Integrations
45	1	L4	330 μH, 3.3 A, Vertical Toroidal	2218-V-RC	Bourns
46	1	LINE1	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
47	1	NEUTRAL1	Test Point, YEL, THRU-HOLE MOUNT	5014	Keystone
48	1	Q1	MOSFET, N-CH, 60 V, 0.5 A (Ta),0.3 W (Ta) , -55 °C ~ 150 °C (TJ), TO-236-3, SC-59, SOT-23-3	MMBF170-7-F	Diodes, Inc.
49	1	Q3	NPN, Small Signal BJT, 80 V, 0.5 A, SOT-23	MMBTA06LT1	Infineon Tech
50	2	Q4 Q5	60 V, 85 A N-Channel, DFN5X6	AON6242	Alpha & Omega Semi
51	1	Q6	PNP, 60 V 1000 mA, SOT-23	FMMT591TA	Zetex
52	2	R1 R2	RES, 75.0 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF7502V	Panasonic
53	3	R3 R9 R22	RES, 10 Ω, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF10R0V	Panasonic
54	5	R5 R34 R38 R42 R53	RES, 10 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
55	3	R6 R8 R13	RES, 6.2 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ625V	Panasonic
56	1	R10	RES, 10.0 kΩ, 1%, 1/16 W, Thick Film, 0402	RC0402FR-0710KL	Yageo
57	2	R11 R12	RES, 3.74 MΩ, 1%, 1/4 W, Thick Film, 1206	CRCW12063M74FKEA	Vishay
58	1	R14	RES, 6.2 MΩ, 1%, 1/4 W, Thick Film, 1206	KTR18EZPF6204	Rohm Semi
59	1	R15	RES, 165.0 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF1653X	Panasonic
60	1	R16	RES, 280.0 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF2803X	Panasonic
61	1	R19	RES, 30.1 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF3012X	Panasonic
62	1	R20	RES SMD 158 kΩ 1% 1/10 W 0402	ERJ-2RKF1583X	Panasonic
63	1	R23	RES, 2.2 Ω, 1%, 1/16 W, Thick Film, 0603	ERJ-3RQF2R2V	Panasonic
64	1	R27	RES, 22.6 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF2262V	Panasonic
65	1	R28	RES, 20 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ203V	Panasonic
66	1	R30	RES, 2.2 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ2R2V	Panasonic
67	1	R31	RES, 750 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF7500V	Panasonic
68	1	R32	RES, 47 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ473V	Panasonic
69	1	R33	RES, 158 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1583V	Panasonic
70	1	R35	RES, 10 Ω, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF10R0V	Panasonic
71	1	R36	RES, 133 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1333V	Panasonic
72	1	R37	RES, 24.3 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF2432V	Panasonic
73	2	R39 R43	RES, 4.7 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ4R7V	Panasonic
74	2	R40 R45	RES, 499 Ω, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF4990V	Panasonic
75	1	R41	RES, 100 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1000V	Panasonic
76	1	R44	RES, 150 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1503V	Panasonic
77	1	R48	RES, 274 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF2743V	Panasonic
78	1	R49	RES, 750 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF7503V	Panasonic
79	1	R50	RES, 75 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ753V	Panasonic
80	1	R51	RES, 10 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF10R0V	Panasonic
81	2	RT1 RT2	NTC Thermistor, 1.3 Ω, 7 A	MF72-001.3D13	Cantherm
82	1	RV1	320 Vac, 80 J, 14 mm, RADIAL	V320LA20AP	Littlefuse
83	1	T1	140 μH ±5%, PFC Choke, Custom for DER-672		Power Integrations
84	1	T2	470 μH ±5%, LLC Transformer, Custom for DER-672		Power Integrations
85	1	U1	HiperPFS-5, InSOP-T28F	PFS5178F	Power Integrations
86	1	U2	HiperLCS2-HB, InSOP-24C	LCS7265C	Power Integrations
87	1	U3	HiperLCS2-SR, InSOP-24D	LSR2000C	Power Integrations
88	1	VR1	DIODE ZENER 30 V 500 mW SOD123	MMSZ5256B-7-F	Diodes, Inc.

7 Magnetics

7.1 *PFC Choke (T1) Specification*

7.1.1 *Electrical Diagram*

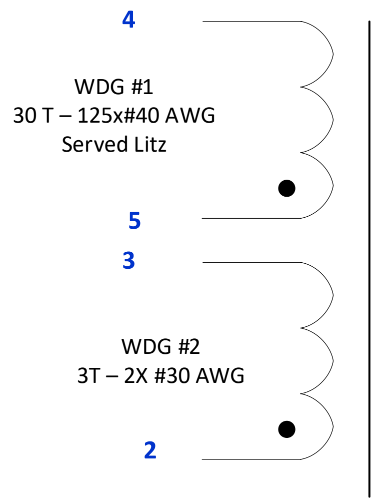


Figure 9 – PFC Choke Electrical Diagram.

7.1.2 *Electrical Specifications*

Inductance	Pins 4-5 measured at 100 kHz, 0.4 RMS.	140 µH ±5%
Resonant Frequency	Pins. N/A	kHz (Min.)

7.1.3 *Material List*

Item	Description
[1]	Core: TDK PC95PQ32/20Z-12. **PI P/N 99-00028-00**
[2]	Bobbin: PQ32/20, Vertical, 12 Pins. **PI P/N 25-00077-00**
[3]	Litz Wire: 125 x #40 AWG Single Coated Solderable, Served.
[4]	2X #30 AWG.
[5]	Tape, Polyester Film: 3M 1350-F1 or Equivalent, 9 mm Wide.
[6]	Tape, Copper. 3M 1181 or Equivalent. 6.4 mm Wide.
[7]	Varnish: Dolph BC-359, or Equivalent.

7.1.4 *Inductor Build Diagram*

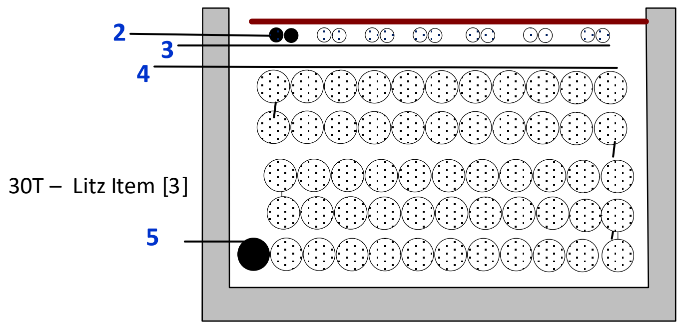


Figure 10 – PFC Inductor Build Diagram.

7.1 LLC Transformer (T2) Specification

7.1.5 *Electrical Diagram*

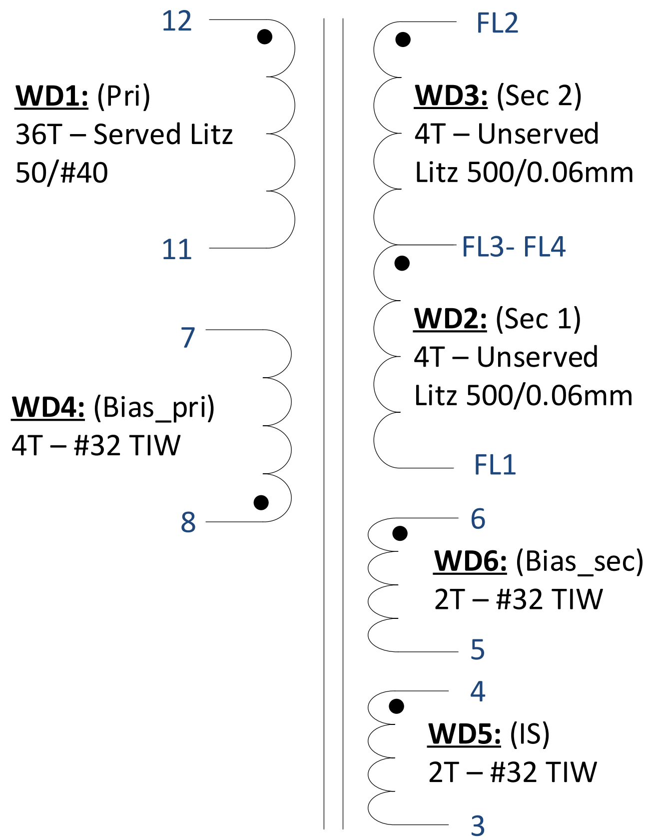


Figure 11 – LLC Transformer Electrical Diagram.

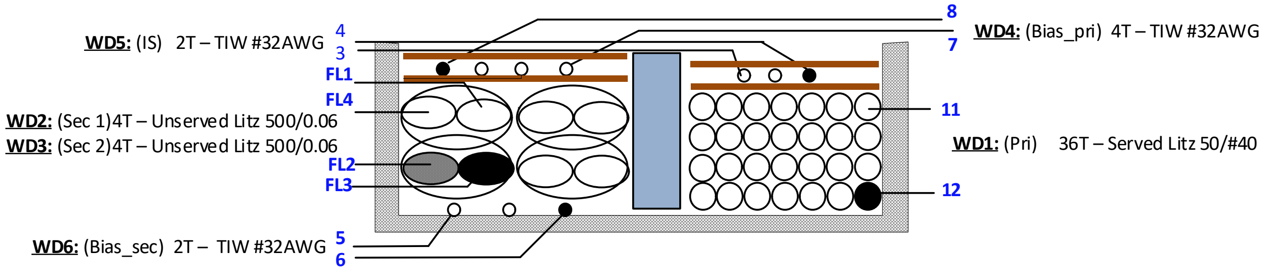
7.1.1 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 3, 4, 5, 6, FL1-FL3, FL2-FL4 to pins 7, 8, 11, 12.	3000 VAC
Primary Inductance (Lpri)	Pins 7-8, all other windings open, measured at 100 kHz, 1 V_{RMS}	470 μH ±5%
Primary Leakage1 (LlkpALL)	Pins 7-8, short **ALL** other pins except IS-winding, measured at 100 kHz, 1 V_{RMS}	88.0 μH ±5%
Primary Leakage2 (LkpIS)	Measured at pins 7-8 (100 kHz, 1 V_{RMS}), Short **ONLY** IS-winding Pins 3&4.	15 μH
Primary Leakage3 (LkpSEC1)	Measured at pins 7-8 (100 kHz, 1 V_{RMS}), Short **ONLY** FL2, FL3, FL4	90 μH
Primary Leakage4 (LkpSEC2)	Measured at pins 7-8 (100 kHz, 1 V_{RMS}), Short **ONLY** FL1, FL3, FL4	90 μH
Primary side Cres		18 nF
Resonant Frequency (fres)	Fseries = 1/ (2.pi*sqrt(LlkpALL.Cres)	125 kHz

7.1.2 Material List

Item	Description
[1]	Core: ETD34 – 3C97 (Ferroxcube) or Equivalent.
[2]	Bobbin with Cover: ETD34-H, 12 Pins (6/6).
[3]	Litz Wire: 50/ #40 AWG_Served Litz.
[4]	Litz Wire: 500/0.060 mm_Unserved Litz.
[5]	Triple Insulated Wire: #32 AWG.
[6]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 13 mm Wide.
[7]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 20 mm Wide.

7.1.3 Build Diagram



Notes: ***1. WD2(SEC1) & WD3(SEC2) must exit at the bottom side of the bobbin on removed pins 1&2.***
2. Wire leads 7&8(WD4) should be twisted together before crossing the isolation barrier.
3. Wire leads 3&4(WD5) should be twisted together before crossing the isolation barrier.

Figure 12 – LLC Transformer Build Diagram.

7.2 Common Mode Choke (L3) Specification

7.2.1 Electrical Diagram

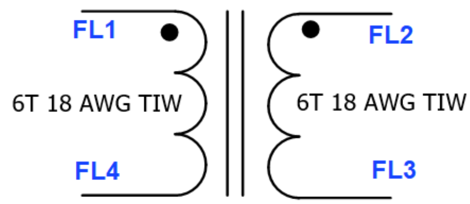


Figure 13 – Inductor Electrical Diagram.

7.2.2 Electrical Specifications

Inductance	FL1-4 or FL2-3, measured at 100 kHz, 0.4 V_{RMS}	0.6 mH, ±15%

7.2.3 Material List

Item	Description
[1]	Ferrite Core Toroid: Encom Ltd., YJ15K-T18/10/7C.
[2]	Triple Insulated Wire: #18 AWG, Solderable Double Coated.
[3]	Triple Insulated Wire: #18 AWG, Furukawa TEX-E or Equivalent.

7.2.4 Construction Details

Figure 14 – Finished Part, Front View.

8 PFC Design Spreadsheet

In this design, the spreadsheet generated warnings to select higher size device for the specified output power, in this case 10 W above the nominal output power of 220 W still leaves enough margin before output voltage starts drooping.

A warning for current density indicates that the design should be checked in its initial stages for excessive temperature rise in the PFC inductor. The guidelines incorporated the spreadsheet are conservative, so that a warning does not necessarily mean that a given design will fail thermally. **The measured temperature and efficiency for this design was satisfactory.**

1	Hiper_PFS-5_Boost_031422; Rev.0.3; Copyright Power Integrations 2022	INPUT	INFO	OUTPUT	UNITS	Discontinuous Mode Boost Converter Design Spreadsheet
2	**Enter Application Variables**					
3	Input Voltage Range	Universal		Universal		Input voltage range
4	VACMIN			90	VAC	Minimum AC input voltage. Spreadsheet simulation is performed at this voltage. To examine operation at other votlages, enter here, but enter fixed value for LPFC_ACTUAL.
5	VACMAX			265	VAC	Maximum AC input voltage
6	VBROWNIN			82	VAC	Expected Typical Brown-in Voltage per IC specifications; Line impedance not accounted for.
7	VBROWNOUT			71	VAC	Expected Typical Brown-out voltage per IC specifications; Line impedance not accounted for.
8	VO			400	VDC	Nominal load voltage
9	PO	230		230	W	Nominal Output power
10	fL			50	Hz	Line frequency
11	TA Max			40	°C	Maximum ambient temperature
12	Efficiency Estimate	0.9500		0.9500		Enter the efficiency estimate for the boost converter at VACMIN. Should approximately match calculated efficiency in Loss Budget section
13	VO_MIN			380	VDC	Minimum Output voltage
14	VO_RIPPLE_MAX			20	VDC	Maximum Output voltage ripple
15	T_HOLDUP			20	ms	Holdup time
16	VHOLDUP_MIN			320	VDC	Minimum Voltage Output can drop to during holdup
17	I_INRUSH			40	A	Maximum allowable inrush current
18	Forced Air Cooling	No		No		Enter "Yes" for Forced air cooling. Otherwise enter "No". Forced air reduces acceptable choke current density and core autopick core size
20	**KP and INDUCTANCE**					
21	LPFC_MIN (0 bias)			130	uH	Minimum PFC inductance value
22	LPFC_TYP (0 bias)			137	uH	LPFC value used for calculations. Enter value to hold constant (also enter core selection) while changing VACMIN to examine brownout operation.
23	LPFC_MAX (0 bias)			144	uH	Maximum PFC inductance value
24	LP_TOL			5.0	%	Tolerance of PFC Inductor Value (ferrite only)
25	LPFC_PEAK			137	uH	Inductance at VACMIN and maximum bias current. For Ferrite, same as LPFC_DESIRED (0 bias)
26	KP_ACTUAL			1.11		Actual KP calculated from LPFC_DESIRED
28	**Basic Current Parameters**					
29	IAC_RMS			2.69	A	AC input RMS current at VACMIN and Full Power load
30	IL_RMS			3.15	A	Inductor RMS current (calculated at VACMIN and Full Power Load)
31	IO_DC			0.58	A	Output average current/Average diode current
34	**PFS Parameters**					
35	PFS Package			F		HiperPFS package selection
36	PFS Part Number	PFS5178F		PFS5178F		If examining brownout operation, over-ride autopick with desired device size

37	Self-Supply Feature	Yes		Yes		Device self-supply feature. Select "Yes" to select device with self-supply feature or "No" for device without self-supply
38	PS_FACTOR	1.0		1.0		Programmable output power selection factor
39	PO_MAX_DEV			240	W	Maximum output power of the device
40	IOCP min			8.10	A	Minimum Current limit
41	IOCP typ			9.30	A	Typical current limit
42	IOCP max			10.20	A	Maximum current limit
43	IP			7.07	A	MOSFET peak current
44	IRMS			2.73	A	PFS MOSFET RMS current
45	RDSON			0.21	Ohms	Typical RDSon at 100 'C
46	FS_PK			85.9	kHz	Estimated frequency of operation at crest of input voltage (at VACMIN)
47	FS_AVG			75.5	kHz	Estimated average frequency of operation over line cycle (at VACMIN)
48	PCOND_LOSS_PFS			1.568	W	Estimated PFS Switch conduction losses
49	PSW_LOSS_PFS			0.030	W	Estimated PFS Switch switching losses
50	PFS_TOTAL			1.598	W	Total Estimated PFS Switch losses
51	TJ Max			100	deg C	Maximum steady-state junction temperature
52	Rth-JS			2.80	°C/W	Maximum thermal resistance (Junction to heatsink)
53	HEATSINK Theta-CA			34.75	°C/W	Maximum thermal resistance of heatsink
56	**INDUCTOR DESIGN**					
57	**Material and Dimensions**					
58	Core Type	Ferrite		Ferrite		Enter "Sendust", "Iron Powder" or "Ferrite"
59	Core Material	PC44/PC95		PC44/PC95		Select from 60u, 75u, 90u or 125 u for Sendust cores. Fixed at PC44/PC95 for Ferrite cores. Fixed at -52 material for Pow Iron cores.
60	Core Geometry	PQ		PQ		Toroid only for Sendust and Powdered Iron; EE or PQ for Ferrite cores.
61	Core	PQ32/20		PQ32/20		Core part number
62	Ae			170.00	mm^2	Core cross sectional area
63	Le			55.50	mm	Core mean path length
64	AL			6530.00	nH/t^2	Core AL value
65	Ve			9.44	cm^3	Core volume
66	HT (EE/PQ/EQ/RM/POT) / ID (toroid)			5.12	mm	Core height/Height of window; ID if toroid
67	MLT			67.1	mm	Mean length per turn
68	BW			8.98	mm	Bobbin width
69	LG			1.32	mm	Gap length (Ferrite cores only)
70	**Flux and MMF Calculations**					
71	BP_TARGET (ferrite only)	2900		2900	Gauss	Target flux density at worst case: IOCP and maximum tolerance inductance (ferrite only) - drives turns and gap
72	B_OCP (or BP)			2880	Gauss	Target flux density at worst case: IOCP and maximum tolerance inductance (ferrite only) - drives turns and gap
73	B_MAX			1899	Gauss	Peak flux density at AC peak, VACMIN and Full Power Load, nominal inductance,minimum IOCP
74	μ_TARGET (powder only)			N/A	%	target μ at peak current divided by μ at zero current, at VACMIN, full load (powder only) - drives auto core selection
75	μ_MAX (powder only)			N/A	%	actual μ at peak current divided by μ at zero current, at VACMIN, full load (powder only)

76	µ_OCP (powder only)			N/A	%	µ at IOCPtyp divided by µ at zero current
77	I_TEST			9.3	A	Current at which B_TEST and H_TEST are calculated, for checking flux at a current other than IOCP or IP; if blank IOCP_typ is used.
78	B_TEST			2626	Gauss	Flux density at I_TEST and maximum tolerance inductance
79	µ_TEST (powder only)			N/A	%	µ at IOCP divided by µ at zero current, at IOCPtyp
80	**Wire**					
81	TURNS			30		Inductor turns. To adjust turns, change BP_TARGET (ferrite) or µ_TARGET (powder)
82	ILRMS			3.15	A	Inductor RMS current
83	Wire type	Litz		Litz		Select between "Litz" or "Magnet" for double coated magnet wire
84	AWG	40		40	AWG	Inductor wire gauge
85	Filar	125		125		Inductor wire number of parallel strands. Leave blank to auto-calc for Litz
86	OD (per strand)			0.079	mm	Outer diameter of single strand of wire
87	OD bundle (Litz only)			1.23	mm	Will be different than OD if Litz
88	DCR			0.074	ohm	Choke DC Resistance
89	P AC Resistance Ratio			0.42		Ratio of total copper loss, including HF AC, to the DC component of the loss
90	J			5.18	A/mm^2	Estimated current density of wires. It is recommended that 4 < J < 6
91	FIT		Warning	99	%	Windings may not fit on this inductor. Use bigger core or reduce KP or reduce wire gauge if possible
92	Layers			4.34		Estimated layers in winding
93	**Loss Calculations**					
94	BAC-p-p			1834	Gauss	Core AC peak-peak flux excursion at VACMIN, peak of sine wave
95	LPFC_CORE_LOSS			0.242	W	Estimated Inductor core Loss
96	LPFC_COPPER_LOSS			0.824	W	Estimated Inductor copper losses
97	LPFC_TOTAL_LOSS			1.066	W	Total estimated Inductor Losses
100	**PFC Diode**					
101	PFC Diode Part Number	Auto		LXA06T600		PFS Diode Part Number
102	Type / Part Number			Qspeed		PFC Diode Type / Part Number
103	Manufacturer			PI		Diode Manufacturer
104	VRRM			600.0	V	Diode rated reverse voltage
105	IF			6.00	A	Diode rated forward current
106	Qrr			71.0	nC	Qrr at High Temperature
107	VF			2.00	V	Diode rated forward voltage drop
108	PCOND_DIODE			1.163	W	Estimated Diode conduction losses
109	PSW_DIODE			0.000	W	Estimated Diode switching losses
110	P_DIODE			1.163	W	Total estimated Diode losses
111	TJ Max			100.0	deg C	Maximum steady-state operating temperature
112	Rth-JS			2.00	degC/W	Maximum thermal resistance (Junction to heatsink)
113	HEATSINK Theta-CA			49.11	degC/W	Maximum thermal resistance of heatsink
114	IFSM			50.0	A	Non-repetitive peak surge current rating. Consider larger size diode if inrush or thermal limited.
117	**Output Capacitor**					
118	COUT	220		220	uF	Minimum value of Output capacitance
119	VO_RIPPLE_EXPECTED			8.8	V	Expected ripple voltage on Output with selected Output capacitor

120	T_HOLDUP_EXPECTED			27.5	ms	Expected holdup time with selected Output capacitor
121	ESR_LF			0.92	ohms	Low Frequency Capacitor ESR
122	ESR_HF			0.37	ohms	High Frequency Capacitor ESR
123	IC_RMS_LF			0.37	A	Low Frequency Capacitor RMS current
124	IC_RMS_HF			1.41	A	High Frequency Capacitor RMS current
125	CO_LF_LOSS			0.124	W	Estimated Low Frequency ESR loss in Output capacitor
126	CO_HF_LOSS			0.734	W	Estimated High frequency ESR loss in Output capacitor
127	Total CO LOSS			0.858	W	Total estimated losses in Output Capacitor
130	**Input Bridge (BR1) and Fuse (F1)**					
131	I^2t Rating			15.45	A^2*s	Minimum I^2t rating for fuse
132	Fuse Current rating			4.13	A	Minimum Current rating of fuse
133	VF			0.90	V	Input bridge Diode forward Diode drop
134	IAVG			2.57	A	Input average current at VBROWNOUT.
135	PIV_INPUT BRIDGE			375	V	Peak inverse voltage of input bridge
136	PCOND_LOSS_BRIDGE			4.360	W	Estimated Bridge Diode conduction loss
137	CIN	0.33		0.33	uF	Input capacitor. Use metallized polypropylene or film foil type with high ripple current rating
138	CIN_DF			0.001		Input Capacitor Dissipation Factor (tan Delta)
139	CIN_PLOSS			0.020	W	Input Capacitor Loss
140	RT1			9.37	ohms	Input Thermistor value
141	D_Precharge			1N5407		Recommended precharge Diode
144	**PFS5 Small Signal Components**					
145	RVS			10.0	kOhms	VS pin resistor for valley sensing. This resistor should be optimized such that proper delay is introduced from the instant the voltage on the sense winding goes below the Vvs2 threshold to the instant when the cascode turns-on (valley sensing). Must be tested on the bench
146	RPS			> 400	kOhms	Power programmability resistor. Leaving PS pin open is acceptable
147	RV1			4.0	MOhms	Line sense resistor 1
148	RV2			6.0	MOhms	Line sense resistor 2
149	RV3			6.0	MOhms	Typical value of the lower resistor connected to the V-PIN. Use 1% resistor only!
150	RV4			155.5	kOhms	Description pending, could be modified based on feedback chain R1-R4
151	C_V			0.514	nF	V pin decoupling capacitor (RV4 and C_V should have a time constant of 80us) Pick the closest available capacitance.
152	C_VCC			1.0	uF	Supply decoupling capacitor
153	C_C			100	nF	Feedback C pin decoupling capacitor
154	Power good Vo lower threshold VPG(L)	280		280	V	Vo lower threshold voltage at which power good signal will trigger
155	PGT set resistor			269.5	kohm	Power good threshold setting resistor
158	**Feedback Components**					
159	RFB_1			4.00	Mohms	Feedback network, first high voltage divider resistor
160	RFB_2			6.00	Mohms	Feedback network, second high voltage divider resistor
161	RFB_3			6.00	Mohms	Feedback network, third high voltage divider resistor
162	RFB_4			155.5	kohms	Feedback network, lower divider resistor

163	CFB_1			0.514	nF	Feedback network, loop speedup capacitor. (R4 and C1 should have a time constant of 80us) Pick the closest available capacitance.
164	RFB_5			40.2	kohms	Feedback network: zero setting resistor
165	CFB_2			1000	nF	Feedback component- noise suppression capacitor
168	**Loss Budget (Estimated at VACMIN)**					
169	PFS Losses			1.598	W	Total estimated losses in PFS
170	Boost diode Losses			1.163	W	Total estimated losses in Output Diode
171	Input Bridge losses			4.360	W	Total estimated losses in input bridge module
172	Input Capacitor Losses			0.020	W	Total estimated losses in input capacitor
173	Inductor losses			1.066	W	Total estimated losses in PFC choke
174	Output Capacitor Loss			0.858	W	Total estimated losses in Output capacitor
175	EMI choke copper loss			0.724	W	Total estimated losses in EMI choke copper
176	Total losses			9.788	W	Overall loss estimate
177	Efficiency			95.92	%	Estimated efficiency at VACMIN, full load.
180	**HiperPFS-5 Integrated CAPZero Function**					
181	Total Series Resistance (Rcapzero1+Rcapzero2)			0.730	MOhms	Maximum total series resistor value to discharge X-capacitors with time constant of 1 second. Resistors must be connected to D1 and D2 pins of the HiperPFS-5 part for integrated CAPZero function
184	**EMI Filter Components Recommendation**					
185	CX2			470	nF	X-capacitor after differencial mode choke and before bridge, ratio with Po
186	LDM_calc			317	uH	Estimated minimum differential inductance to avoid <10kHz resonance in input current
187	CX1			470	nF	X-capacitor before common mode choke, ratio with Po
188	LCM			10.0	mH	Typical common mode choke value
189	LCM_leakage			30	uH	Estimated leakage inductance of CM choke, typical from 30~60uH
190	CY1 (and CY2)			220	pF	typical Y capacitance for common mode noise suppression
191	LDM_Actual			287	uH	cal_LDM minus LCM_leakage, utilizing CM leakage inductance as DM choke.
192	DCR_LCM			0.070	Ohms	Total DCR of CM choke for estimating copper loss
193	DCR_LDM			0.030	Ohms	Total DCR of DM choke(or CM #2) for estimating copper loss
195	**Note: CX2 can be placed between CM choke and DM choke depending on EMI design requirement.**					

9 LLC Transformer Design Spreadsheet

1	ACDC_HiperLCS2_031622; Rev.1.0; Copyright Power Integrations 2022	INPUT	INFO	OUTPUT	UNITS	LCS2 Design Spreadsheet
2	General					
3	Description			>		LCS7265C-360W-24V-15A-SynchRF-36T-4T-380uH-88uH-18nF-128kHz
4	Input Parameters					
5	VIN MIN	280		280	V	Brownout Threshold Voltage
6	VIN RES	400		400	V	Input Voltage at Resonance - lower Vres to lower Npri
7	VIN NOM	400		400	V	Nominal Input Voltage - default CRM Vres=Vnom (or DCM Vres>Vnom, CCM Vres<Vnom)
8	VIN MAX			430	V	Maximum Input Voltage - decrease Vmax to lower Fmax
9	PFC	YES		YES		Input Option
10	Output Parameters					
11	Vout1			24.00	V	Main Output Voltage
12	Iout1 PK	15.0		15.0	A	Peak Main Output Current - default = 200% of Iout1Cont - used to select device size - higher power lower Llk
13	Pout1 PK			360.0	W	Main Output Peak Power
14	Iout1 CONT	9.2		9.2	A	Continuous Main Output Current - default 50% of Ppeak - used to select device size - losses calculated at this power level
15	Pout1 CONT			220.8	W	Continues Main Output Power
16	External CC	NO		NO		Use external CC operation
17	Vout1 Min (CC)				V	Minimum Output Voltage when operating in CC - lower VoutMin lowers Lm and also lowers efficiency
18	VCC				V	Output current sense resistor voltage when operating at CC-threhsold
19	RCC				mOhm	Output current sense resistor value
20	RCC Rated Power				W	Output current sense resistor rated power
21	Estimated Prameters, Design Choices and Selections					
22	FS Range	1		1		Frequency Range
23	FS Vnom (Target)			120.0	kHz	Switching Frequency at VinNom
24	Output Rectifier	SynchRF		SynchRF		Output Rectifier
25	Ron_SR1	3.6		3.6	mOhms	Sync. Rectifier ON Resitance
26	VF_SR1	0.7		0.7	V	Output Diode Average Voltage Drop
27	Design Results					
28	DESIGN RESULT			Design Passed		Current Design Status
29	Device Variables					
30	DEVNAME	LCS7265C		LCS7265C		PI Device Name

31	COSS			166	pF	Equivalent Coss of selected device
32	RDSON			0.410	Ohms	RDSON of selected device
33	Fault Responce	NON_LATCHING		NON_LATCHING		..
34	**Tank Circuit Components & Operation Frequency Range**					
35	LP Nominal			468.04	uH	Nominal Primary Inductance
36	Lm			380.0	uH	Magnetizing inductance of transformer - modified by Kz, Device size and frequency
37	Lres			88.1	uH	Series resonant or primary leakage inductance - modified by Pmax
38	Cres	18.00		18.00	nF	Series resonant capacitor.
39	f_calc@Vbrownout			83.4	kHz	Frequency at PoutCont at Vbrownout, full load - adjust VinBrownout
40	f_calc@resonance			126.4	kHz	Frequency at PoutCont at Vres (defined by Lres and Cres) - adjust Vres)
41	f_calc@Vnom			127.6	kHz	Frequency at PoutCont at Vnom - adjust FS Vnom Target or Vnom
42	f_calc@Vinmax			137.1	kHz	Expected frequency at maximum input voltage and full load; Heavily influenced by n_eq and primary turns
43	VINGmaxInversion			253.0	V	Minimum Input Voltage for negative Gain at 100% load. Below this voltage the Gain becomes positive (unstable loop)
44	**Core Dimensions/TRF Mechanical Parameters**					
45	AE			97.00	mm^2	Transformer Core Cross-sectional area
46	VE			7.6	cm^3	Transformer Core Volume
47	MLT			56.90	mm	Middle Length of a Turn
48	AW			160.60	mm^2	Core Window area
49	BW			20.90	mm	Bobbin Winding Width
50	Bobbin Chambers			2		Bobbin Chambers
51	ChambDist	3.20		3.20	mm	Width of bobbin with no windings - empty space between primary/secondary generates leakage inductance
52	Bobbin Height			5.38	mm	Height of the bobbin, maximum Stack height
53	Prim. Bobbin Chamber Width			5.16	mm	Part of the bobbin allocated for primary
54	Sec. Bobbin Chamber Width			12.54	mm	Part of the bobbin allocated for secondary
55	K-PD			0.35		Penetration Depth multiplier (for Single Strand LITZ calulation)
56	**Transformer Generic Parameters**					
57	CR_TYPE	ETD34		ETD34		Transformer Core Type
58	FR_TYPE	Auto		3F3		Magnetic material used
59	BACmax Actual			251.79	mT	Estmated Flux Density at Vnom - increase Ns to reduce Bmax

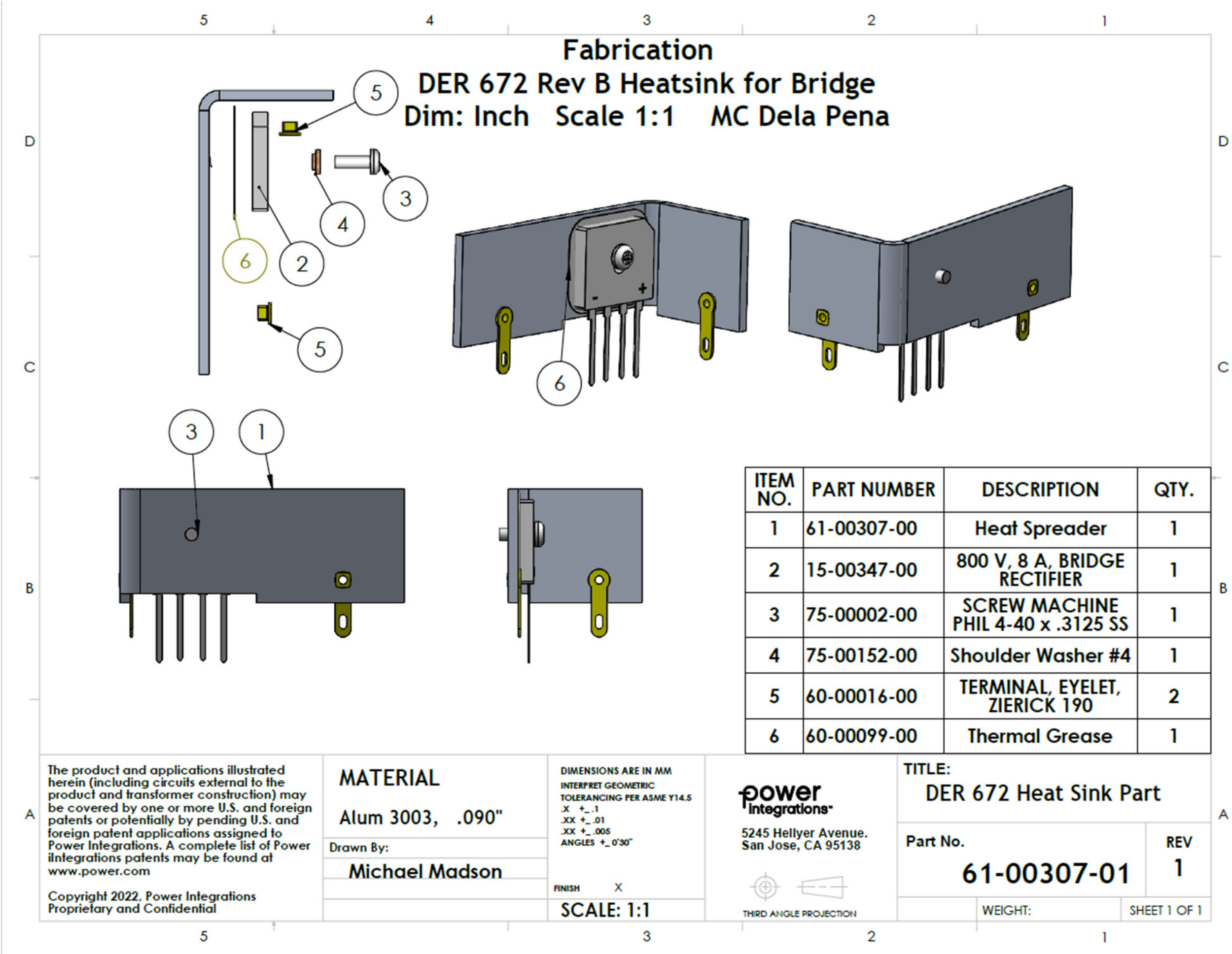
60	Use Litz Primary	YES		YES		Primary Windings Bundled (served) Yes/No
61	Use Litz Secondary	YES		YES		Secondary Windings Bundled (served) Yes/No
62	Fixed Litz Bundles	NO		NO		Use preferred Litz Wire Bundles (yes) - or use customer bundle (no)
63	kSecChamb	0.60		0.60		Percentage of Bobbin Chamber Width used for Secondary Windings - Adjust to change Used Percentage of Primary/Secondary Windows
64	**Transformer Primary Parameters**					
65	Npri			36		Calculated Primary Winding Total Number of Turns
66	Iprim RMS			1.24	A	Transformer Primary Winding RMS Current at PoutCont and VinNom
67	Prim. Wire Type			LITZ		Primary Wire Type
68	Primary LIz Wire Type	SERVED		SERVED		Litz Insulation type, SERVED bundled with sleave, UNSERVED loose wires
69	Target Prim. Current density			6.0	A/mm^2	Primary current density target - reduce target to increase copper
70	Prim. Single Strand Wire Gauge			40	AWG	Single Strand Gauge (LITZ) / AWG (ECW)
71	Prim. Single Strand Diameter			0.08	mm	Primary Single Strand Copper Diameter
72	Number of Prim. Strands	50		50		Prim. Number of Strands (LITZ) / Fillars (ECW)
73	Actual Prim. Current Density			4.95	A/mm^2	Actual Primary Current Density
74	Actual Prim. Copper Diameter			0.57	mm	Primary Equivalent Total Copper Diameter
75	Actual Prim. External Diameter			0.72	mm	Primary Wire External Diameter (bundle size - copper plus insulation plus fill)
76	Layers Primary			5.14		Not Rouned Primary number of layers
77	Primary Window Usage			80.75	%	Used Percentage of Available Primary Winding Window - Maximum copper gives 100%
78	**Main Output Parameters**					
79	NSec	4		4		Secondary Number of Turns
80	ISRMS			11.70	A	Transformer Secondary Winding RMS Current
81	Sec. Wire Type			LITZ		Main Output Wire Type
82	Secondary LIZ Wire type	UNSERVED		UNSERVED		Litz Insulation type, SERVED bundled with sleave, UNSERVED loose wires
83	Target Sec. Current density			8.0	A/mm^2	Secondary current density target - reduce target to increase copper
84	Sec. Single Strand Wire Gauge	40		40	AWG	Single Strand Gauge (LITZ) / AWG (ECW)

85	Sec. Single Strand Diameter			0.08	mm	Secondary Single Strand Copper Diameter
86	Number of Sec. Strands	500		500		Sec. Number of Strands (LITZ) / Fillars (ECW)
87	Actual Sec. Curr Density			4.65	A/mm^2	Sec. Actual Current Density
88	Actual Sec. Copper Diameter			1.79	mm	Secondary Equivalen Total Copper Diameter
89	Actual Sec. External Diameter			2.29	mm	Secondary Wire External Diameter(bundle size - copper plus insulation plus fill)
90	Layers Secondary			1.60		Not Rouned Secondary number of layers
91	Secondary Window Usage			85.12	%	Used Percentage of Available Secondary Winding Window - Maximum copper gives 100%
92	**Losses**					
93	CoreLoss			1.56	W	Core Losses at VinNom
94	Pr.WindLoss			0.35	W	Primary Winding Losses at VinNom and PoutCont
95	Sec.WindLoss			0.29	W	Secondary Winding Losses at VinNom and PoutCont
96	CO ESR Loss			0.05	W	Secondary Winding Losses at VinNom and PoutCont
97	PLOSS Switch			0.32	W	Single Primary Switch Conduction Loss at VinNom and PoutCont
98	PLOSS Output Rectifier			0.19	W	Single Output Rectifier Conduction Loss at VinNom and PoutCont
99	PLOSS RCC			0.00	W	Current sense resisitor power loss at VinNom and PoutCont
100	PLOSS Total			3.27	W	Total Loss at VinNom and PoutCont
101	**Circuit Components**					
102	RZ1			150	kOhm	Control Zero (boost high-frequency gain)
103	CP2			100	pF	Control Pole2 (roll-off high-frequency gain)
104	Cp1			2.2	nF	Control Pole1 (roll-off low-frequency gain)
105	Resr CO			1.00	mOhms	ESR of the output capacitor
106	COmin			1618	uF	Min CO to satisfy burst conditions
107	RD1			500	Ohm	RD1 Resistor value
108	RD2			500	Ohm	RD2 Resistor value
109	CBPL			1	uF	CBPL Capacitor Value /25V
110	CBPH			1	uF	CBPH Capacitor Value /25V
111	C5VL			1	uF	C5VL Capacitor Value /10V
112	C5VH			220	nF	C5VH Capacitor Value /10V
113	C5VFL			100	nF	C5VLFL Capacitor Value /10V
114	C5VS			10	uF	C5VS Capacitor Value /10V
115	CBPS			10	uF	CBPS Capacitor Value /35V
116	RL			4800	kOhms	L-pin Input Voltae (Vin) Sense Resistor

117	RPP			158	kOhms	RPP Resistor /1% E96 series
118	RPS			75	kOhms	RPS Resistor /1% E96 series
119	**Bias, IS Circuit & Feedback Components**					
120	NS1			3		Primary Bias Turns
121	NSB			2		Secondary Bias Turns
122	NVIS			2		Secondary (Is) Sense Turns
123	RIS			1040	kOhms	Rris Resistor Value
124	CIS			470	pF	IS sense winding coupling capacitor
125	RFBH			129.8	kOhm	Calulated value of top feedback resistor. use series closest resistor 1% E96
126	RFBL			24.0	kOhm	Calulated value of low feedback resistor. use series closest resistor 1% E96
127	**Currents and Winding loss elements**					
128	Iprim RMS			1.24	A	Transformer Primary Winding RMS Current at PoutCont at VinNom
129	ISRMS			11.70	A	Transformer Secondary Winding RMS Current at PoutCont at VinNom
130	Irms_SR			7.23	A	Secondary Rectifier RMS Current at PoutCont at VinNom
131	Irms_CO1			7.23	A	Output Capacitor RMS Current at PoutCont at VinNom
132	RdcPrim			0.18	Ohms	Primary Winding DC Resistance
133	RacPrim			0.23	Ohms	Primary Winding AC Resistance
134	RdcSec			2.025	mOhms	Secondary Winding DC Resistance
135	RacSec			2.129	mOhms	Secondary Winding AC Resistance
136	**Errors, Warnings, Information**					
137	Information			0		Number of variables required bench functionality check. Check the variables with "Info" in the third column .
138	Design Warnings			0		Number of variables whose values exceed electrical/datasheet specifications. Check the variables with "Err" in the third column .
139	Design Errors			0		The list of design variables which result in an infeasible design.
140	**Advanced Settings**					
141	Kz			1.0		coefficient of surplus ZVS energy @ Vnom - raise Kz to lower Vin(GmaxInv) - Kz should be >= 1.0 to ensure ZVS operation

142	Tdd1_Vinnom			250	ns	Half-bridge slew at 100% load @ Vnom - raise Tdd1 to lower ZVS currents
143	Coupling			0.89		Transformer Coupling
144	Cpri			40.00	pF	Stray Capacitance at transformer primary

10 Bridge Heat Sink



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00307-00	Heat Spreader	1
2	15-00347-00	800 V, 8 A, BRIDGE RECTIFIER	1
3	75-00002-00	SCREW MACHINE PHIL 4-40 x .3125 SS	1
4	75-00152-00	Shoulder Washer #4	1
5	60-00016-00	TERMINAL, EYELET, ZIERICK 190	2
6	60-00099-00	Thermal Grease	1

Figure 15 – Bridge Heat Sink Assembly Drawing.

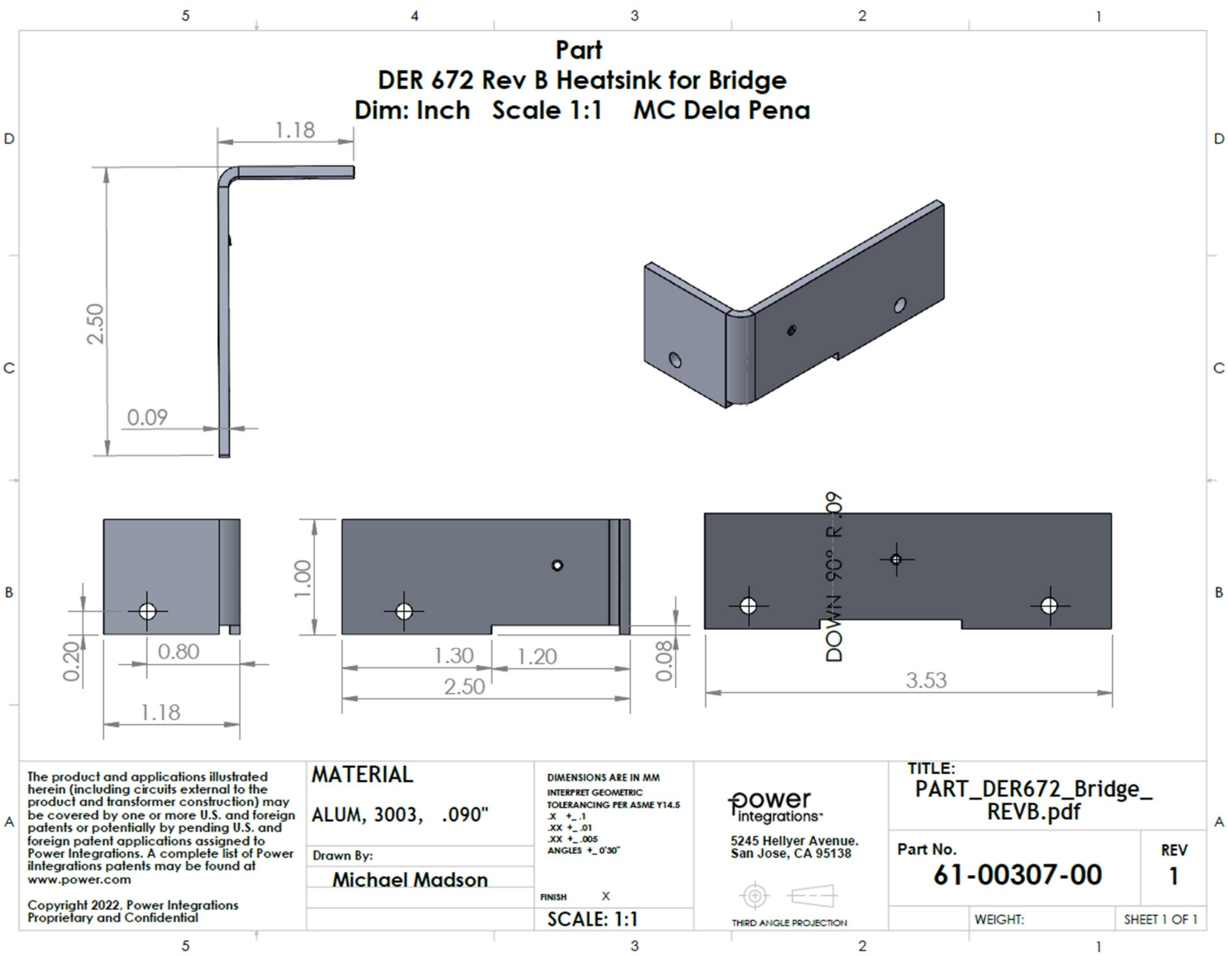


Figure 16 – Bridge Heat Sink Sheet Metal Drawing.

11 Performance Data

This section provides a summary of the unit under test's performance under certain line and load conditions. Furthermore, it gives an overview of the set up and conditions under which the unit was tested into.

11.1 *Total Efficiency*

The graph below shows the total power supply efficiency of the unit with respect to output power and different line voltages. A variable AC source was used to supply a Sine wave input and a DC electronic load set to CC mode was used as load on the output.

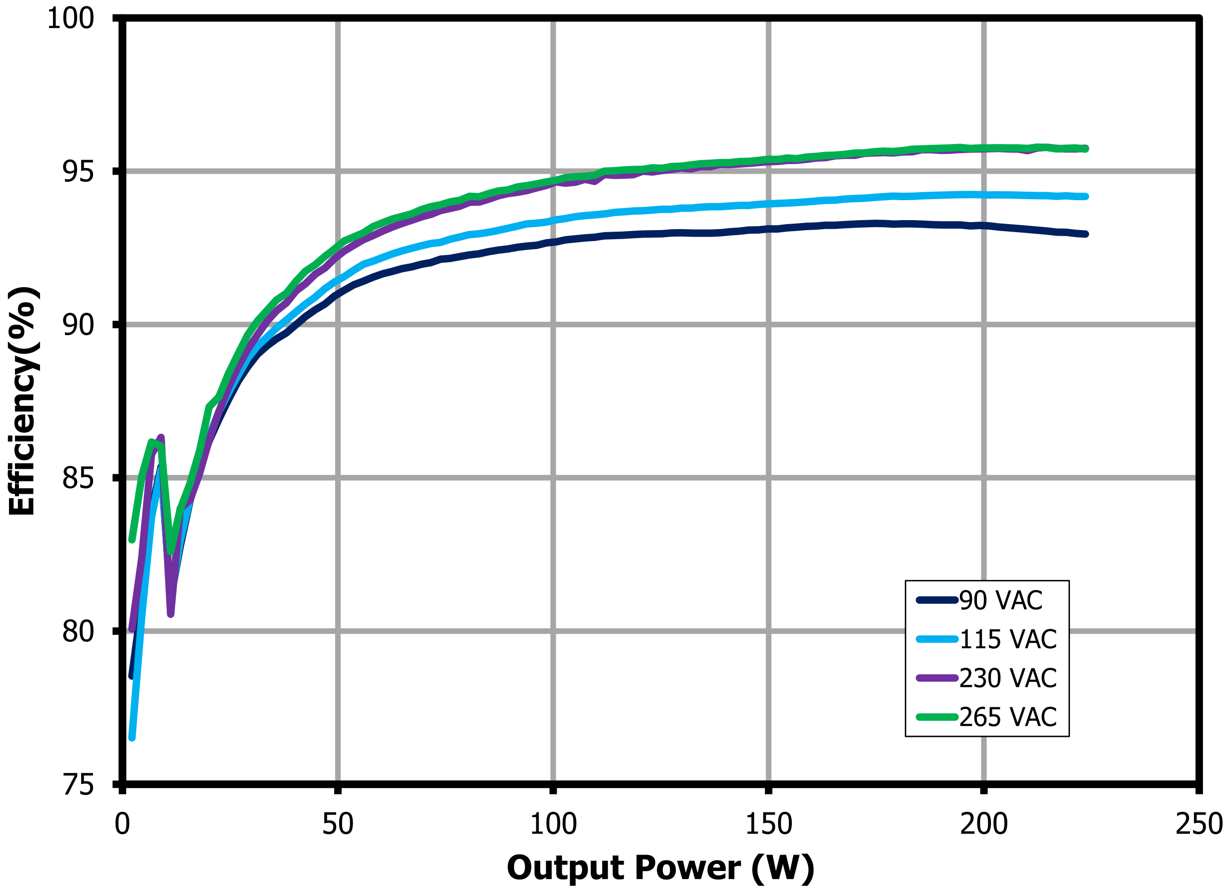


Figure 17 – Total Efficiency vs. Load, 24 V Output.

11.2 ***No-Load Input Power***

The total no-load input power of both LLC and PFC was measured at room temperature with an integration time of 15 minutes. The output was completely disconnected from the load and no other probes was connected aside from the input power meter.

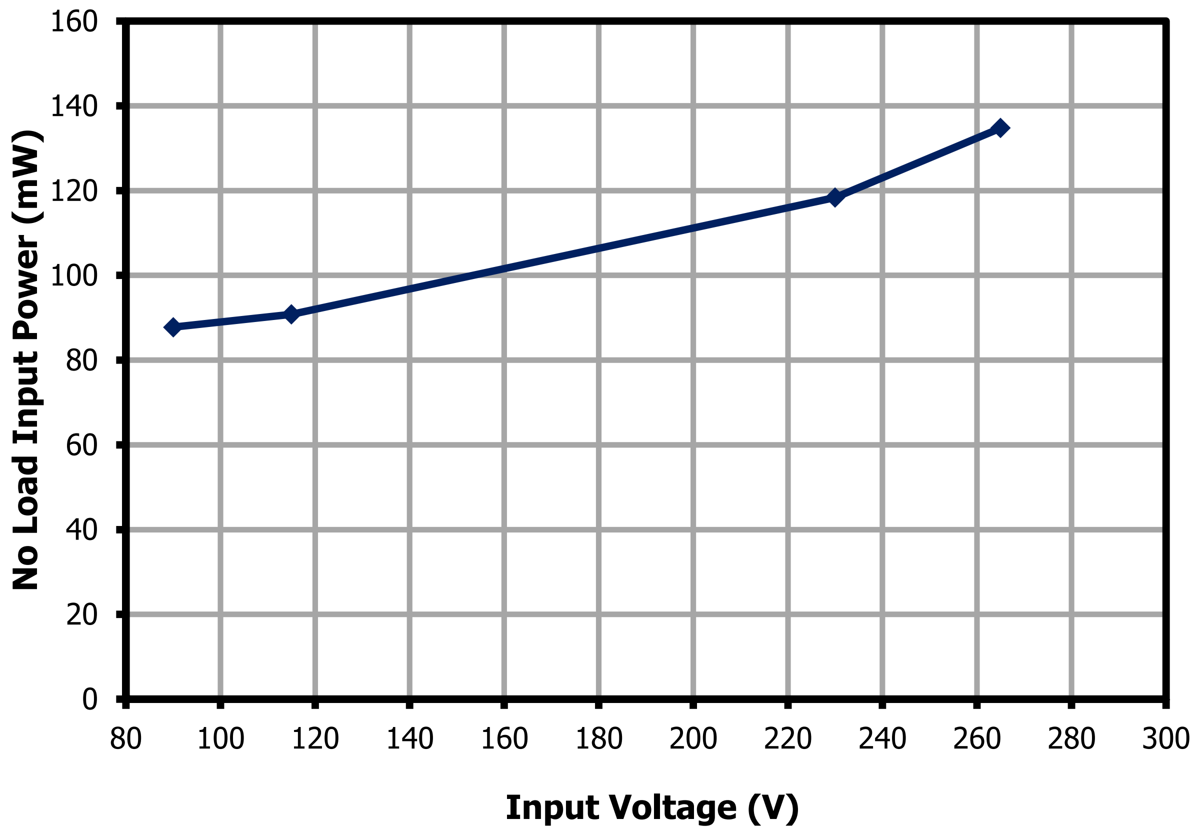


Figure 18 – No-Load Input Power vs. Input Voltage.

11.3 *Power Factor*

Power Factor was measured at different line voltages with varying loads using a power meter. A variable AC source was used to supply a Sine wave input and a DC electronic load set to CC mode was used as load on the output.

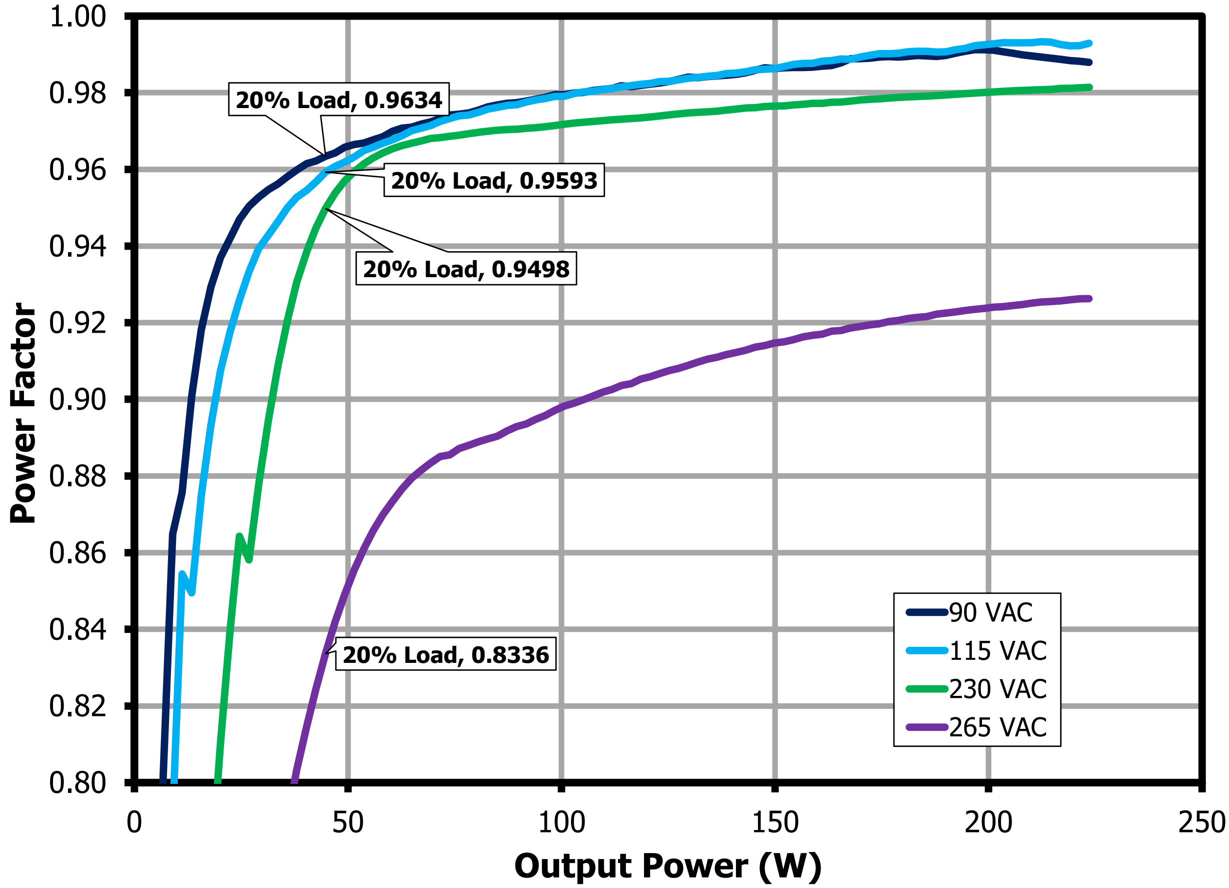


Figure 19 – Power Factor vs. Output Power.

Load (W)	Power Factor			
	90 V_{AC}	115 V_{AC}	230 V_{AC}	265 V_{AC}
22 W (10% Load)	0.942	0.9176	0.8398	0.7015
44 W (20% Load)	0.9634	0.9593	0.9498	0.8336
220 W (100% Load)	0.9879	0.9929	0.9814	0.9263

Table – Power Factor vs. Output Power 10%, 20% and 100% load.

11.4 *Total Harmonic Distortion*

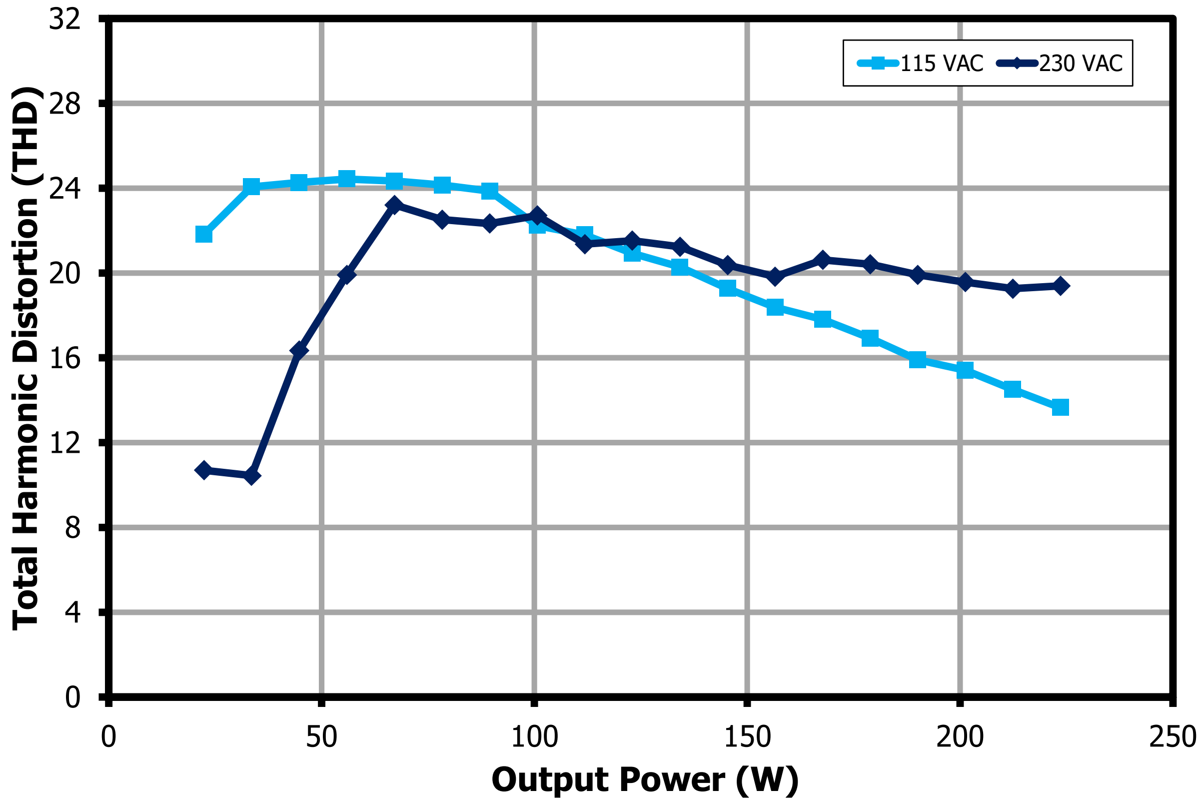


Figure 20 – Total Harmonic Distortion.

11.5 *Line Regulation*

Line regulation was measured with an AC source connected to the input supply which is varied at 10 V interval with an electronic load set in CCH mode to draw a constant current output from the power supply.

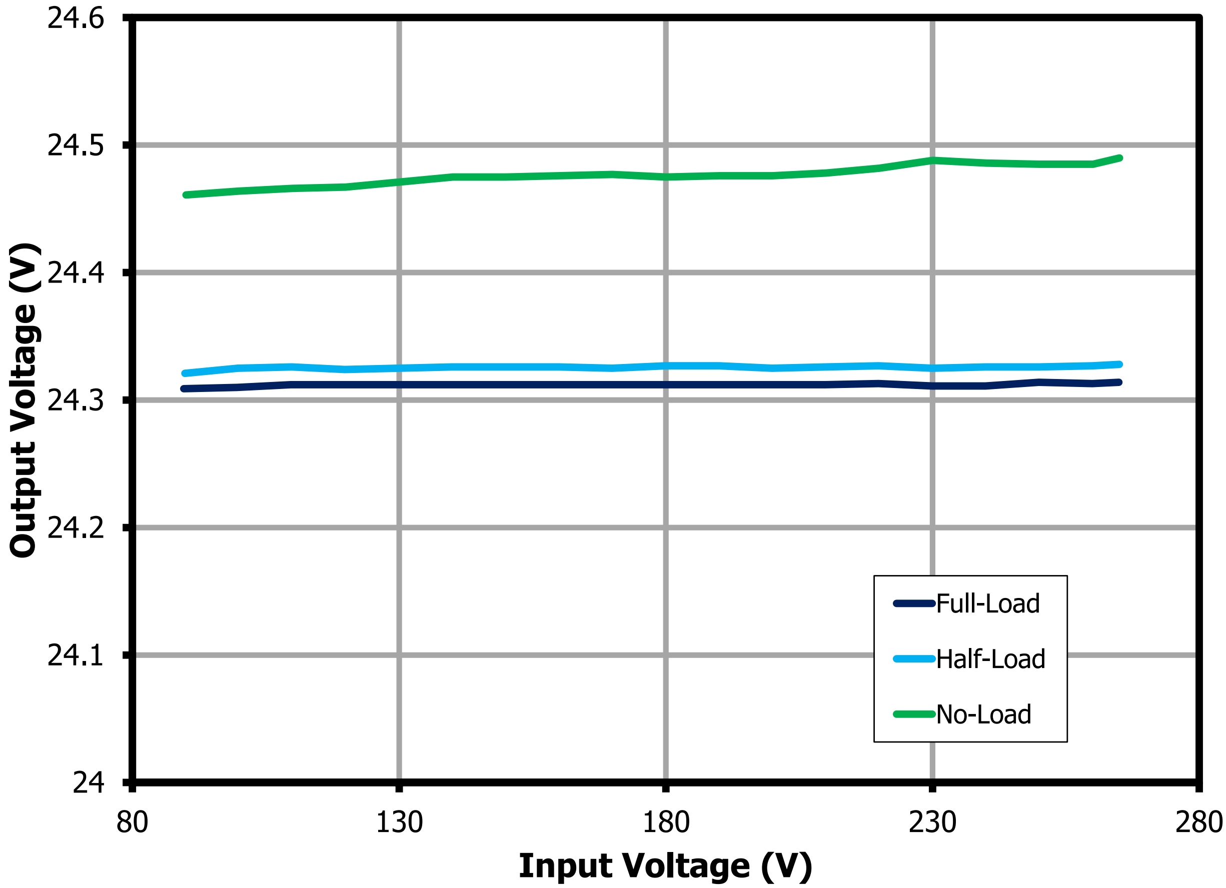


Figure 21 – Line Regulation.

11.6 *Load Regulation*

Load regulation was measured by decreasing the load from full load down to light loads using an DC electronic load as a load on the output. The test was repeated on different line voltages.

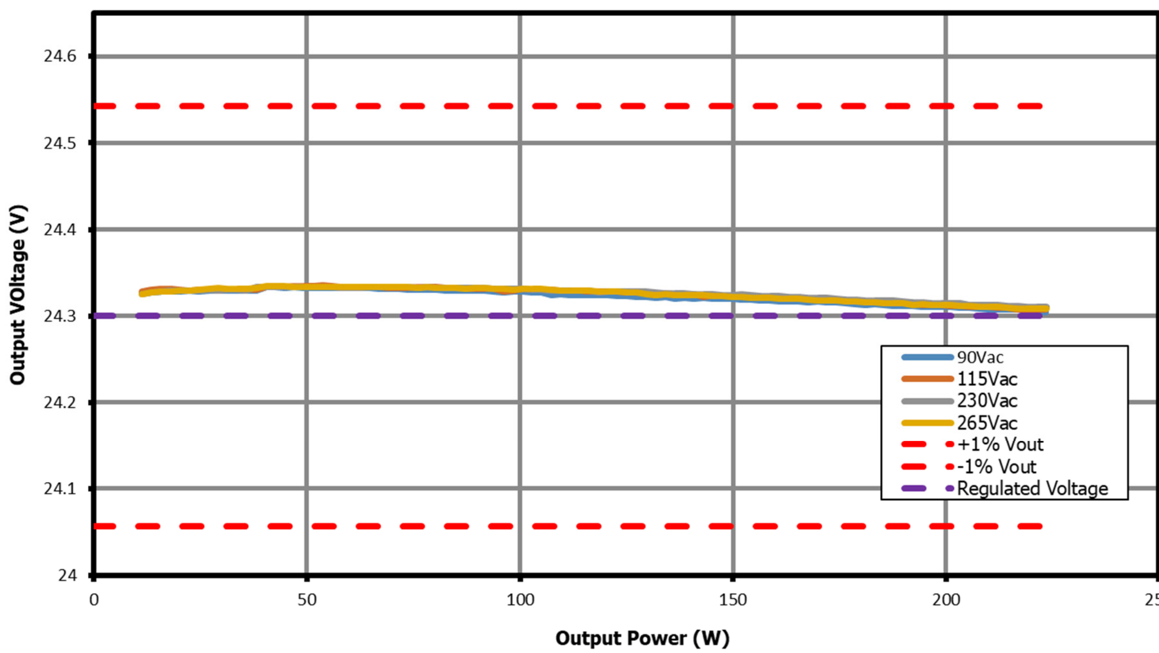


Figure 22 – Load Regulation.

12 Waveforms

12.1 *Input Current, 100% Load*

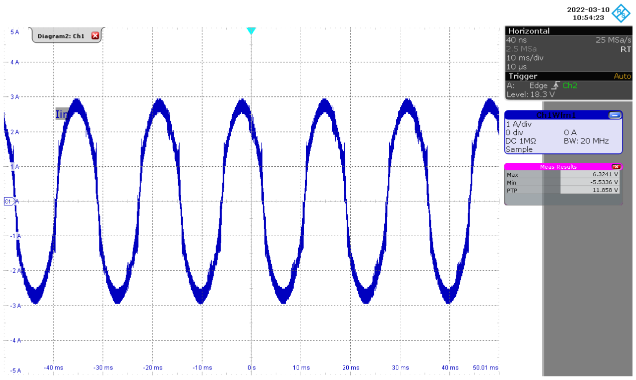


Figure 23 – Input Current, 115 VAC, 60 Hz, 4 A / div.

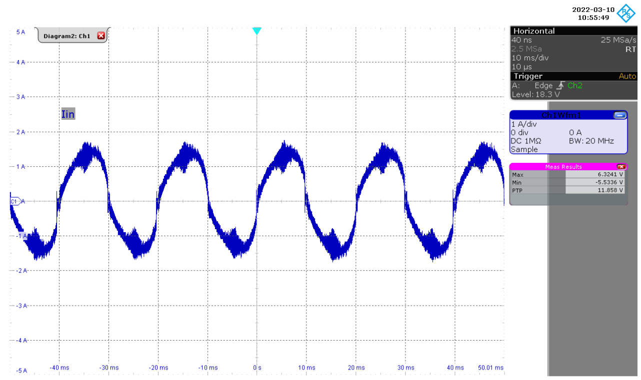


Figure 24 – Input Current, 230 VAC, 50 Hz, 4 A / div.

12.2 *LLC Primary Voltage and Current*

Shown in the figures below are the half-bridge voltage and current of the LLC section.

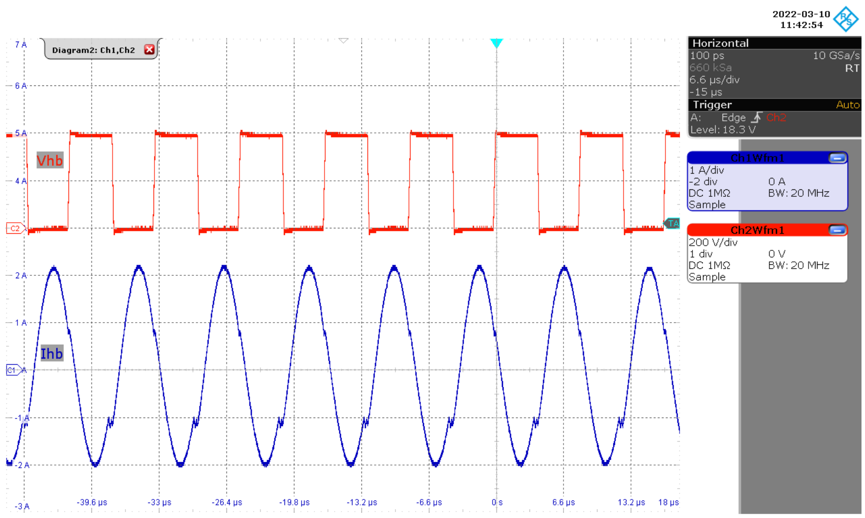


Figure 25 – LLC Stage Primary Voltage and Current, 100% Load.
Upper: HB Voltage, 200 V, 5 μs / div.
Lower: HB Current, 1 A / div.

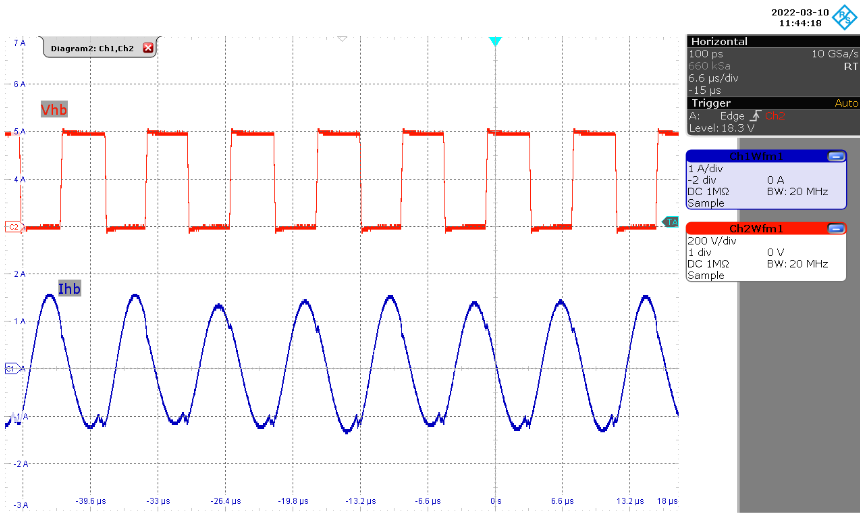


Figure 26 – LLC Stage Primary Voltage and Current, 50% Load.
Upper: HB Voltage, 200 V, 5 µs / div.
Lower: HB Current, 1 A / div.

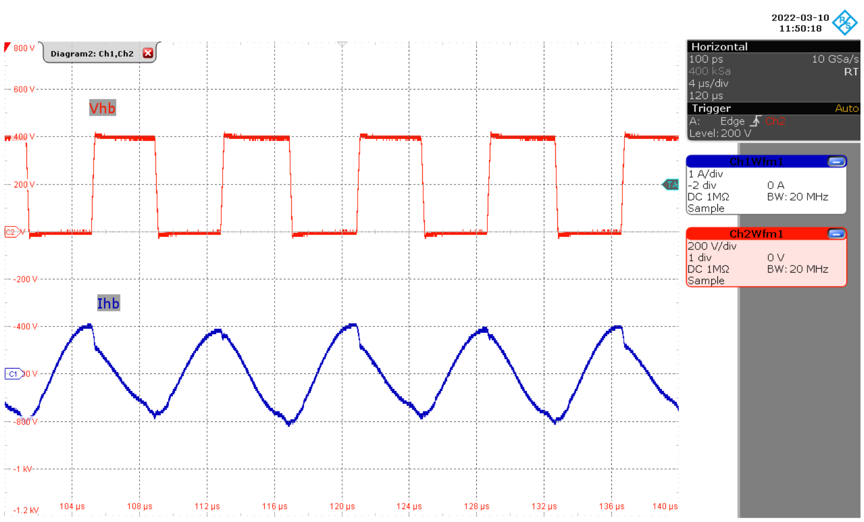


Figure 27 – LLC Stage Primary Voltage and Current, No-Load.
Upper: HB Voltage, 200 V, 5 µs / div.
Lower: HB Current, 1 A / div.

12.3 ***SR Waveforms***

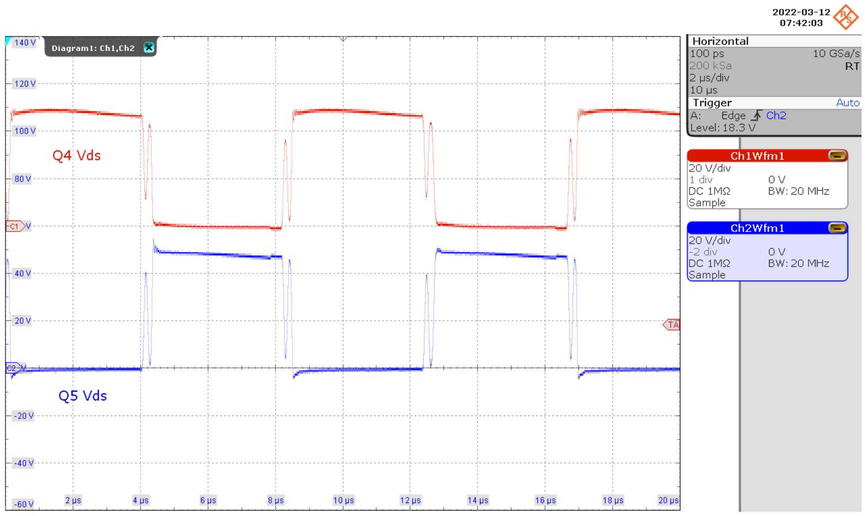


Figure 28 – Output Rectifier Peak Reverse Voltage. 230 VAC, Full Load.
Upper: Q_4 V_{DS}, 20 V / div.
Lower: Q_5 V_{DS}, 20 V / div.

12.4 ***PFC Voltage and Current, 100% Load***

The figures below shows CRM and DCM operation with valley switching of HiperPFS-5.

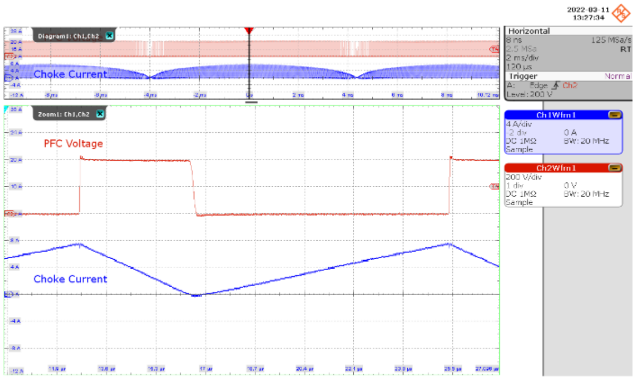


Figure 29 – V_{DS} and Choke Current, 90 VAC.
Upper: V_{DRAIN}, 200 V / div.
Lower: Choke Current, 4 A / div., 2 ms / div.

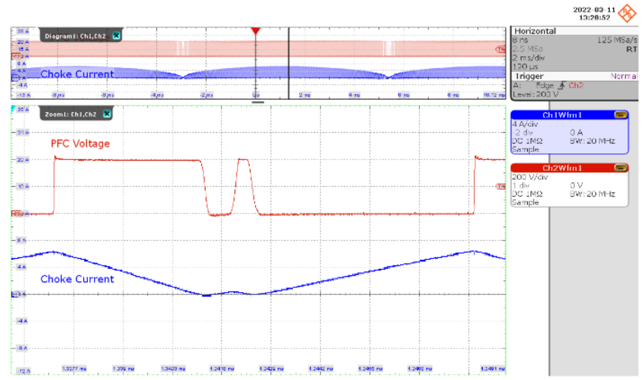


Figure 30 – V_{DS} and Choke Current, 115 VAC.
Upper: V_{DRAIN}, 200 V / div.
Lower: Choke Current, 4 A / div., 2 ms / div.

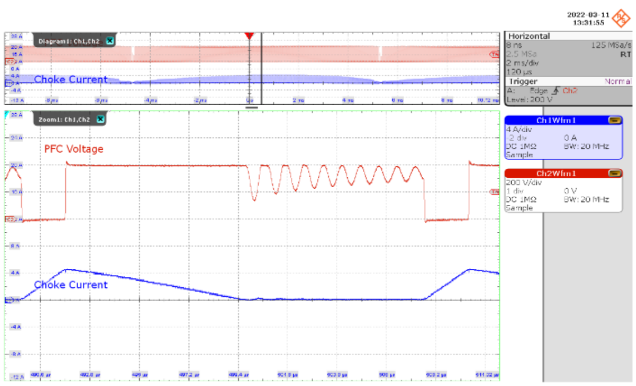


Figure 31 – V_{DS} and Choke Current, 230 VAC.
Upper: V_{DRAIN}, 200 V / div.
Lower: Choke Current, 4 A / div., 2 ms / div.

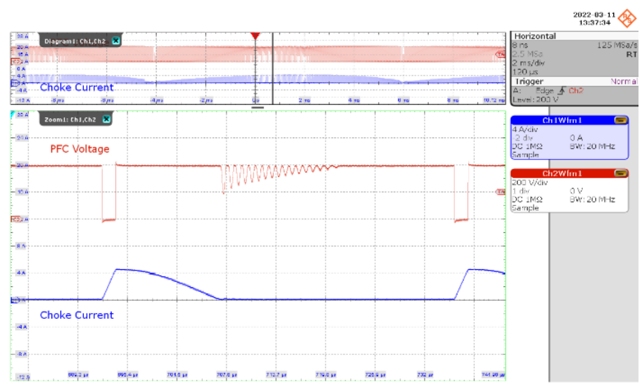


Figure 32 – V_{DS} and Choke Current, 265 VAC.
Upper: V_{DRAIN}, 200 V / div.
Lower: Choke Current, 4 A / div., 2 ms / div.

12.5 *Start Up Waveforms*

The figures below show the waveforms of V_{BULK}, V_{AC} and V_{OUT} during start-up at both full load and no-load.

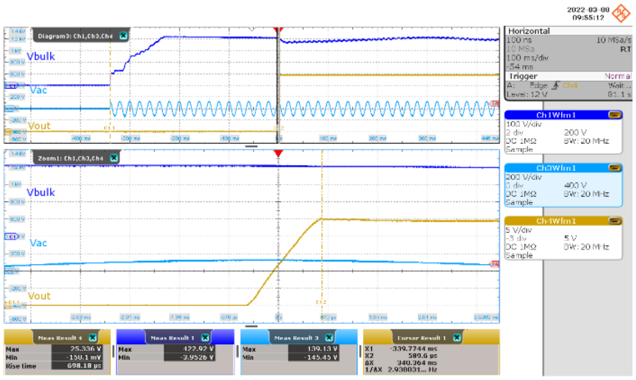


Figure 33 – Unit Start-up. 90 VAC, Full Load.
Dark Blue: V_{BULK}, 100 V / div.
Light Blue: V_{AC}, 200 V / div.
Yellow: V_{OUT}, 5 V / div.

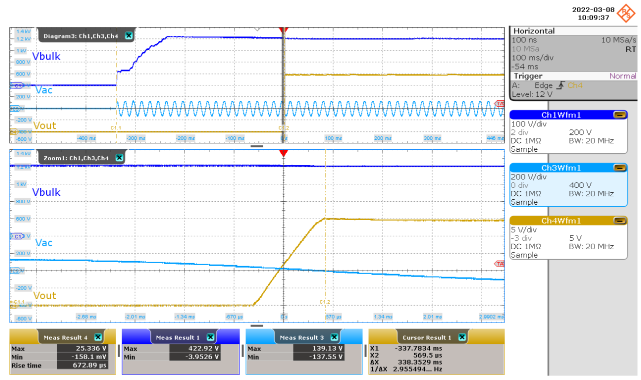


Figure 34 – Unit Start-up. 90 VAC, No-Load.
Dark Blue: V_{BULK}, 100 V / div.
Light Blue: V_{AC}, 200 V / div.
Yellow: V_{OUT}, 5 V / div.

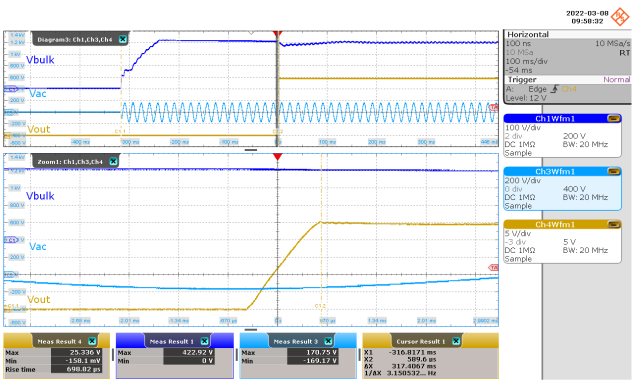


Figure 35 – Unit Start-up. 115 VAC, Full Load.
Dark Blue: V_{BULK}, 100 V / div.
Light Blue: V_{AC}, 200 V / div.
Yellow: V_{OUT}, 5 V / div.

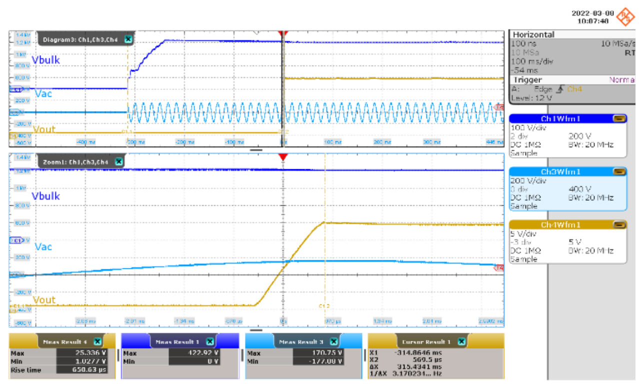


Figure 36 – Unit Start-up. 115 VAC, No-Load.
Dark Blue: V_{BULK}, 100 V / div.
Light Blue: V_{AC}, 200 V / div.
Yellow: V_{OUT}, 5 V / div.

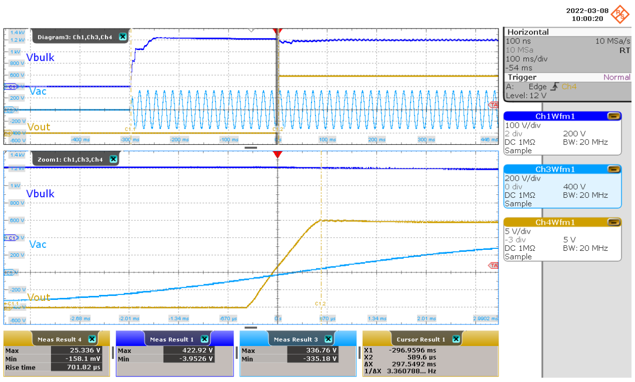


Figure 37 – Unit Start-up. 230 VAC, Full Load.
Dark Blue: V_{BULK}, 100 V / div.
Light Blue: V_{AC}, 200 V / div.
Yellow: V_{OUT}, 5 V / div.

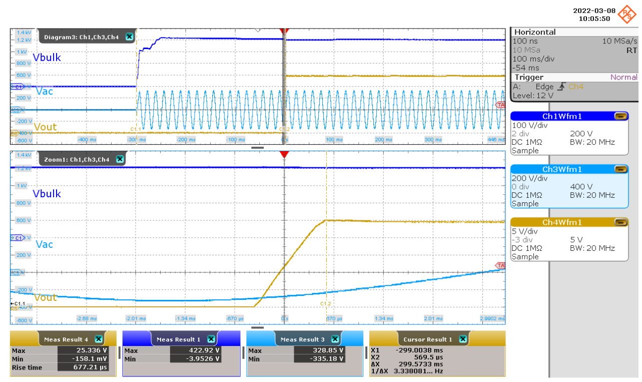


Figure 38 – Unit Start-up. 230 VAC, No-Load.
Dark Blue: V_{BULK}, 100 V / div.
Light Blue: V_{AC}, 200 V / div.
Yellow: V_{OUT}, 5 V / div.

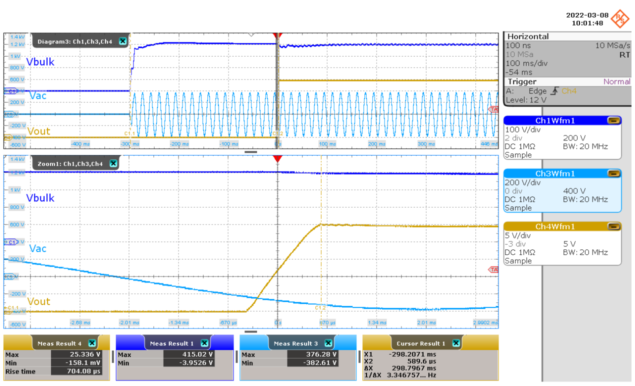


Figure 39 – Unit Start-up. 265 VAC, Full Load.
Dark Blue: V_{BULK}, 100 V / div.
Light Blue: V_{AC}, 200 V / div.
Yellow: V_{OUT}, 5 V / div.

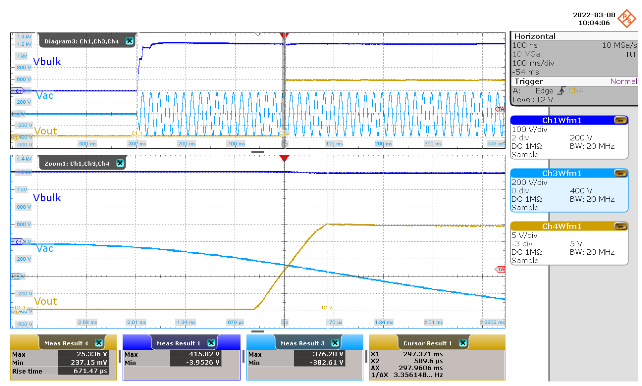


Figure 40 – Unit Start-up. 265 VAC, No-Load.
Dark Blue: V_{BULK}, 100 V / div.
Light Blue: V_{AC}, 200 V / div.
Yellow: V_{OUT}, 5 V / div.

12.6 *Burst Operation Waveforms*

Burst Mode is generally used for system efficiency, output regulation and to limit the burst frequency envelope below audio frequency. Shown below are the different burst mode of operations namely Intermediate (IM) mode, Light Load (LL) Mode and the Super Light Load (SLL) Mode.

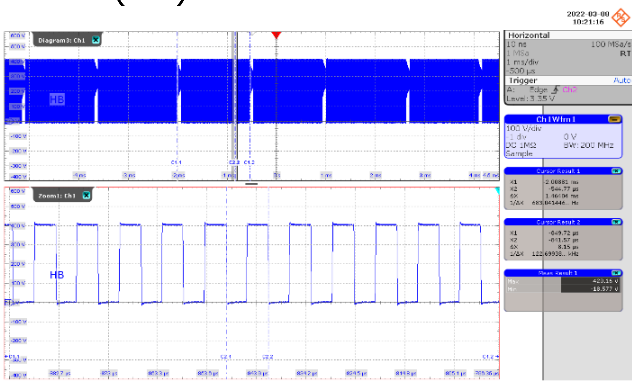


Figure 41 – Burst Operation. 230 VAC, IM Mode (1.6 A). V_{HB}, 100 V / div. Burst Time = 1.46 ms.

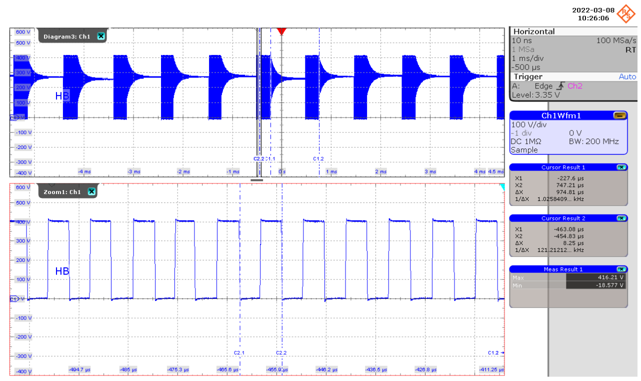


Figure 42 – Burst Operation. 230 VAC, LL Mode (0.4 A). V_{HB}, 100 V / div. Burst Time = 974.81 µs.

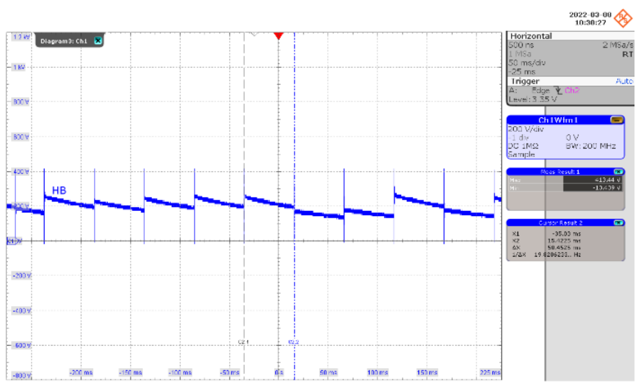


Figure 43 – Burst Operation. 230 VAC, SLL Mode (NL). V_{HB}, 100 V / div. Burst Time = 50.45 ms.

12.7 *Dynamic Loading*

Figures below show the response of the LLC converter during a dynamic loading with very minimal undershoot (note: during no-load it is operating at burst mode that is why you can see a slightly higher regulation than loaded conditions).

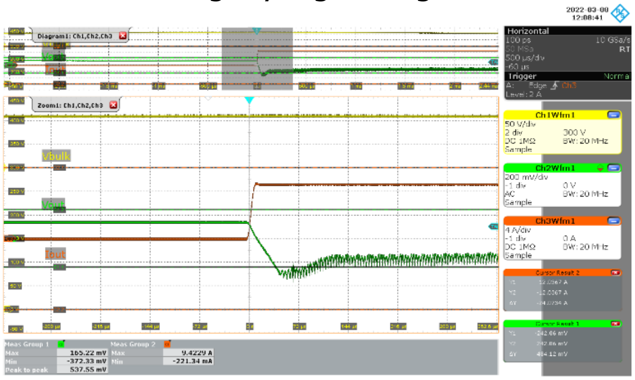


Figure 44 – Dynamic Loading. 115 VAC, 0-100% Load.
Yellow: V_{BULK}, 50 V / div.
Green: V_{OUT}, 200 mV / div.
Orange: I_{OUT}, 4 A / div.

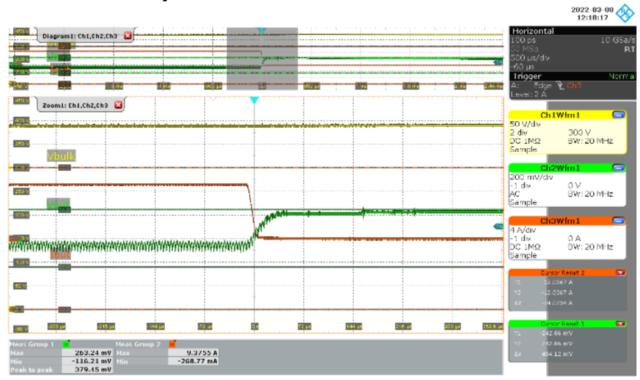


Figure 45 – Dynamic Loading. 115 VAC, 100-0% Load.
Yellow: V_{BULK}, 50 V / div.
Green: V_{OUT}, 200 mV / div.
Orange: I_{OUT}, 4 A / div.

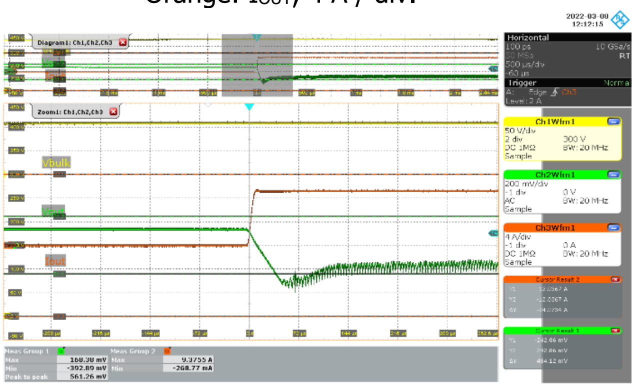


Figure 46 – Burst Operation. 230 VAC, 0-100% Load.
Yellow: V_{BULK}, 50 V / div.
Green: V_{OUT}, 200 mV / div.
Orange: I_{OUT}, 4 A / div.

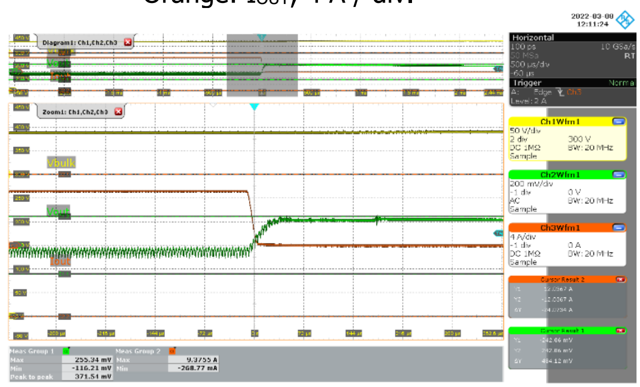


Figure 47 – Burst Operation. 230 VAC, 100-0% Load.
Yellow: V_{BULK}, 50 V / div.
Green: V_{OUT}, 200 mV / div.
Orange: I_{OUT}, 4 A / div.

13 Output Ripple Measurements

13.1 *Ripple Measurement Technique*

For DC output ripple measurements a modified oscilloscope test probe is used to reduce spurious signals. Details of the probe modification are provided in the figures below.

Tie two capacitors in parallel across the probe tip of the 4987BA probe adapter. A 0.1 μF / 100 V ceramic capacitor and 47 μF / 100 V aluminum electrolytic capacitor were used. The aluminum electrolytic capacitor is polarized, so always maintain proper polarity across DC outputs.

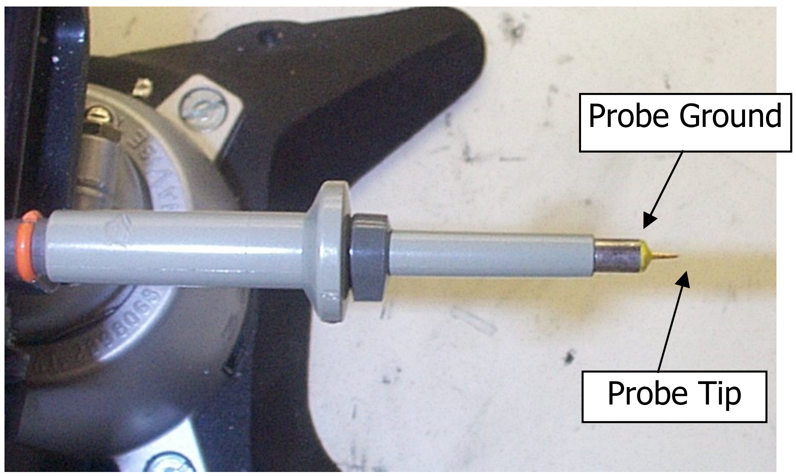


Figure 48 – Oscilloscope Probe Prepared for Ripple Measurement (End Cap and Ground Lead Removed).

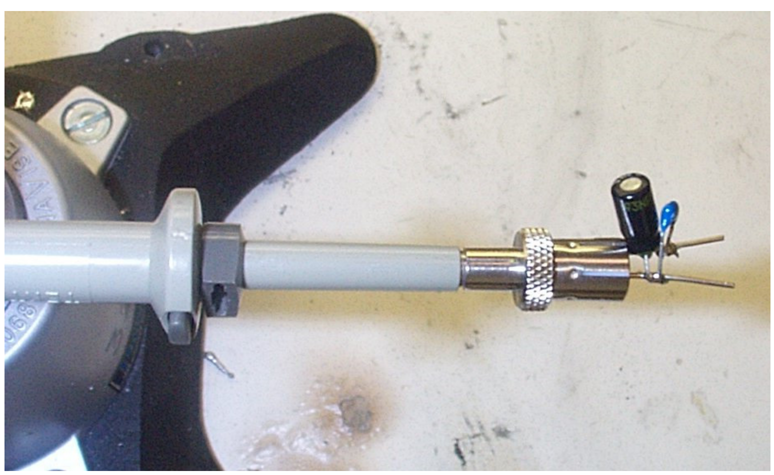


Figure 49 – Oscilloscope Probe with Probe Master 4987BA BNC Adapter (Modified with Wires for Probe Ground for Ripple measurement and Two Parallel Decoupling Capacitors Added).

13.2 *Ripple Measurements*

The following pictures show the output voltage ripple measurement with electronic load configured to constant current (CCH) mode. Measurements were taken at 115 VAC and 230 VAC line voltages at full load, intermediate burst and light load burst.

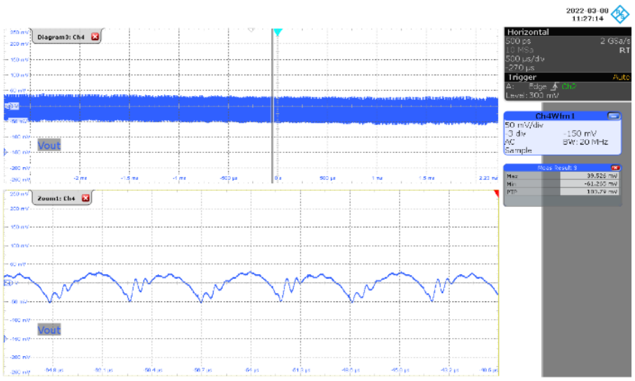


Figure 50– Output Ripple, Full Load (9.2 A), 115 VAC.
Blue: V_{OUT}, 50 mV / div.
Ripple: 0.42% Ripple.

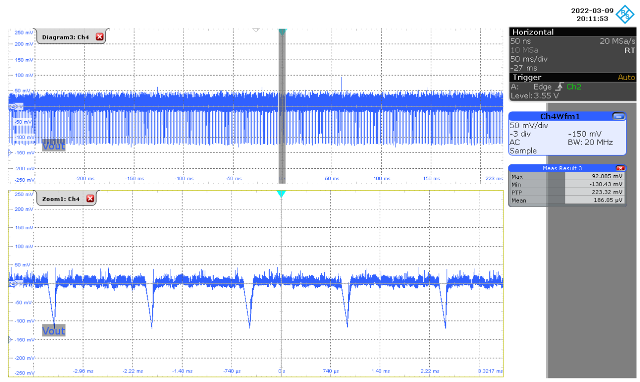


Figure 51– Output Ripple, IM Burst (1.3 A), 115 VAC.
Blue: V_{OUT}, 50 mV / div.
Ripple: 0.93% Ripple.

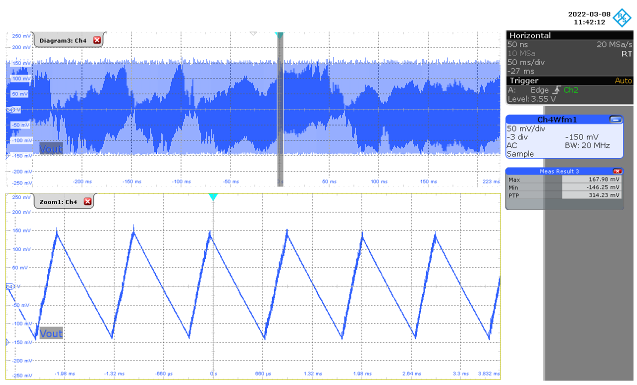


Figure 52– Output Ripple, LL Burst (0.4 A), 115 VAC.
Blue: V_{OUT}, 50 mV / div.
Ripple: 1.31% Ripple.

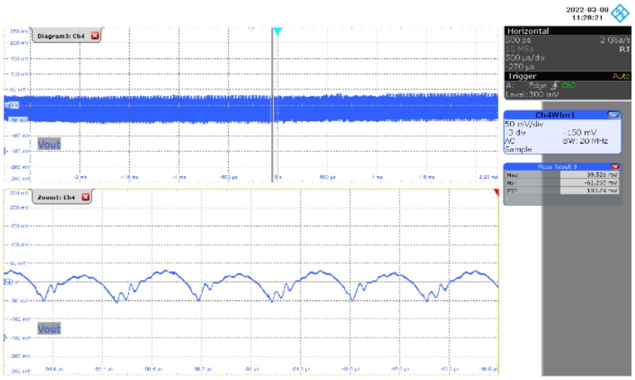


Figure 53– Output Ripple, Full Load (9.2 A), 230 VAC.
Blue: V_{OUT}, 50 mV / div.
Ripple: 0.42% Ripple.

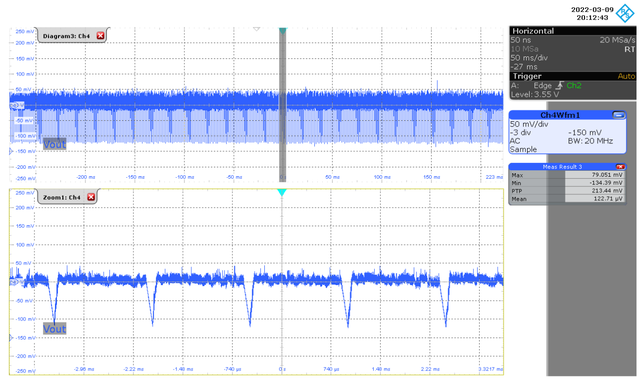


Figure 54– Output Ripple, IM Burst (1.3 A), 115 VAC.
Blue: V_{OUT}, 50 mV / div.
Ripple: 0.89% Ripple.

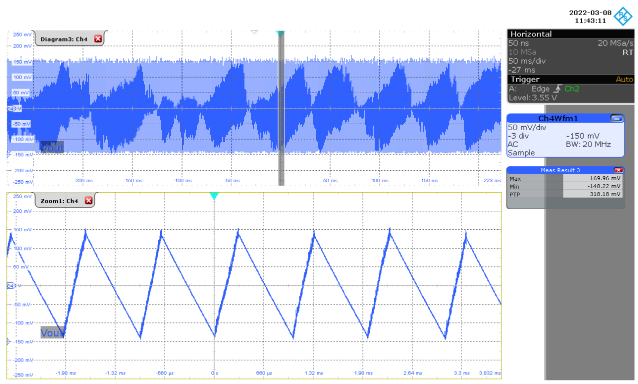


Figure 55– Output Ripple, LL Burst (0.4 A), 115 VAC.
Blue: V_{OUT}, 50 mV / div.
Ripple: 1.33% Ripple.

14 Temperature Profiles

The board was placed in an enclosed acrylic box, with electronic load set at constant current mode with full load current of 9.2 A. For each test conditions, the UUT was soaked for 1 hour before measurement was made.

14.1 *90 VAC, 60 Hz, 220 W Output*

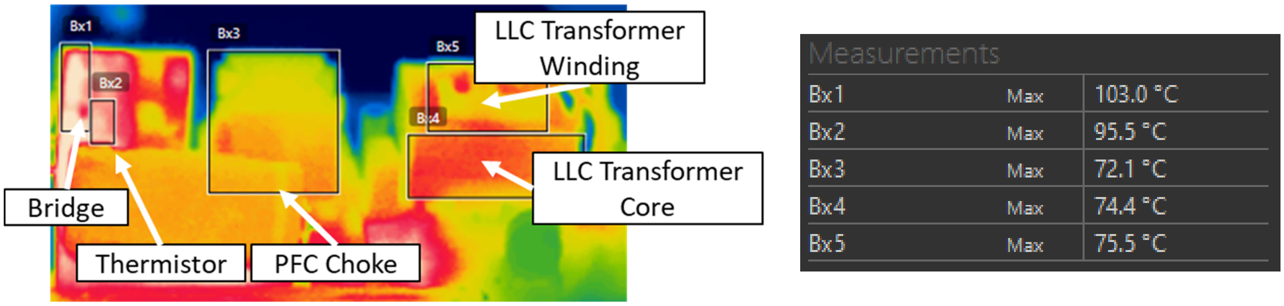


Figure 56 – Top Side Thermal Picture, 100% Load, 90 VAC.

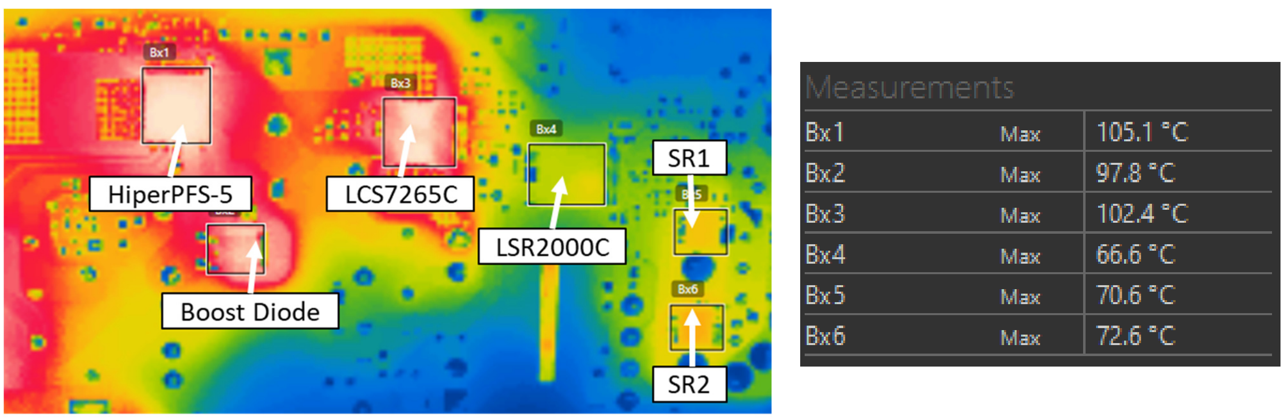
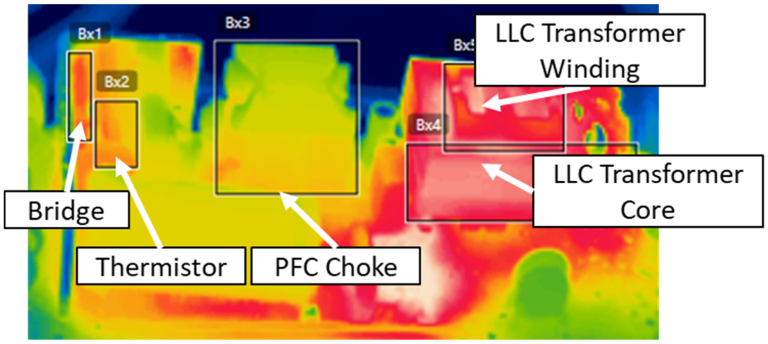


Figure 57 – Bottom Side Thermal Picture, 100% Load, 90 VAC.

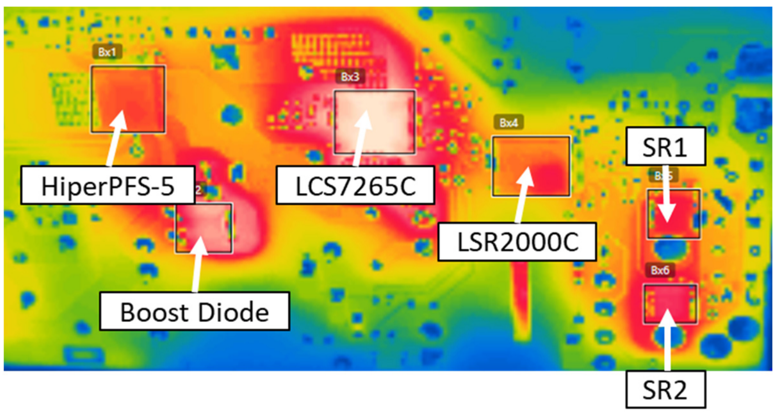
Component	Temperature (ºC)
Ambient Temperature	34.1
PFC Choke	72.1
LLC Transformer	75.5
Bridge	103.0
Boost Diode	97.8
HiperLCS-2 Primary	102.4
HiperLCS-2 Secondary	66.6
PFS	105.1
SR1	70.6
SR2	72.6

14.2 ***265 VAC, 50 Hz, 220 W Output, Room Temperature***



Measurements		
Bx1	Max	59.4 °C
Bx2	Max	57.6 °C
Bx3	Max	56.4 °C
Bx4	Max	72.2 °C
Bx5	Max	74.5 °C

Figure 58– Top Side Thermal Picture, 100% Load, 265 VAC.



Measurements		
Bx1	Max	62.6 °C
Bx2	Max	77.2 °C
Bx3	Max	87.0 °C
Bx4	Max	65.1 °C
Bx5	Max	64.8 °C
Bx6	Max	68.8 °C

Figure 59– Bottom Side Thermal Picture, 100% Load, 265 VAC.

Component	Temperature (ºC)
Ambient Temperature	30.2
PFC Choke	56.4
LLC Transformer	73.9
Bridge	59.3
Boost Diode	77.2
HiperLCS-2 Primary	87.0
HiperLCS-2 Secondary	65.1
PFS	62.6
SR1	64.8
SR2	68.8

15 Revision History

Date	Author	Revision	Description and Changes	Reviewed
16-Mar-22	MCDP	1.0	Initial Release	Apps & Mktg

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