Design Example Report

Title	***65 W USB PD 3.0 Power Supply with 3.3 V – 21 V PPS Output Using InnoSwitch™3-Pro PowiGaN™ INN3370C-H302, MinE-CAP MIN1072M and VIA Labs VP302 Controller***
Specification	90 VAC – 265 VAC Input; 5 V / 3 A; 9 V / 3 A; 15 V / 3 A; 20 V / 3.25 A; or 3.3 V – 21 V PPS Outputs
Application	Mobile Phone / Laptop Charger
Author	Applications Engineering Department
Document Number	DER-626
Date	October 5, 2020
Revision	1.2

Summary and Features

- InnoSwitch3-Pro - digitally controllable CV/CC QR flyback switcher IC with integrated high-voltage power MOSFET, synchronous rectification and FluxLink™ feedback
  - I^2C Interface enables low pin count USB PD controller (8 pin)
  - Sophisticated telemetry and comprehensive protection features
- Compact design with high power density using GaN switch and MinE-CAP: >15.0 W / inch^3 with enclosure
- USB PD 3.0 with PPS using highly optimized, low pin count USB PD Controller VP302
- All the benefits of secondary-side control with the simplicity of primary-side regulation
  - Insensitive to transformer variation
- Meets DOE6 and CoC v5 2016 efficiency requirement (>1% efficiency margin)
- Micro stepping of voltages (20 mV) and CC thresholds (50 mA) in compliance with PPS protocol
- Output overvoltage and overcurrent protection
- Integrated thermal protection
- <50 mW no-load input power

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Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This document is an engineering report describing a 65 W USB PD power supply with 5 V / 3 A, 9 V / 3 A, 15 V / 3 A, 20 V / 3.25 A, or 3.3 V – 21 V Programmable Power Supply (PPS) output using the InnoSwitch3-Pro PowiGaN INN3370C-H302 IC, MinE-CAP MIN1072M and a VIA Labs VP302 USB PD controller. The USB PD source capabilities of the power supply are listed below.

- 5 V / 3 A (Fixed Supply PDO)
- 9 V / 3 A (Fixed Supply PDO)
- 15 V / 3 A (Fixed Supply PDO)
- 20 V / 3.25 A (Fixed Supply PDO)
- 3.3 V – 21 V / 3 A (Programmable Power Supply APDO)

This design demonstrates the high power density and efficiency that can be attained due to the high level of integration of the InnoSwitch3-Pro controller and total volume reduction due to the MinE-CAP family of ICs. The MinE-Cap is used to minimize the physical size of the input bulk capacitors and, together with the use of low-profile planar magnetics, a form factor of 82 mm (L) x 51 mm (W) x 12 mm (H) without an enclosure corresponding to a power density of 21.22 W/in^3 is realized.

The report contains the power supply specification, schematic diagram, printed circuit board layout, bill of materials, magnetics and adapter case specifications, and performance data.

Figure 1 – Populated Circuit Board Photograph, Entire Assembly.

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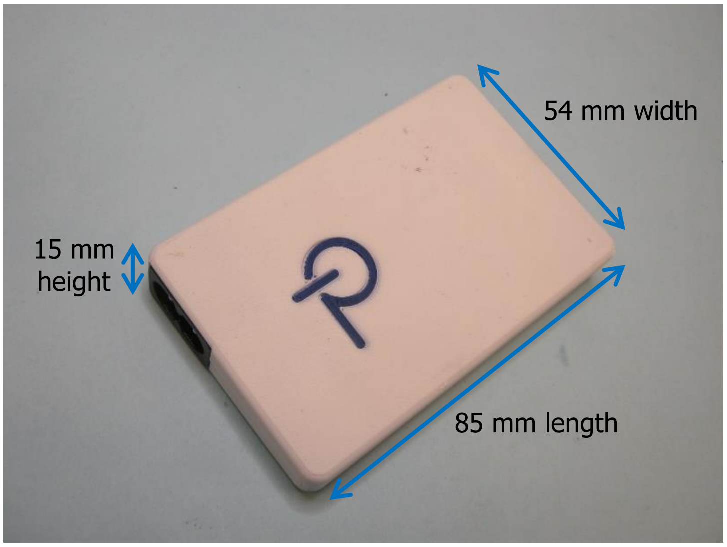

Figure 2 – Unit Enclosure with Dimensions.

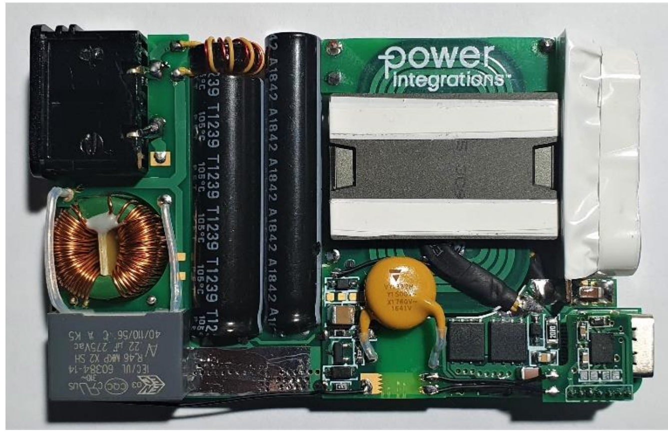

Figure 3 – Populated Circuit Board Photograph - Top.

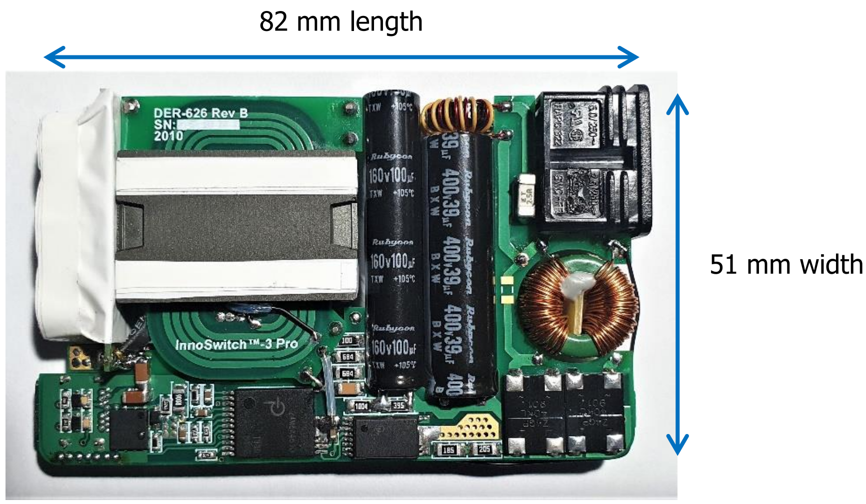

Figure 4 – Populated Circuit Board Photograph - Bottom.

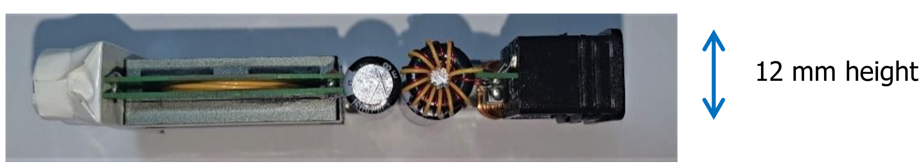

Figure 5 – Populated Circuit Board Photograph - Side.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power				60	mW	Measured at 230 VAC.
5 V Setting						
Output Voltage	$V_{OUT\ (5\ V)}$		5.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(5\ V)}$			200	mV	Measured at End of 100 mΩ Cable. (20 MHz Bandwidth).
Output Current	$I_{OUT(5\ V)}$			3.0	A	±3%
Average Efficiency	$\eta_{(5\ V)}$		>90		%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(5\ V)}$			15	W	
9 V Setting						
Output Voltage	$V_{OUT(9\ V)}$		9.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(9\ V)}$			200	mV	Measured at End of 100 mΩ Cable. (20 MHz Bandwidth).
Output Current	$I_{OUT(9\ V)}$			3.0	A	±3%
Average Efficiency	$\eta_{(9\ V)}$		>90		%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(9\ V)}$			27	W	
15 V Setting						
Output Voltage	$V_{OUT(15\ V)}$		15.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(15\ V)}$			200	mV	Measured at End of 100 mΩ Cable. (20 MHz Bandwidth).
Output Current	$I_{OUT(15\ V)}$			3.0	A	±3%
Average Efficiency	$\eta_{(15\ V)}$		>90		%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(15\ V)}$			45	W	
20 V Setting						
Output Voltage	$V_{OUT(20\ V)}$		20.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(20\ V)}$			200	mV	Measured at End of 100 mΩ Cable. (20 MHz Bandwidth).
Output Current	$I_{OUT(20\ V)}$			3.0	A	±3%
Average Efficiency	$\eta_{(20\ V)}$		>90		%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(20\ V)}$			65	W	
3.3 – 21 V PPS Setting						
Maximum Programmable Output Voltage	$V_{OUT(MAX)}$			21	V	APDO Maximum Voltage.
Minimum Programmable Output Voltage	$V_{OUT(MIN)}$	3.3			V	APDO Minimum Voltage.
Output Voltage Ripple	$V_{RIPPLE(PPS)}$			200	mV	Measured at End of 100 mΩ Cable. (20 MHz Bandwidth).
Output Current	$I_{OUT(PPS)}$			3.25	A	±3%
PPS Voltage Step	$V_{STEP(PPS)}$		20		mV	PPS Voltage Step (USB PD 3.0).
PPS Current Step	$I_{STEP(PPS)}$		50		mA	PPS Current Step (USB PD 3.0).
Continuous Output Power	$P_{OUT(20\ V)}$			65	W	
Conducted EMI		Meets CISPR22B / EN55022B				
Ambient Temperature	T_{AMB}	0		40	ºC	Free Convection, Sea Level.

Note: To use this design for a charger/adapter, circuit board would need to be modified depending on shape and form factor of the housing. ESD and Line surge performance should be evaluated and layout adjusted to meet the target specification.

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3 Schematic

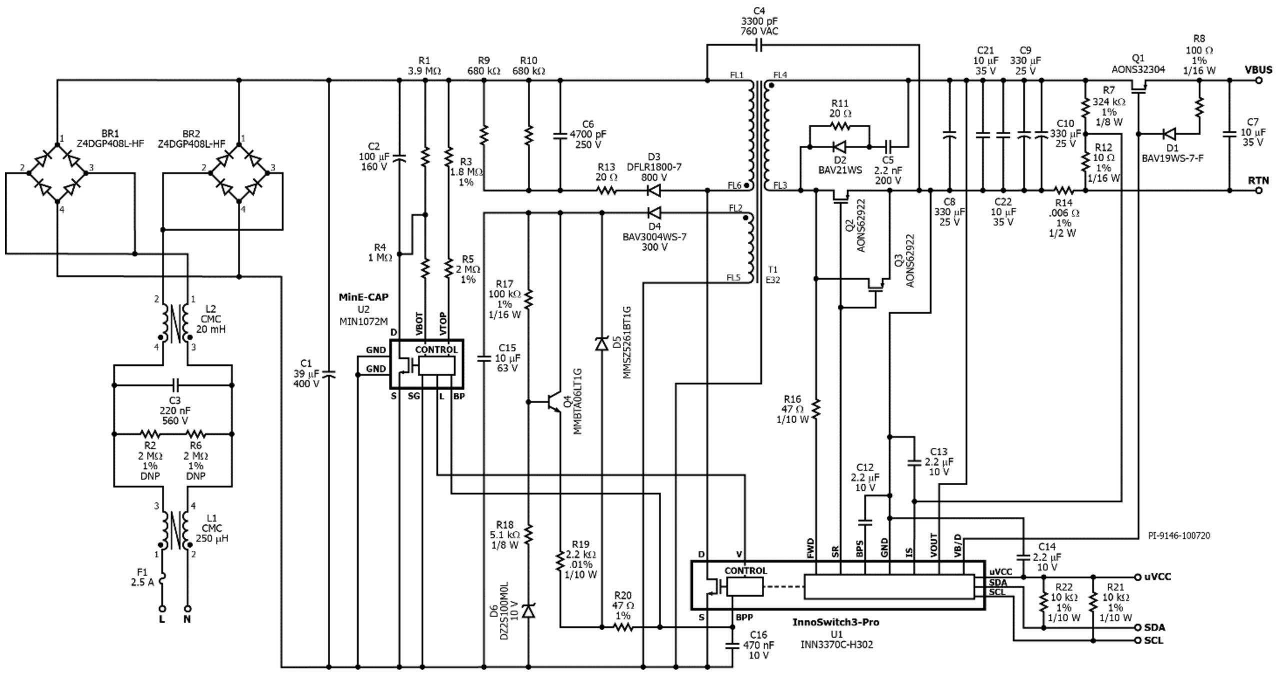

Figure 6 – Schematic, Power Section.

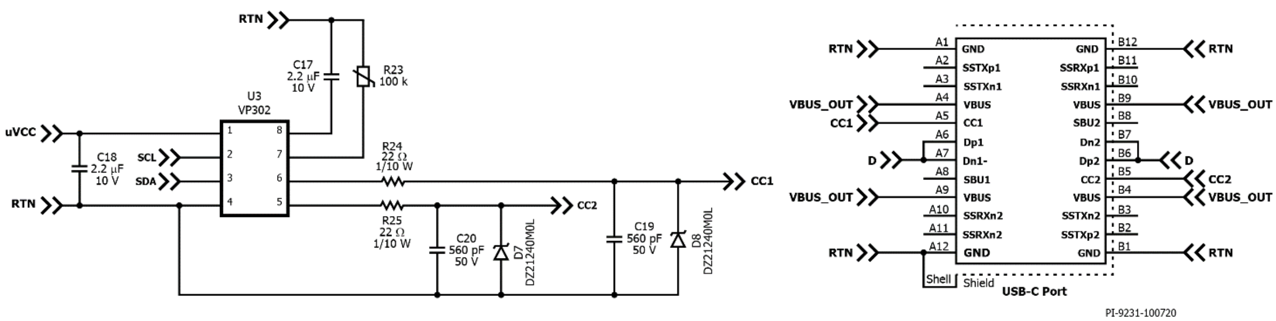

Figure 7 – Schematic, USB PD Controller Section.

4 Circuit Description

4.1 *Input Rectifier, MinE-CAP and EMI Filter*

Fuse F1 isolates the circuit and protects the AC line from excessive current due to component failure. Common mode chokes L1 and L2 along with capacitors C3 and C4 provide common mode and differential mode noise filtering to minimize conducted EMI emissions. Resistors R2 and R6 discharge the X capacitor C3 when the AC input is removed. The bridge rectifier formed by BR1 and BR2 rectifies the AC line voltage and provides a full-wave rectified DC voltage across the high-voltage bulk capacitor, C1. Two bridge rectifiers are used to improve heat dissipation by doubling the rectifier surface area since power loss from two rectifiers is the same as that of a single device.

4.2 *InnoSwitch3-Pro IC Primary*

One end of the transformer primary is connected to the rectified DC bus and the other end is connected to the drain terminal of the switch inside the InnoSwitch3-Pro IC U1. Resistors R4 and R5 provide input voltage sensing for protection in case of AC input undervoltage or overvoltage.

The V pin of the InnoSwitch3-Pro IC is connected directly to the L pin of the MinE-CAP. Resistors R3 and R4 provide input voltage sensing for both the MinE-CAP and InnoSwitch ICs. The MinE-CAP uses R3 and R5 primarily to monitor the line voltage and the voltage across the low-voltage bulk capacitor, C2. The InnoSwitch3-Pro uses the current from the L pin to determine line undervoltage and overvoltage conditions. During regular operation, the current from the L pin follows the current flowing through R3 and R5, so the InnoSwitch3-Pro IC operates as if said resistors are connected directly to the V pin. Resistor R1 is a bleed resistor used to regulate the voltage across C2, while resistor R4 is used by the MinE-CAP to sample the voltage at the negative terminal of C2.

For this specific design, bypass capacitor C16 is shared by both the BPP pin of the InnoSwitch3-Pro IC and the BP pin of the MinE-CAP. The value of C8 is chosen based on the desired current limit of the InnoSwitch3-Pro IC. One end of the transformer primary is connected to the rectified DC bus while the other end is connected to the InnoSwitch3-Pro DRAIN pin.

A low-cost RCD snubber formed by diode D3, resistors R9, R10 and R13, and capacitor C6 limits the voltage across the InnoSwitch3-Pro Drain-Source nodes during turn-off by dissipating the energy stored in the leakage inductance of the transformer.

The InnoSwitch3-Pro IC has an internal current source that charges capacitor C16 when AC input is first applied. Once the InnoSwitch3-Pro IC starts switching and during normal operation, bias current is drawn from the auxiliary winding of the transformer. The output of the auxiliary winding is rectified using diode D4 and filtered by capacitor C15. Resistor R15 and capacitor C11 form an RC snubber to suppress voltage spikes and

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ringing across D2, if necessary. Since the output voltage of the charger varies from 5 V to 20 V, the output of the auxiliary winding also varies and depending on the secondary to auxiliary turns ratio as well as the coupling coefficient between the primary and auxiliary. A linear regulator comprising resistors R17 and R18, Zener diode D6, and transistor Q4 provides a relatively stable DC voltage based on the breakdown voltage of D6 at the emitter terminal of Q1. Bias current can then be controlled using resistor R19.

Zener diode D5 offers primary sensed overvoltage protection. In case of overvoltage at the output of the converter, the auxiliary winding voltage also increases until D5 breaks down, causing excess current to flow into the BPP pin of the InnoSwitch3-Pro IC. If the current flowing into the BPP pin exceeds the I_{SD} threshold, the InnoSwitch3-Pro controller latches off to prevent any further increase in output voltage. Resistor R20 limits the current injected to the BPP pin during an overvoltage event.

4.3 *InnoSwitch3-Pro IC Secondary and USB Power Delivery Controller*

The secondary-side of the InnoSwitch3-Pro IC provides output voltage and current sensing and a gate drive to a FET for synchronous rectification. The voltage across the transformer secondary winding is rectified by the secondary-side FETs (or SR FET) Q2 and Q3 and filtered by parallel capacitors C8, C9, and C10. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via an RCD snubber, R11, C5, and D2.

The gates of Q2 and Q3 are turned on by secondary-side controller inside of IC U1, based on the secondary winding voltage sensed via resistor R16 and fed into the FWD pin of the IC.

In continuous conduction mode of operation, the SR FET is turned off just prior to the secondary-side commanding a new switching cycle from the primary. In discontinuous mode of operation, the SR FET is turned off when the magnitude of the voltage drop across the SR FET falls below a threshold of approximately $V_{SR(TH)}$. Secondary-side control of the primary-side power switch avoids any possibility of cross conduction of the two switches and provides extremely reliable synchronous rectifier operation.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C12 connected to the BPS pin of InnoSwitch3-Pro IC U1 provides decoupling for the internal circuitry.

The output current is sensed by monitoring the voltage drop across resistor R14. Resistors R7 and R12 add an offset to the sensed output current to provide a positive slope to the CC characteristic. The resulting current measurement is filtered with decoupling capacitor C13 and monitored across the IS and SECONDARY GROUND pins. An internal current sense threshold which is configured via the I^2C interface up to approximately 32 mV is used to reduce losses. Once the threshold is exceeded, the

InnoSwitch3-Pro IC U1 regulates the number of switch pulses to maintain a fixed output current.

During constant current (CC) operation, when the output voltage falls, the secondary-side controller inside InnoSwitch3-Pro IC U1 will power itself from the secondary winding directly. During the on-time of the primary-side power switch, the forward voltage that appears across the secondary winding is used to charge the SECONDARY BYPASS pin decoupling capacitor C12 via resistor R16 and an internal regulator. This allows output current regulation to be maintained down to the minimum UV threshold. Below this level the unit enters auto-restart until the output load is reduced.

When the output current is below the CC threshold, the converter operates in constant voltage mode. The output voltage is monitored by the VOUT pin of the InnoSwitch3-Pro IC. Similar with current regulation, the output voltage is also compared to an internal voltage threshold that is set via the I^2C interface and the controller inside IC U1 regulates the output voltage by controlling the number of switch pulses. Capacitor C21 is needed between the VOUT pin and the SECONDARY GROUND pin for ESD protection of the VOUT pin.

N-channel MOSFET Q1 functions as the bus switch which connects or disconnects the output of the flyback converter from the USB Type-C receptacle. Q1 is controlled by the VB/D pin on the InnoSwitch3-Pro IC. Resistor R8 and diode D1 are connected across the Source and Gate terminals of the Q1 to provide a discharge path for the bus voltage when the Q1 is turned off. Capacitors C7 is used at the output for ESD protection.

In this design, VP302 (U3) is the USB Power Delivery (USB PD) controller. It is powered by the InnoSwitch3-Pro IC through the μVCC pin. USB PD protocol is communicated over either CC1 or CC2 line depending on the orientation in which Type-C plug is connected.

VP302 communicates with InnoSwitch3-Pro IC through the I^2C interface using the SCL and SDA lines in which it sets the CV, CC, V_{KP}, OVA and UVA parameters. These parameters correspond to the output voltage, constant output current, constant output power voltage threshold, output overvoltage threshold, and output undervoltage threshold registers of the InnoSwitch3-Pro IC, respectively. The status of the InnoSwitch3-Pro IC is read by the VP302 IC from the telemetry registers also using the I^2C interface.

Capacitors C17 and C18 provide decoupling to the μVCC of the InnoSwitch3-Pro IC and VCC of the VP302 IC. Capacitors C19 and C20, resistors R24 and R25, and TVS diodes D7, and D8 provide protection from ESD to pins CC1 and CC2.

Thermistor R23 is connected to NTC pin of the VP302 IC to provide temperature detection of the USB Type-C receptacle. The VBUS pin of the VP302 IC is used to sense the output voltage at the USB Type-C receptacle, which is the voltage after the bus

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switch Q1. The VBUS pin is also used for discharging the capacitor C7 when the bus switch Q1 is opened.

5 PCB Layout

PCB is 4-layer with total thickness of 0.8 mm. Copper weight for Top and Bottom layers is 2 oz. while Inner layers is 3 oz.

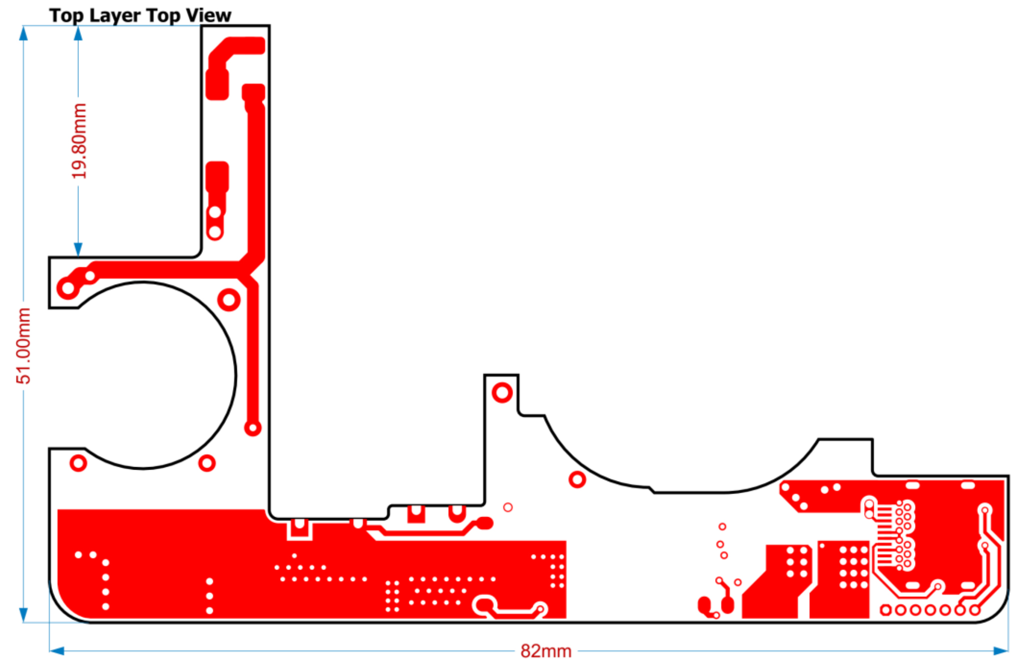

Figure 8 – Motherboard Printed Circuit Layout, Top.

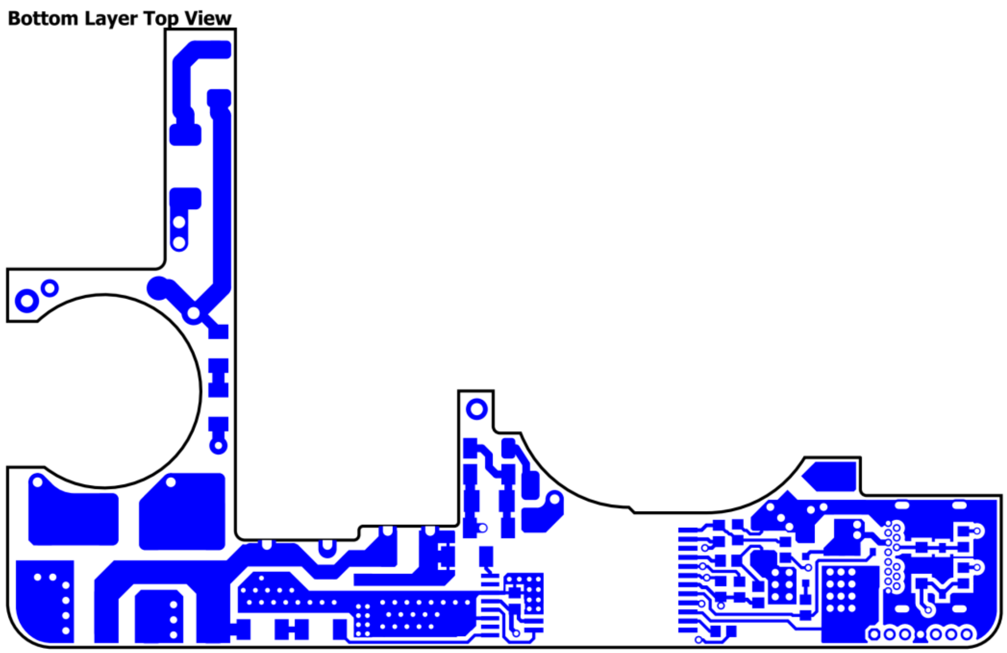

Figure 9 – Motherboard Printed Circuit Layout, Bottom.

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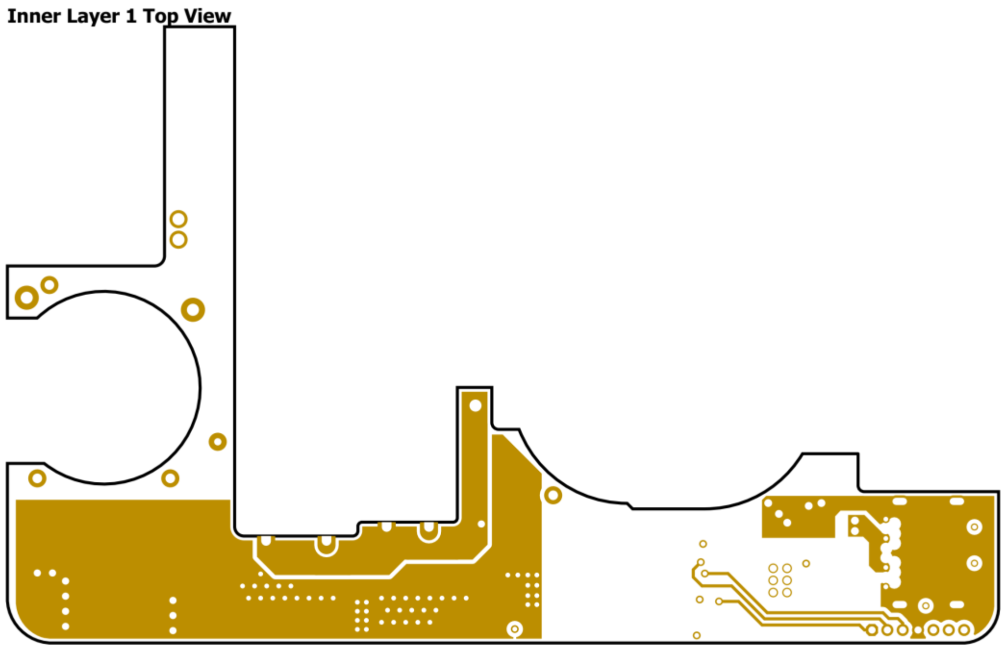

Figure 10 – Motherboard Printed Circuit Layout, Inner 1.

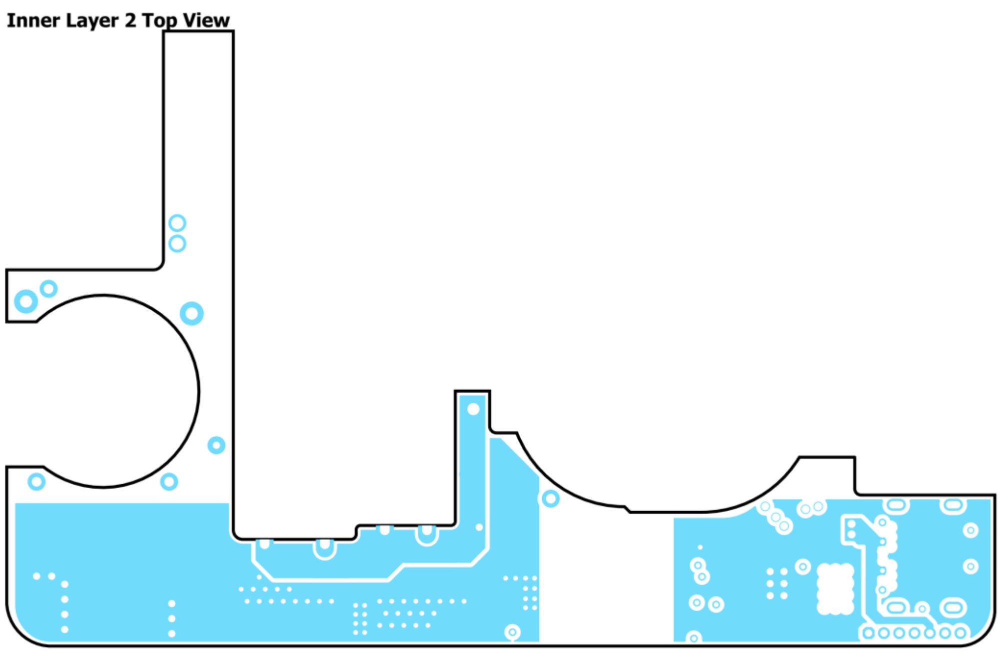

Figure 11 – Motherboard Printed Circuit Layout, Inner 2.

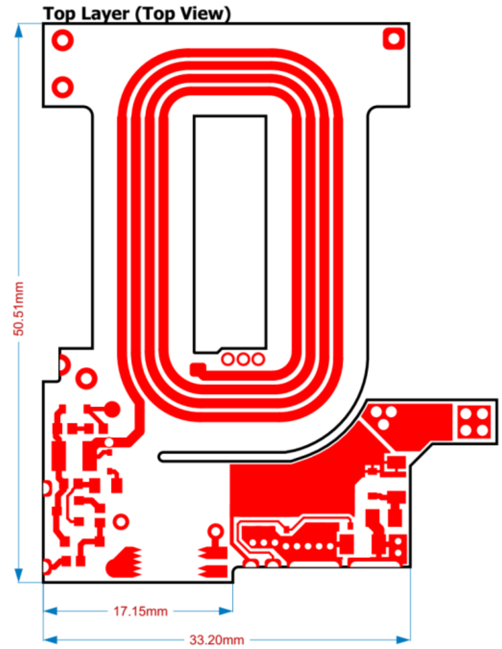

Figure 12 – SR FET, Bias Supply, and Primary-Side Winding PCB, Top and Bottom Layers.

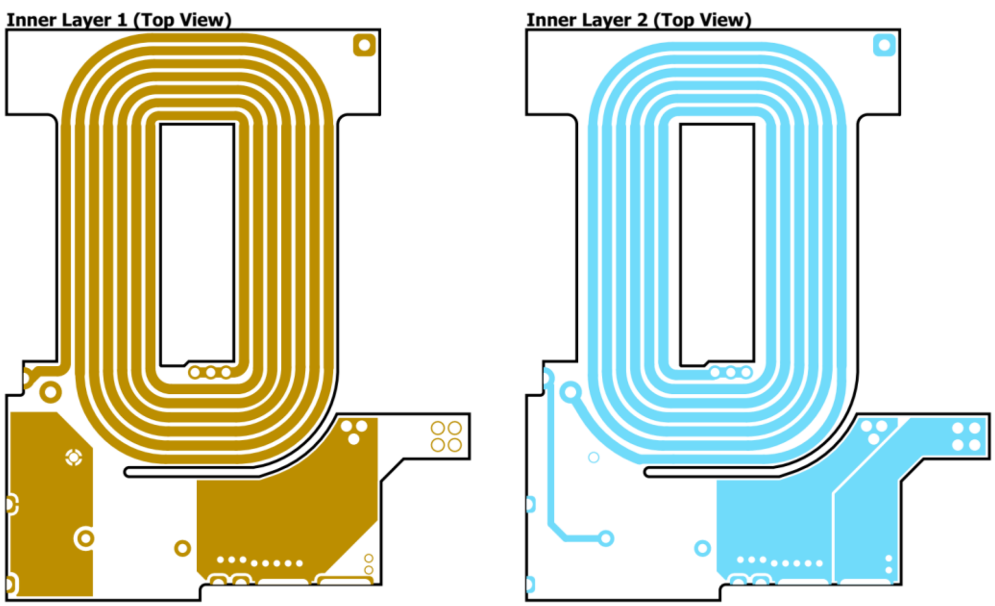

Figure 13 – SR FET, Bias Supply, and Primary-Side Winding PCB, Inner Layers.

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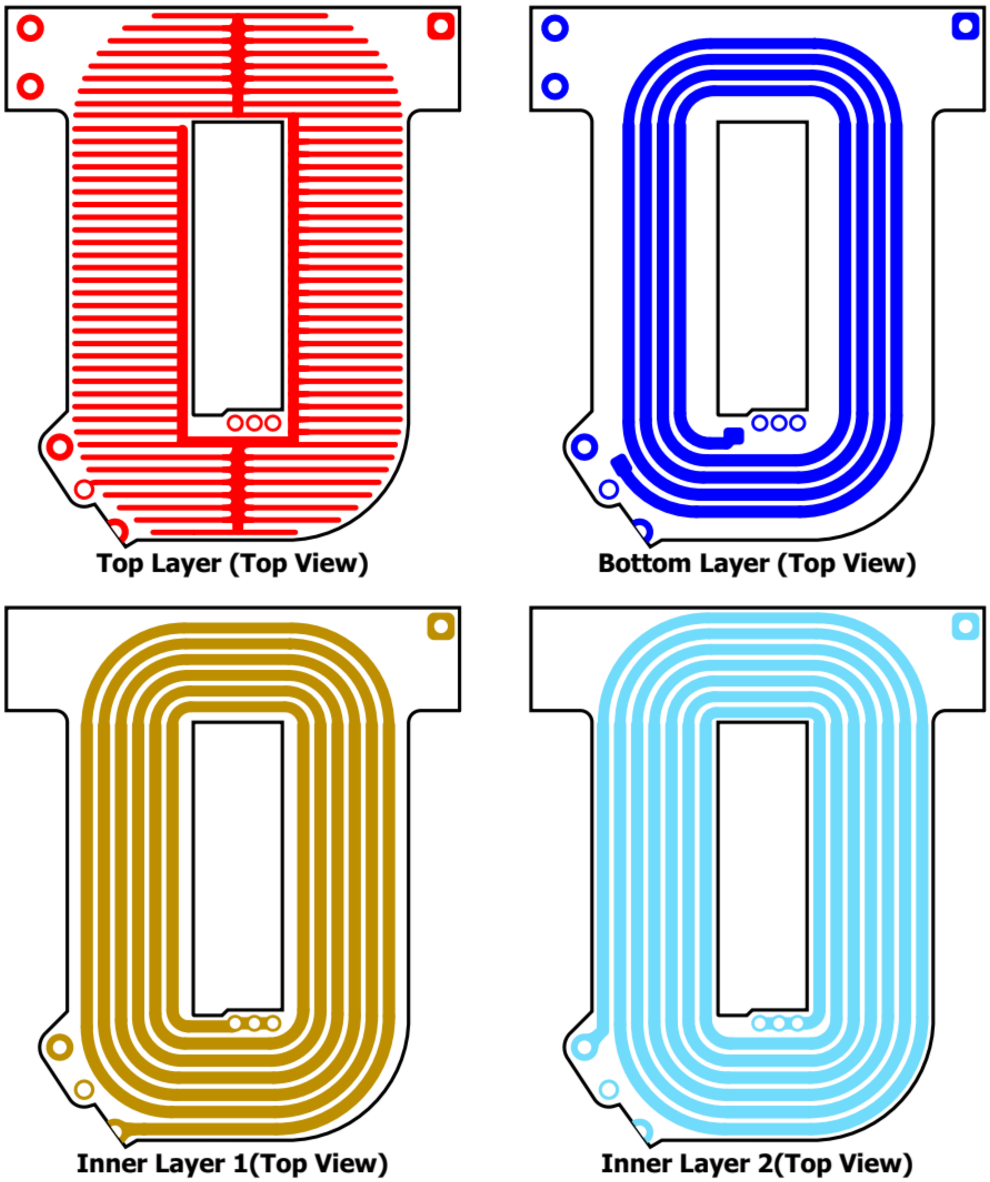

Figure 14 – Primary and Bias Winding PCB 2, All Layers.

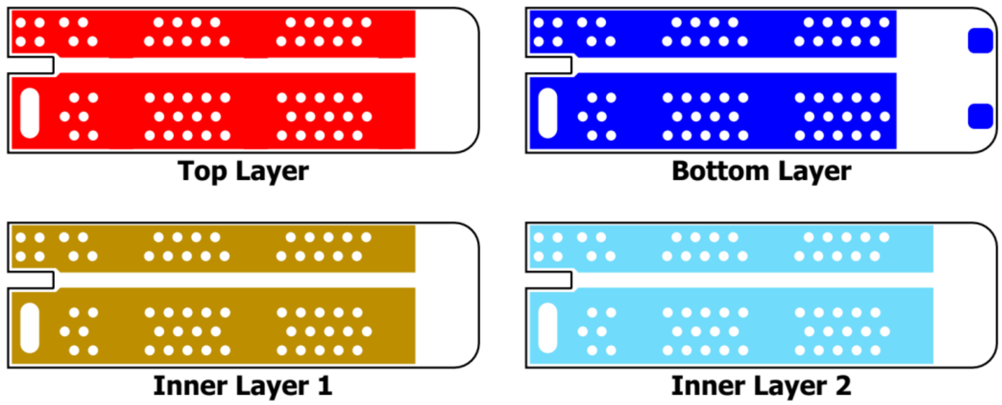

Figure 15 – Output Capacitor Bank PCB, All Layers.

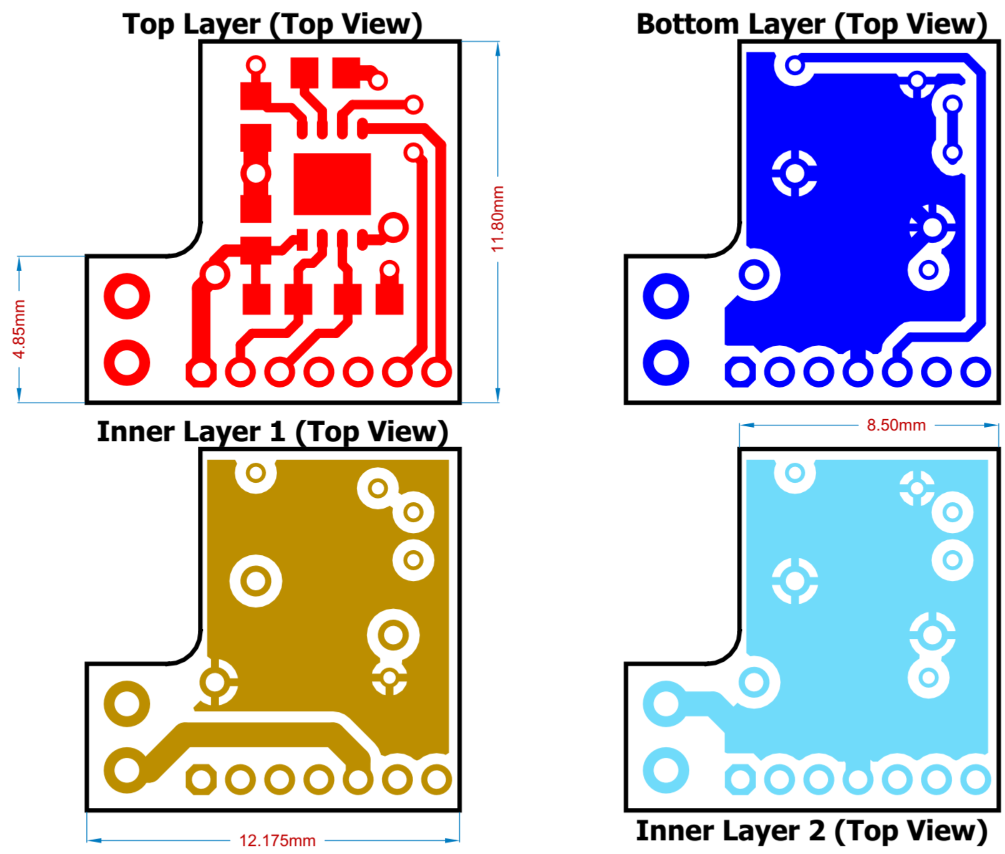

Figure 16 – PD Controller PCB, All Layers.

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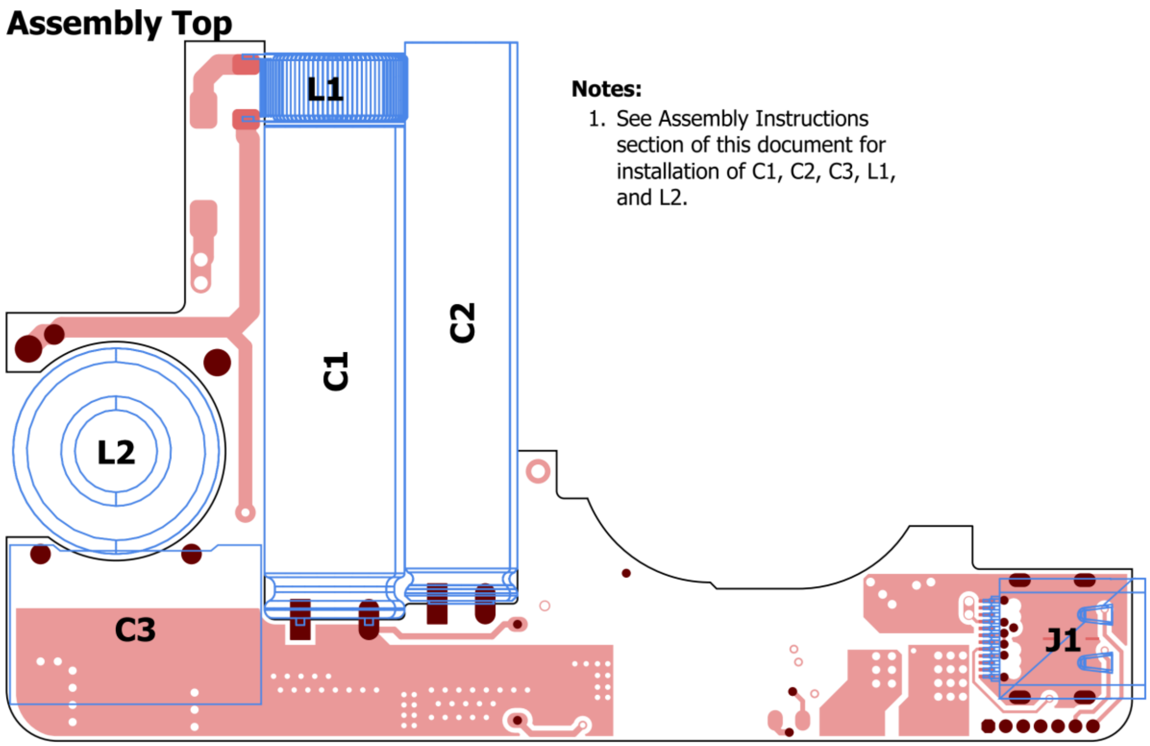

Figure 17 – Motherboard Printed Circuit Assembly Top.

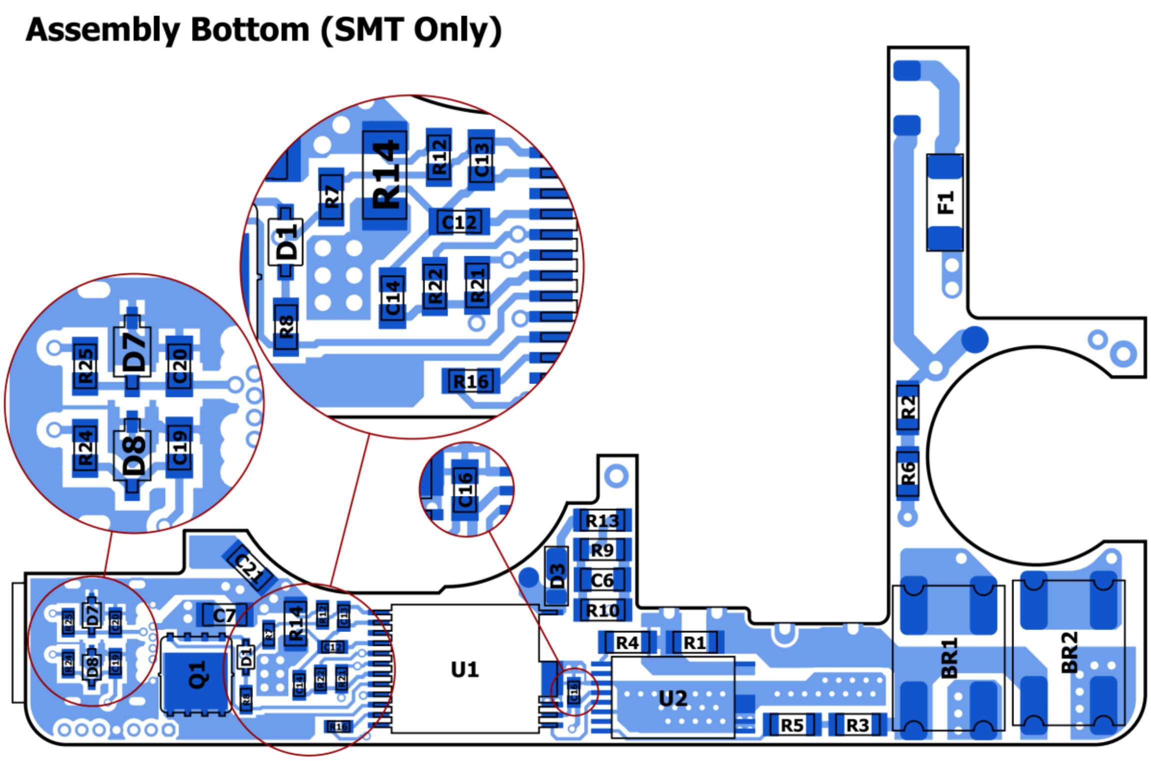

Figure 18 – Motherboard Printed Circuit Assembly Bottom.

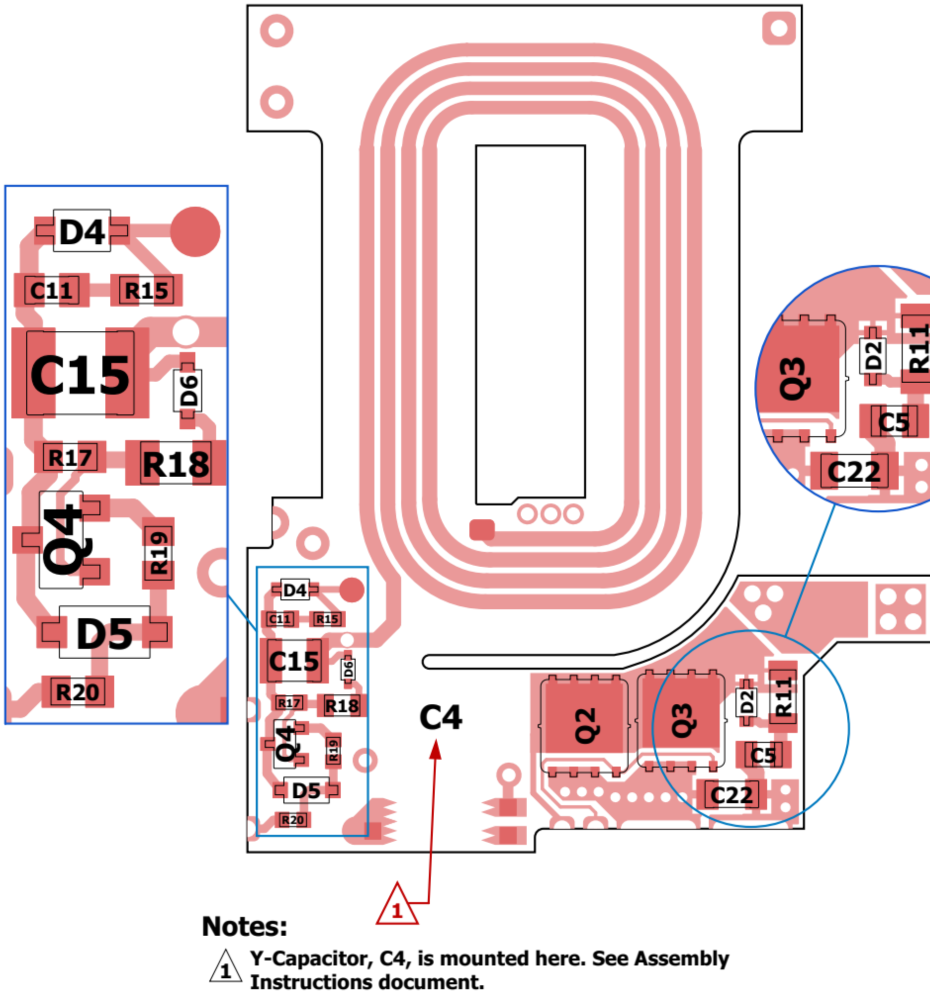

Figure 19 – SR FET, Bias Supply, and Primary Side Winding PCB Assembly Top.

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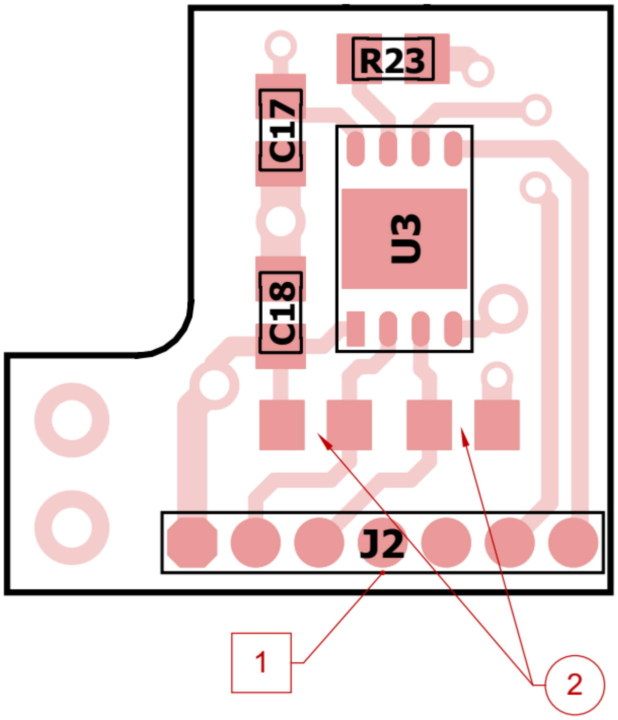

Notes:

1. See assembly instructions for installation of J2 and mating of PD Controller Board with Main Board
2. Alternate location for R21 and R22 only. DO NOT POPULATE if R21 and R22 already present in Main PCB.

Figure 20 – PD Conroller Board Printed Circuit Assembly Top.

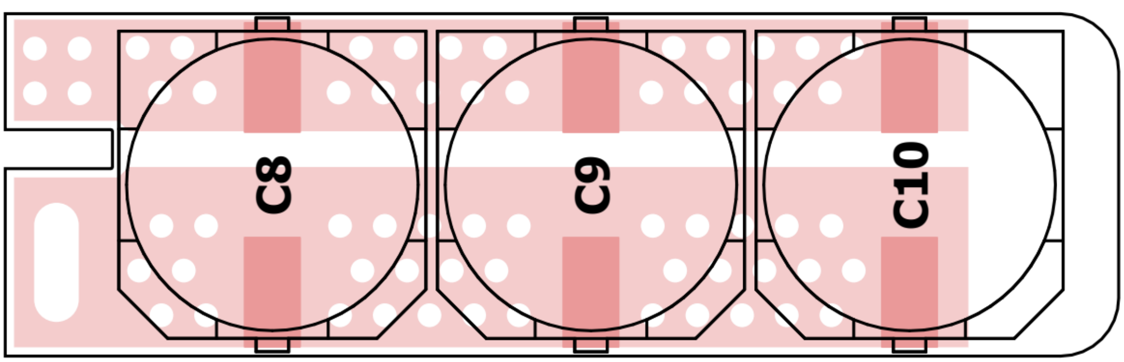

Figure 21 - Output Capacitor Bank Printed Circuit Assembly Top

Note:
Component references R2 and R6, although present in the layout, should not be populated.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	2	BR1, BR2	RECT BRIDGE, GP, 800 V, 4A, Z4-D	Z4DGP408L-HF	Comchip
2	1	C1	CAP ALUM 39 μF 20% 400 V TH	400BXW39MEFR10X35	Rubycon
3	1	C2	CAP ALUM 100 μF 20% 160 V RADIAL	160TXW100MEFR8X40	Rubycon
4	1	C3	CAP FILM 0.22 μF 10% 560 VDC RAD	R46KI322040P0K	KEMET
5	1	C4	CAP CER 3300 pF 760 VAC Y5U RADIAL	VY1332M59Y5UQ63V0	Vishay
6	1	C5	CAP CER 0805 2.2 nF 250V X7R 10%	C0805C222KARACAUTO	KEMET
7	1	C6	CAP CER 4700 pF 250V X7R 1206	C1206C472KARAC7800	KEMET
8	3	C7, C21, C22	CAP CER 10 μF 35V X7R 1206	C3216X7R1V106K160AC	TDK
9	3	C8, C9, C10	CAP ALUM POLY 330 μF 20% 25V SMD	PCR1E331MCL1GS	Nichicon
10	5	C12,C13, C14,C17, C18	CAP 2.2 uF, 10 V, Ceramic, X7R, 0603	GRM188R71A225KE15D	Murata
11	1	C15	CAP CER 10 μF 63V X7R 1210	CL32B106KMVNNWE	Samsung
12	1	C16	0.47 uF, 10 V, Ceramic, X5R, 0603	CGA3E3X7R1E474K080A B	TDK
13	2	C19, C20	CAP 560 pF, 50 V, Ceramic, X7R, 0603, 0.063" L x 0.031" W (1.60 mm x 0.80 mm)	CL10B561KB8NNNC	Samsung
14	1	D1	DIODE GEN PURP 100 V 200 mA SOD323	BAV19WS-7-F	Diodes, Inc.
15	1	D2	DIODE GEN PURP 200 V 200 mA SOD323	BAV21WS-7-F	Diodes, Inc.
16	1	D3	800 V, 1 A, Fast Recovery Rectifier, POWERDI123	15-01244-00	Diodes, Inc.
17	1	D4	DIODE, GEN PURP, FAST RECOVERY, 300 V, 225 mA, SOD323	BAV3004WS-7	Diodes, Inc.
18	1	D5	DIODE ZENER 47 V 500 mW SOD123	MMSZ5261BT1G	ON Semi
19	1	D6	10 V, 5%, 150 mW, SSMINI-2	DZ2S100M0L EDZVT2R10B	Panasonic Rohm
20	2	D7, D8	DIODE, ZENER, 24 V, 200MW, SC-90, SOD-323F, SMini2-F5-B	15-01042-00	Panasonic
21	1	F1	2.5 A 125 V AC 125 V DC Fuse Board Mount (Cartridge Style Excluded) SMT 2-SMD, Square End Block	SST 2.5	Bel Fuse
22	1	J1	Connector, "Certified", USB - C, USB 3.1, For 0.062" PCB Material, Superspeed+, 24 Pos, SMT, RA, TH	6.32723E+11	Wurth
23	1	J2	CONN HEADER VERT 7POS 1.27MM	GRPB071VWVN-RC	Sullins Connector
24	1	J3	PWR ENT RCPT IEC320-C8 PNL SLDR	770W-X2/10	Qualtek
25	1	L1	250 μH, Toroidal Common Mode Choke, custom, DER-538, wound on 32-00275-00 core.	32-00367-00	Power Integrations
26	1	L2	Custom, CMC, 20 mH @ 10 kHz, Toroidal, 17.5 mm OD x 11.0 mm thick. 45 turns x 2, 0.40 mm wire 190 mΩ max	30-04126-00	Power Integrations
27	1	Q1	30V N-CHANNEL MOSFET	AONS32304	Alpha & Omega Semi
28	2	Q2, Q3	120V N-CHANNEL MOSFET	AON62922	Alpha & Omega Semi
29	1	Q4	NPN, Small Signal BJT, 80 V, 0.5 A, SOT-23	MMBTA06LT1G	On Semi
30	1	R1	RES SMD 3.9 MΩ 5% 1/4W 1206	ERJ-8GEYJ395V	Panasonic
31	1	R3	RES, 1.80 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1804V	Panasonic
32	1	R4	RES, 1 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ105V	Panasonic
33	3	R2, R5, R6	RES, 2.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
34	1	R7	RES, 324 kΩ, 1%, 1/8 W, Thick Film, 0603	RC0603FR-07324KL	Yageo
35	1	R8	RES, 100 Ω, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1000V	Panasonic
36	2	R9, R10	RES, 680 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ684V	Panasonic
37	1	R11, R13	RES, 20 R, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ200V	Panasonic

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38	1	R12	RES, 10 Ω, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF10R0V	Panasonic
39	1	R14	RES 0.006 Ω 1% ½ W 1206	PR1206FKE7W0R006Z	Yageo
40	1	R16, R20	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
41	1	R17	RES, 100 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1003V	Panasonic
42	1	R18	RES, 5.1 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ512V	Panasonic
43	1	R19	RES SMD 2.2 KΩ 0.1% 1/10W 0603	ERA-3AEB222V	Panasonic
44	2	R21, R22	RES SMD 10 kΩ 1% 1/10W 0603	ERJ-3EKF1002V	Panasonic
45	1	R23	THERM NTC 100 kΩ 4250K 0603	NCP18WF104D03RB NTCG164KF104FT1S	Murata TDK
46	2	R24, R25	RES, 22 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ220V	Panasonic
47	1	U1	InnoSwitch3-Pro SIZE 10	INN3370C-H302	Power Integrations
48	1	U2	MinE-CAP	MIN1072M	Power Integrations
49	1	U3	IC, USB PD Type-C Controller for SMPS, DFN-8	VP 302	Via Labs
50	1	T1	Ferrite Core E32/6/20 Planar E 3C95	E32/6/20/R-3C95	Ferroxcube
51	1	T1	Ferrite Core E32/6/20 Planar I 3C95	PLT32/20/3.2/R-3C95	Ferroxcube

7 Transformer Specification

7.1 *Electrical Diagram*

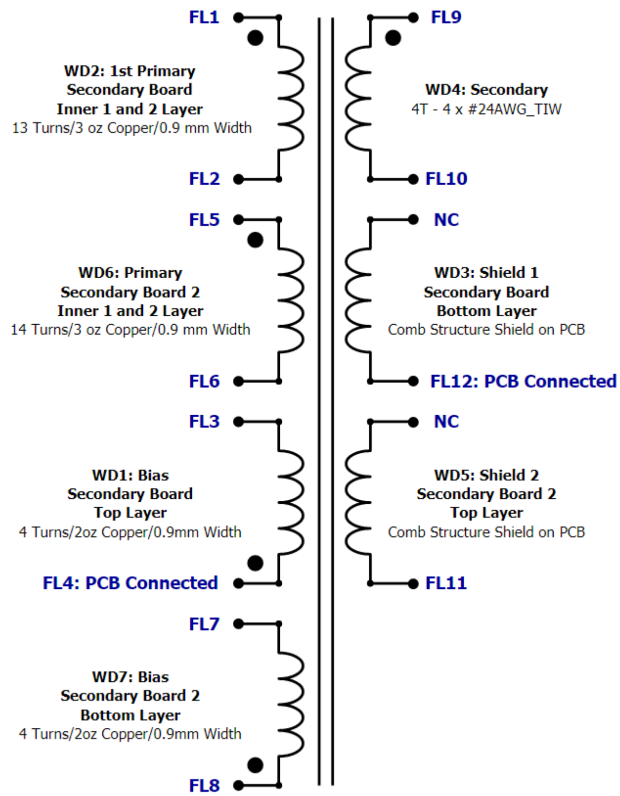

Figure 22 – Transformer Electrical Diagram.

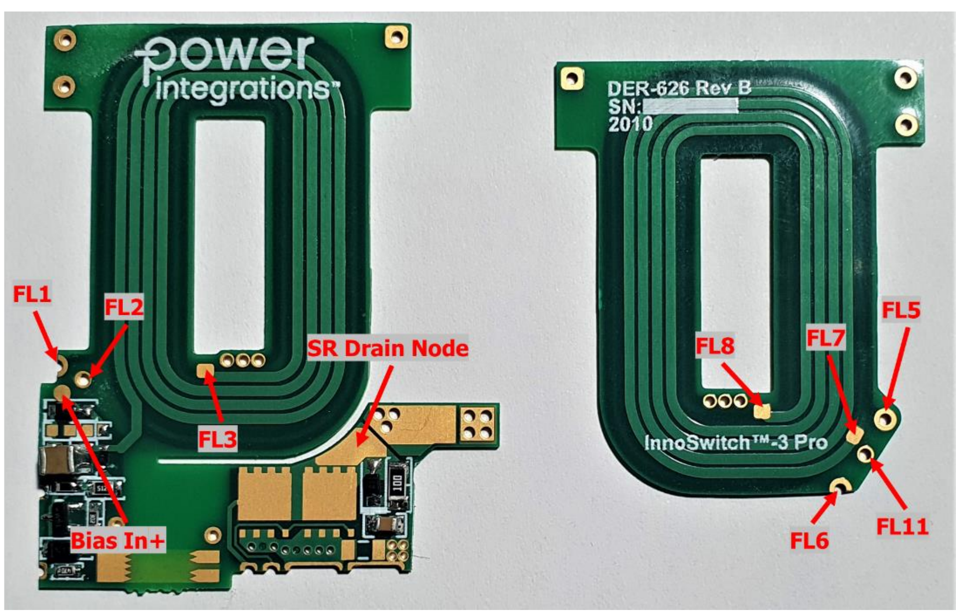

Figure 23 – Secondary PCBs 1 and 2 with Port Labels.

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7.2 *Electrical Specifications*

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 50 kHz switching frequency, between FL1 and FL6, with all other windings open. FL2 and FL5 shorted.	555 μH± 5%
Resonant Frequency	Between pin FL1 and FL6, other windings open. FL2 and FL5 shorted.	1500 kHz (Min.)
Primary Leakage Inductance	Between pin FL1 and FL6, with shorted FL9 and FL10. FL2 and FL5 shorted.	4.5 μH (Max.)

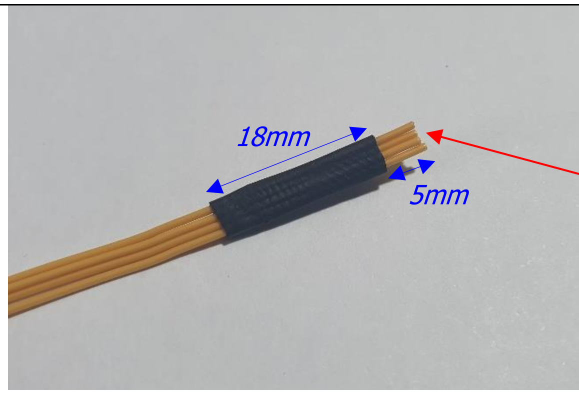
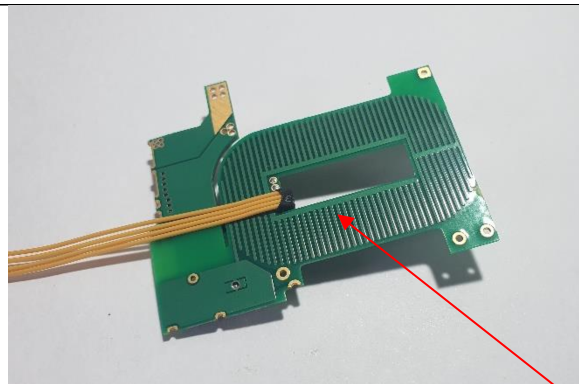
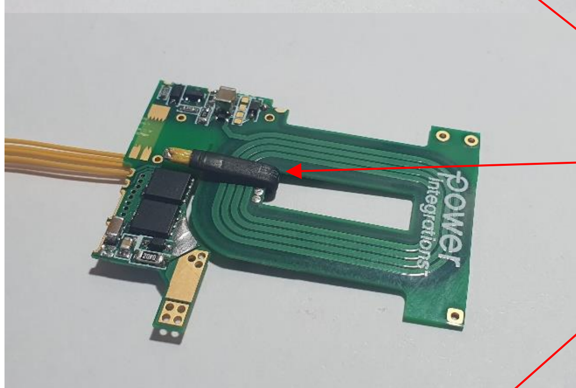
7.3 *Material List*

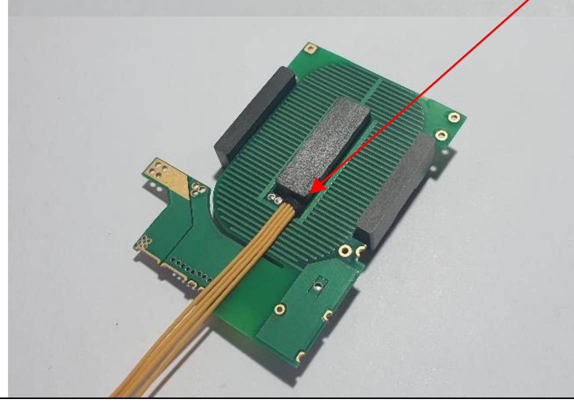
Item	Description
[1]	Core: E32/6/20/R-3C95 + PLT32/20/3.2/R-3C95, Ferroxcube.
[2]	Magnet Wire: #24 AWG, Triple Insulated Wire.
[3]	Wire-wrapping Wire: #26AWG, Kynar Wire.
[4]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 8.2 mm Width.
[5]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 30 mm x 55 mm.
[6]	2.5 mm Shrink Tube.
[7]	Varnish: Dolph BC-359.

7.4 *Transformer Construction*

Primary Winding and Secondary PCB Preparation	Populate the Secondary Board with all surface mount components for the Bias Supply circuit, SR FETs and snubber. Prepare 4 strands of Item [2] with a length of 35 cm. Place an 18 mm, 2.5 mm diameter heat shrink tube (Item [6]) on one end of the TIW. Leave a 5 mm allowance at the end of the wire to be used to solder the TIW to the DRAIN node of the SR FETs. Make sure to keep the 4 strands of wire flat when heating the shrink tube. The end of the wire with the heat shrink tube will be FL9.
Secondary Winding	Bend the 4-strand TIW 90 degrees 15 mm from the end. Insert the wire into the hole for the center leg on the transformer on the secondary PCB. Position the wire on the notch in the PCB. Place the E-core section of the transformer core and then insert the second secondary PCB. The longer part of the bent TIW must be in between the two secondary PCBs. Place the I-section of the core and tape the whole assembly using Item [4]. There will be a gap between the center leg of the core and the secondary PCB. Insert two 50mm wire wrapping wires Item [3] through the gap near the TIW wires. Teflon tubes can be used to protect Item [3]. Connect FL3 to FL8. Use another strand of Item [3] to connect FL7 to Bias In+. Wind the secondary 4 times around the center leg of the core as shown in the images in the next section.
Finish Assembly	Place solder on the end of FL9. Bend the wire and position the soldered section over the pad near the Drain node of the SR FETs. Solder FL9 in place. Apply varnish on the transformer section of the assembly only. Ideally, varnish must only be applied between the secondary PCBs to secure the secondary windings. Solder Y-capacitor C4 in place. Varnish with Item [12].

7.5 *Transformer Assembly Illustrations*

<table>
<tr>
<td>Primary Winding and Secondary PCB Preparation</td>
<td>
</td>
<td>The 4 Strand AWG 24 TIW must be flat when the heat shrink is heated.</td>
</tr>
<tr>
<td>Secondary Winding</td>
<td>


</td>
<td>Insert the end of the wire with the heat shrink into the center leg hole.

Bend the wire further to secure the wire when inserting the core.

Make sure the secondary winding is bent at a location where the shrink tube will protect the TIW from the edge of the PCB.</td>
</tr>
</table>

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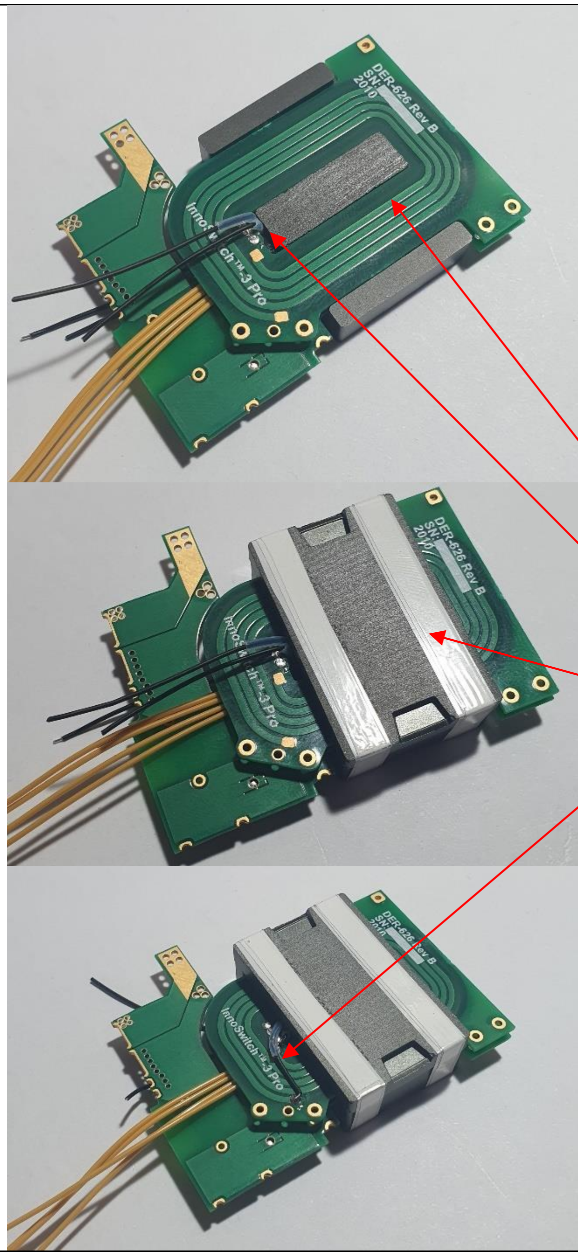
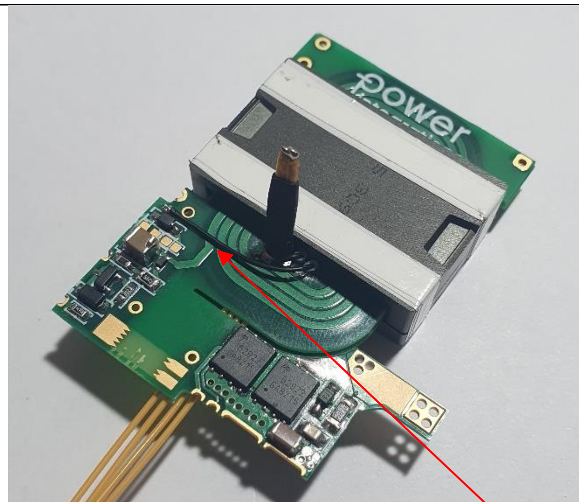
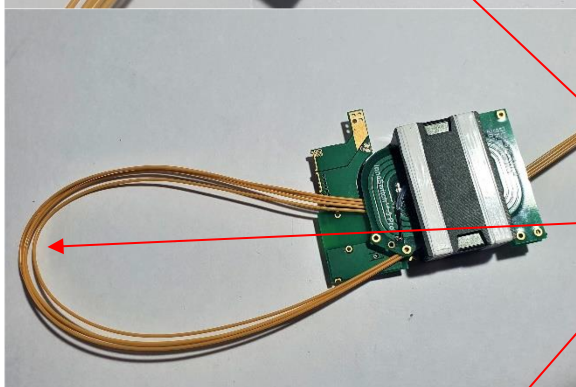
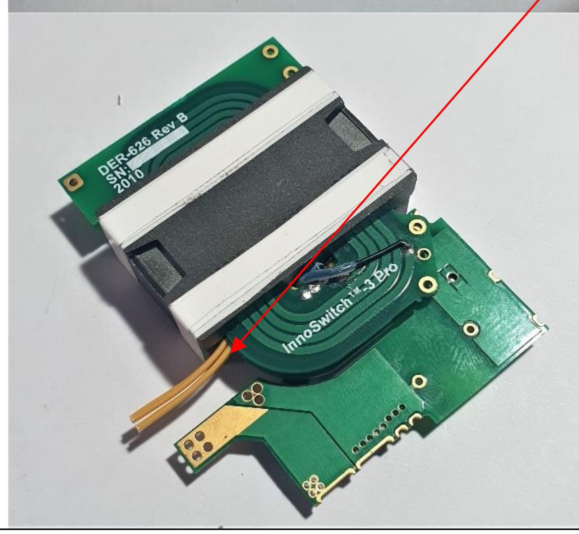
Secondary Winding		Position the 2nd secondary PCB. Insert Item [3] through gap between PCB and core leg. Position the I-section of the core and use Item [4] to secure the whole assembly. Connect Auxiliary Winding jumpers. Connect FL3 to FL8 and FL7 to Bias In+.

<table>
<tr>
<td>Secondary Winding</td>
<td>



</td>
<td>Connect Auxiliary Winding jumpers.

Wind the secondary winding between the PCBs and around the core center leg 4 times.

Completed winding.</td>
</tr>
</table>

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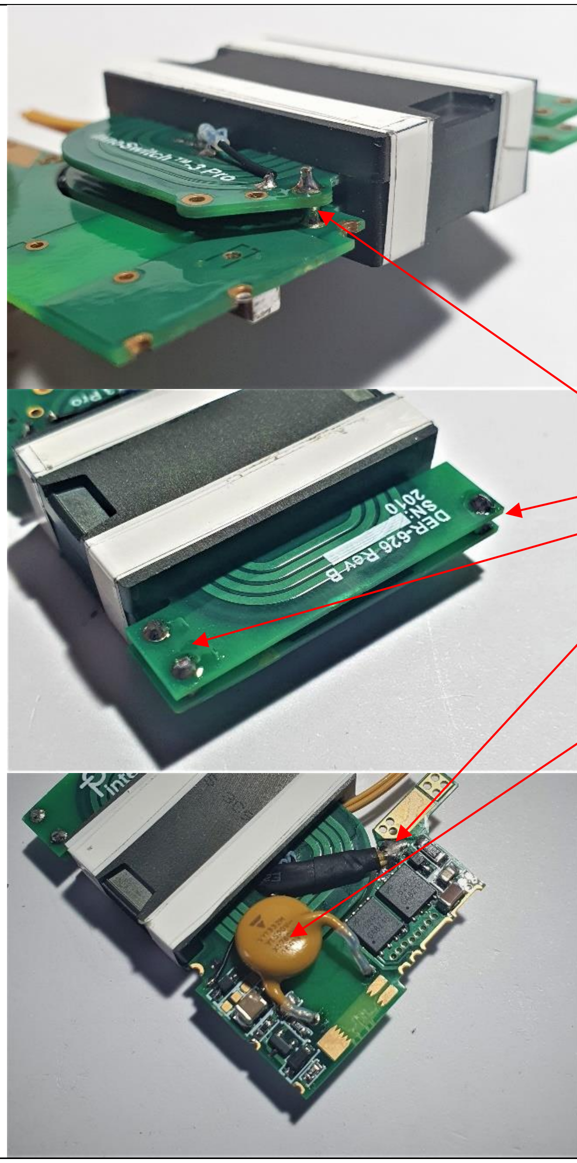
Finish Assembly		Use 1mm wire to connect the FL2 to FL5. Secure the PCBs by soldering 1mm jumpers at these locations. Solder FL9 to the SR FET Drain node pad. Position and install the Y-cap C4. Use Teflon tubing to insulate the capacitor leads.

8 Common Mode Choke Specifications

8.1 *250 μH Common Mode Choke (L1)*

8.1.1 Electrical Diagram

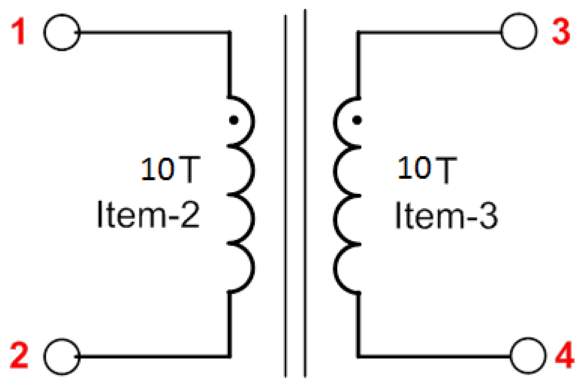


Figure 24 – Inductor Electrical Diagram.

8.1.2 Electrical Specifications

Winding Inductance	Pin 1 – pin 2 (pin 3 – pin 4), all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	250 μH ±20%

8.1.3 Material List

Item	Description
[1]	Toroidal Core: 35T0375-10H, PI#: 32-00275-00.
[2]	Triple Insulated Wire: #26 AWG, Triple Coated.
[3]	Magnet Wire: #26 AWG, Double Coated.

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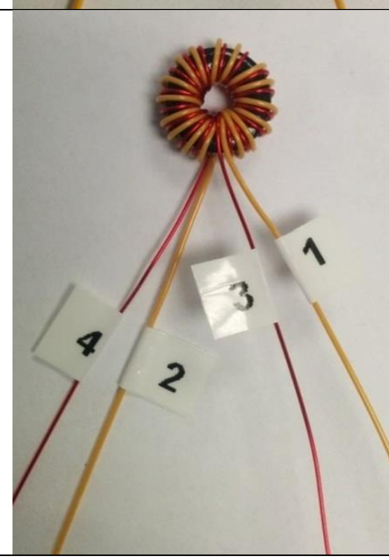
8.1.4 Winding Instructions

Mark the start end of the winding as 1 and wind 10 turns of Item [2] on Item [1]. Mark the end of this winding as 2	
Repeat the same procedure as above for the other winding using Item [3], making sure that the start/end and the direction of winding is the same as the first winding. Varnish using Item [4]. Mark the start of this winding as 3 and the end as 4.	

8.2 ***20 mH Common Mode Choke (L2)***

8.2.1 Electrical Diagram

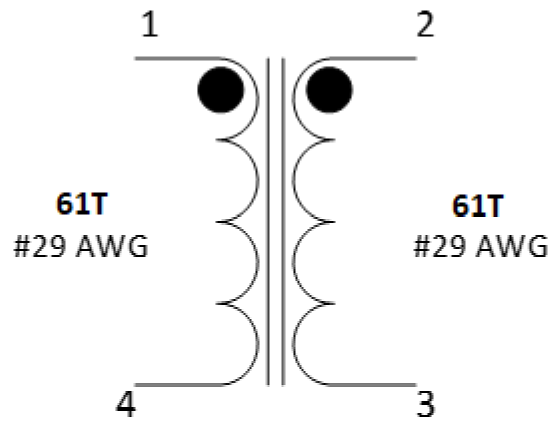


Figure 25 – Inductor Electrical Diagram.

8.2.2 Electrical Specifications

Inductance	Pins 1 - 4 and pins 2 - 3 measured at 10 kHz.	20 mH ±25%
Core effective Inductance Index		5950 nH/N^2
Leakage Inductance	Pins 1 - 4, with pins 2 - 3 shorted.	80 μH ±10%

8.2.3 Material List

Item	Description
[1]	Toroid: FERRITE INDUCTOR TOROID T14 x 8 x 5.5, PI#: 32-00286-00.
[2]	Divider: Cable Tie, Panduit - Fish Paper, Insulating Cotton Rag, 0.010” Thick, PI#: 66-00042-00.
[3]	Magnet Wire: #29 AWG Heavy Nyleze.
[4]	Epoxy: Devon, 5 mins Epoxy; or Equivalent.

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8.2.4 Winding Instructions

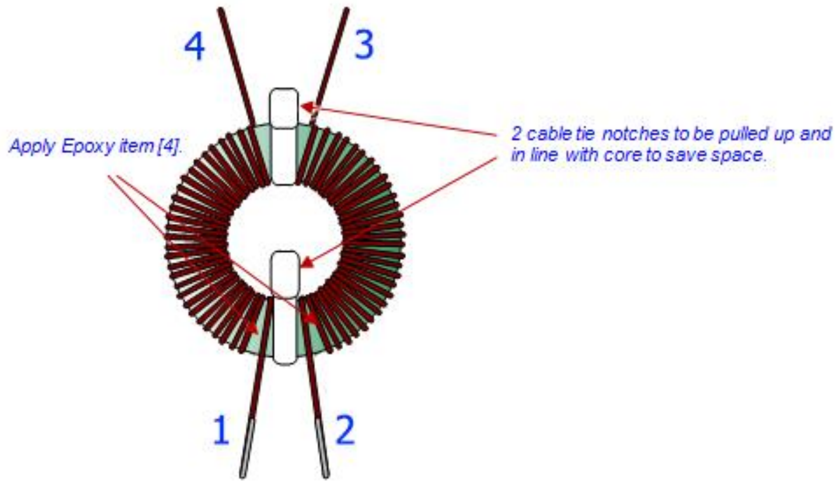

Figure 26 – 20 mH CMC Illustration Image.

- Place 2 pieces of cable tie Item [2] on to toroid Item [1] to divide 2 equal sections.
- Use 4 ft of wire Item [3], start as 1, wind 55 turns in 2 layers in a half section of toroid, and end as 4.
- Do the same for another half of Toroid, start as 2 and end as 3.
- Pull up 2 notches of cable ties to be in line with toroid body (to save space) and apply Epoxy Item [4] where leads floating.

9 Transformer Design Spreadsheet

1	ACDC_Flyback_061319; Rev.0.1; Copyright Power Integrations 2019	INPUT	INFO	OUTPUT	UNITS	Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	VAC_MIN	90		90	V	Minimum AC line voltage
4	VAC_MAX			265	V	Maximum AC input voltage
5	VAC_RANGE			UNIVERSAL		AC line voltage range
6	FLINE			50	Hz	AC line voltage frequency
7	CAP_INPUT	139.0		139.0	uF	Input capacitance
9	**SET-POINT 1**					
10	VOUT1	20.00		20.00	V	Output voltage 1, should be the highest output voltage required
11	IOUT1	3.250		3.250	A	Output current 1
12	POUT1			63.00	W	Output power 1
13	EFFICIENCY1	0.92		0.92		Converter efficiency for output 1
14	Z_FACTOR1	0.50		0.50		Z-factor for output 1
16	**SET-POINT 2**					
17	VOUT2	15.00		15.00	V	Output voltage 2
18	IOUT2	3.000		3.000	A	Output current 2
19	POUT2			45.00	W	Output power 2
20	EFFICIENCY2	0.92		0.92		Converter efficiency for output 2
21	Z_FACTOR2	0.50		0.50		Z-factor for output 2
23	**SET-POINT 3**					
24	VOUT3	9.00		9.00	V	Output voltage 3
25	IOUT3	3.000		3.000	A	Output current 3
26	POUT3			27.00	W	Output power 3
27	EFFICIENCY3	0.92		0.92		Converter efficiency for output 3
28	Z_FACTOR3	0.50		0.50		Z-factor for output 3
30	**SET-POINT 4**					
31	VOUT4	5.00		5.00	V	Output voltage 4
32	IOUT4	3.000		3.000	A	Output current 4
33	POUT4			15.00	W	Output power 4
34	EFFICIENCY4	0.92		0.92		Converter efficiency for output 4
35	Z_FACTOR4	0.50		0.50		Z-factor for output 4
37	**SET-POINT 5**					
38	VOUT5	3.30		3.30	V	Output voltage 5
39	IOUT5	3.000		3.000	A	Output current 5
40	POUT5			9.90	W	Output power 5
41	EFFICIENCY5	0.90		0.90		Converter efficiency for output 5
42	Z_FACTOR5	0.50		0.50		Z-factor for output 5
44	**SET-POINT 6**					
45	VOUT6			0.00	V	Output voltage 6
46	IOUT6			0.000	A	Output current 6
47	POUT6			0.00	W	Output power 6
48	EFFICIENCY6			0.00		Converter efficiency for output 6
49	Z_FACTOR6			0.00		Z-factor for output 6
51	**SET-POINT 7**					
52	VOUT7			0.00	V	Output voltage 7
53	IOUT7			0.000	A	Output current 7
54	POUT7			0.00	W	Output power 7
55	EFFICIENCY7			0.00		Converter efficiency for output 7
56	Z_FACTOR7			0.00		Z-factor for output 7
58	**SET-POINT 8**					
59	VOUT8			0.00	V	Output voltage 8
60	IOUT8			0.000	A	Output current 8
61	POUT8			0.00	W	Output power 8
62	EFFICIENCY8			0.00		Converter efficiency for output 8
63	Z_FACTOR8			0.00		Z-factor for output 8

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65	**SET-POINT 9**					
66	VOUT9			0.00	V	Output voltage 9
67	IOUT9			0.000	A	Output current 9
68	POUT9			0.00	W	Output power 9
69	EFFICIENCY9			0.00		Converter efficiency for output 9
70	Z_FACTOR9			0.00		Z-factor for output 9
71						
72	VOLTAGE_CDC	0.000		0.000	V	Cable drop compensation desired at full load
76	**PRIMARY CONTROLLER SELECTION**					
77	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
78	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
79	VDRAIN_BREAKDOWN	750		750	V	Device breakdown voltage
80	DEVICE_GENERIC	AUTO		INN33X0		Device selection
81	DEVICE_CODE			INN3370C		Device code
82	PDEVICE_MAX			75	W	Device maximum power capability
83	RDSON_25DEG			0.39	Ω	Primary switch on-time resistance at 25°C
84	RDSON_100DEG			0.54	Ω	Primary switch on-time resistance at 100°C
85	ILIMIT_MIN			2.139	A	Primary switch minimum current limit
86	ILIMIT_TYP			2.300	A	Primary switch typical current limit
87	ILIMIT_MAX			2.461	A	Primary switch maximum current limit
88	VDRAIN_ON_PRSW			0.40	V	Primary switch on-time voltage drop
89	VDRAIN_OFF_PRSW			575.31	V	Peak drain voltage on the primary switch during turn-off
93	**WORST CASE ELECTRICAL PARAMETERS**					
94	FSWITCHING_MAX	65733	Info	65733	Hz	The worst case minimum operating frequency is less than 25kHz: may result in audible noise
95	VOR	132.0		132.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
96	VMIN			92.39	V	Valley of the rectified minimum input AC voltage at full load
97	KP			0.755		Measure of continuous/discontinuous mode of operation
98	MODE_OPERATION			CCM		Mode of operation
99	DUTYCYCLE			0.589		Primary switch duty cycle
100	TIME_ON		Info	13.12	us	Primary switch on-time
101	TIME_OFF			6.25	us	Primary switch off-time
102	LPRIMARY_MIN			527.4	uH	Minimum primary magnetizing inductance
103	LPRIMARY_TYP			555.1	uH	Typical primary magnetizing inductance
104	LPRIMARY_TOL			5.0	%	Primary magnetizing inductance tolerance
105	LPRIMARY_MAX			582.9	uH	Maximum primary magnetizing inductance
107	**PRIMARY CURRENT**					
108	IAVG_PRIMARY			0.737	A	Primary switch average current
109	IPEAK_PRIMARY			2.243	A	Primary switch peak current
110	IPEDESTAL_PRIMARY			0.492	A	Primary switch current pedestal
111	IRIPPLE_PRIMARY			2.109	A	Primary switch ripple current
112	IRMS_PRIMARY			1.056	A	Primary switch RMS current
113						
114	SECONDARY CURRENT					
115	IPEAK_SECONDARY			15.140	A	Secondary winding peak current
116	IPEDESTAL_SECONDARY			3.321	A	Secondary winding pedestal current
117	IRMS_SECONDARY			5.952	A	Secondary winding RMS current
118	IRIPPLE_CAP_OUT			4.986	A	Output capacitor ripple current
122	**TRANSFORMER CONSTRUCTION PARAMETERS**					
123	**CORE SELECTION**					

124	CORE	CUSTOM		CUSTOM		Core selection
125	CORE NAME		Info	0		Core code
126	AE	130.0		130.0	mm^2	Core cross sectional area
127	LE	35.1		35.1	mm	Core magnetic path length
128	AL	8750		8750	nH	Ungapped core effective inductance per turns squared
129	VE	4560		4560	mm^3	Core volume
130	BOBBIN NAME					Bobbin name
131	AW				mm^2	Bobbin window area
132	BW				mm	Bobbin width
133	MARGIN			0.0	mm	Bobbin safety margin
135	**PRIMARY WINDING**					
136	NPRIMARY			27		Primary winding number of turns
137	BPEAK			4183	Gauss	Peak flux density
138	BMAX			3672	Gauss	Maximum flux density
139	BAC			1719	Gauss	AC flux density (0.5 x Peak to Peak)
140	ALG			762	nH	Typical gapped core effective inductance per turns squared
141	LG			0.196	mm	Core gap length
142	LAYERS_PRIMARY			3		Primary winding number of layers
143	AWG_PRIMARY			25		Primary wire gauge
144	OD_PRIMARY_INSULATED			0.518	mm	Primary wire insulated outer diameter
145	OD_PRIMARY_BARE			0.455	mm	Primary wire bare outer diameter
146	CMA_PRIMARY			303.4	Cmils/A	Primary winding wire CMA
148	**SECONDARY WINDING**					
149	NSECONDARY	4		4		Secondary winding number of turns
150	AWG_SECONDARY			19		Secondary wire gauge
151	OD_SECONDARY_INSULATED			1.217	mm	Secondary wire insulated outer diameter
152	OD_SECONDARY_BARE			0.912	mm	Secondary wire bare outer diameter
153	CMA_SECONDARY			216.4	Cmils/A	Secondary winding wire CMA
155	**BIAS WINDING**					
156	NBIAS			8		Bias winding number of turns
160	**PRIMARY COMPONENTS SELECTION**					
161	**LINE UNDERVOLTAGE**					
162	BROWN-IN REQURED			72.00	V	Required line brown-in threshold
163	RLS			3.56	MΩ	Connect two 1.91 MOhm resistors to the V-pin for the required UV/OV threshold
164	BROWN-IN ACTUAL			71.40	V	Actual brown-in threshold using standard resistors
165	BROWN-OUT ACTUAL			64.58	V	Actual brown-out threshold using standard resistors
167	**LINE OVERVOLTAGE**					
168	OVERVOLTAGE_LINE			297.50	V	The device voltage stress will be higher than 600V when overvoltage is triggered
170	**BIAS WINDING**					
171	VBIAS		Info	9.00	V	The rectified bias voltage maybe too low to supply the BP pin: Increase the rectified bias voltage to a value higher than 9V
172	VF_BIAS			0.70	V	Bias winding diode forward drop
173	VREVERSE_BIASDIODE			119.61	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
174	CBIAS			22	uF	Bias winding rectification capacitor
175	CBPP			0.47	uF	BPP pin capacitor
179	**SECONDARY COMPONENTS SELECTION**					
180	**RECTIFIER**					
181	VDRAIN_OFF_SRFET			75.31	V	Secondary rectifier reverse voltage (not accounting parasitic voltage ring)
182	SRFET	AONS62922		AONS62922		Secondary rectifier (Logic MOSFET)

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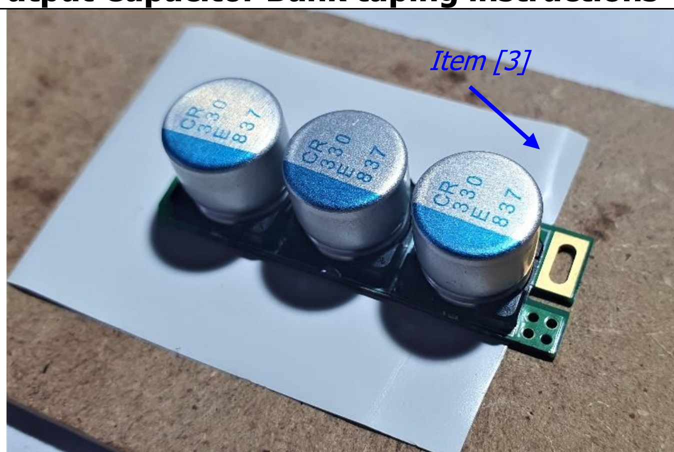
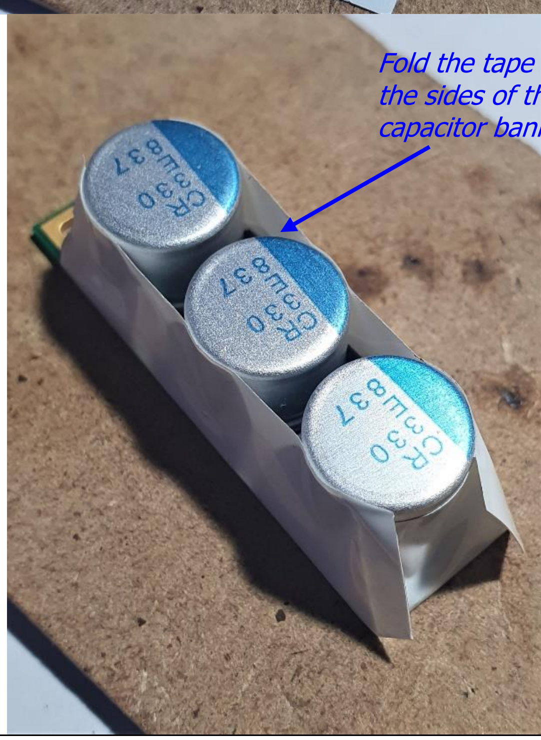
183	VBREAKDOWN_SRFET			120	V	Secondary rectifier breakdown voltage
184	RDSON_SRFET			7.0	mΩ	SRFET on time drain resistance at 25degC for VGS=4.4V
188	**SET-POINTS ANALYSIS**					
189	**TOLERANCE CORNER**					
190	USER_VAC	90		90	V	Input AC RMS voltage corner to be evaluated
191	USER_ILIMIT	MIN		2.139	A	Current limit corner to be evaluated
192	USER_LPRIMARY	MAX		582.9	uH	Primary inductance corner to be evaluated
194	**SET-POINT SELECTION**					
195	SET-POINT	4		4		Select the set-point which needs to be evaluated
196	FSWITCHING			24544.5	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
197	VOR			33.5	V	Voltage reflected to the primary winding when the primary switch turns off
198	VMIN			117.73	V	Valley of the minimum input AC voltage
199	KP			1.265		Measure of continuous/discontinuous mode of operation
200	MODE_OPERATION			DCM		Mode of operation
201	DUTYCYCLE			0.184		Primary switch duty cycle
202	TIME_ON			7.48	us	Primary switch on-time
203	TIME_OFF			33.26	us	Primary switch off-time
205	**PRIMARY CURRENT**					
206	IAVG_PRIMARY			0.139	A	Primary switch average current
207	IPEAK_PRIMARY			1.511	A	Primary switch peak current
208	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
209	IRIPPLE_PRIMARY			1.511	A	Primary switch ripple current
210	IRMS_PRIMARY			0.374	A	Primary switch RMS current
212	**SECONDARY CURRENT**					
213	IPEAK_SECONDARY			10.197	A	Secondary winding peak current
214	IPEDESTAL_SECONDARY			0.000	A	Secondary winding pedestal current
215	IRMS_SECONDARY			4.729	A	Secondary winding RMS current
216	IRIPPLE_CAP_OUT			3.656	A	Output capacitor ripple current
218	**MAGNETIC FLUX DENSITY**					
219	BPEAK			3636	Gauss	Peak flux density
220	BMAX			2509	Gauss	Maximum flux density
221	BAC			1254	Gauss	AC flux density (0.5 x Peak to Peak)

10 PCB Assembly Instructions

10.1 *Materials*

Item	Description
[1]	Assembled Output Capacitor Bank (PCB and C8, C9, and C10).
[2]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 5 mm Wide.
[3]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 36 mm Wide.
[4]	Teflon Tubing #22.

10.2 *Assembly Instructions*

Output Capacitor Bank taping instructions	
 	Wrap the bottom and sides of the Output Capacitor bank with tape Item [3] to insulate the capacitor form transformer core.

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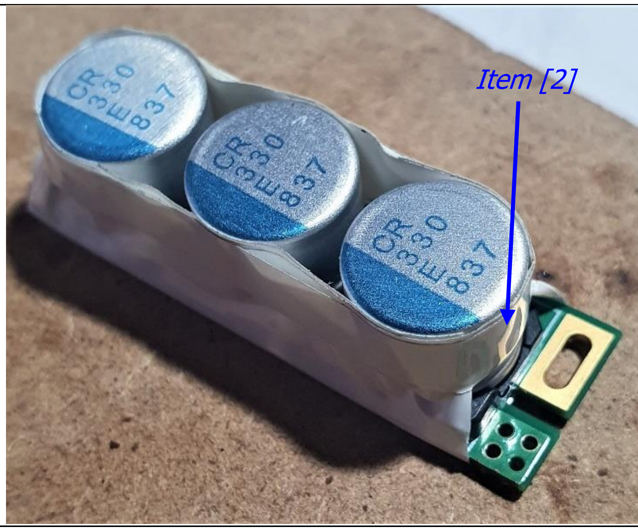
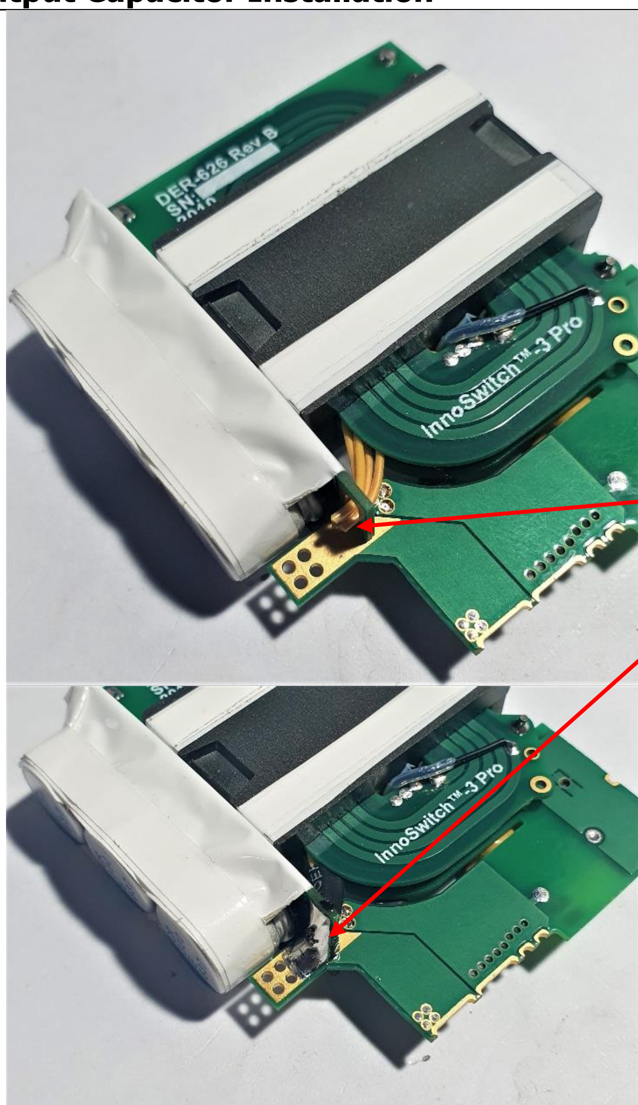
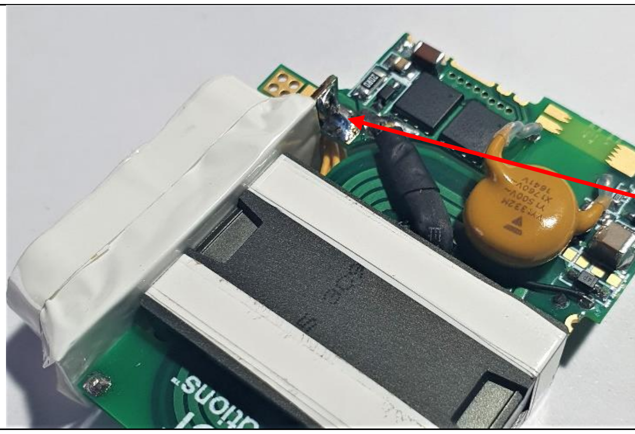
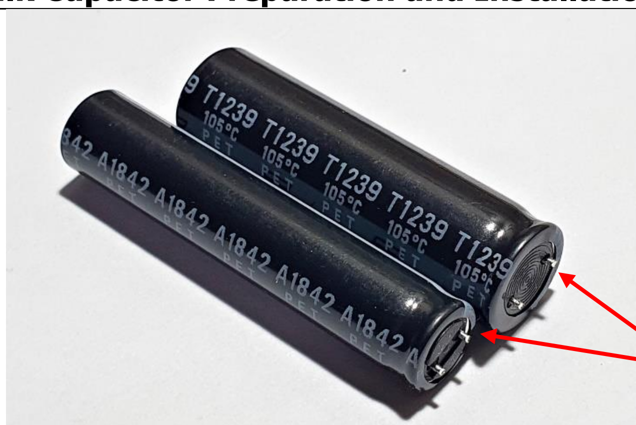
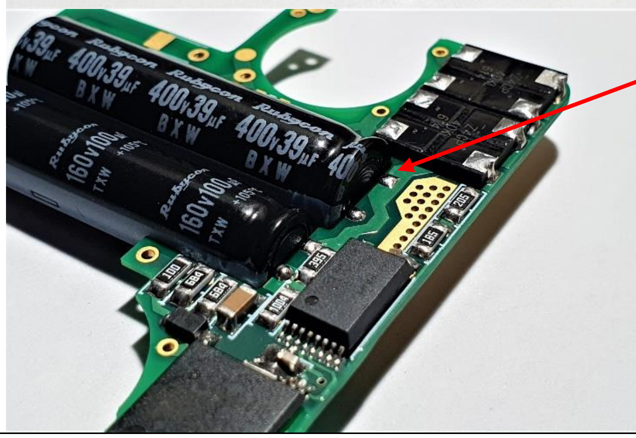
	Use Item [2] to secure the folded tape and complete taping of the capacitor bank.
Output Capacitor Installation	
	Insert FL6 into the slot in the output capacitor bank. Solder FL6 to the slot and the output capacitor board to the secondary board.

	Solder the negative node of the output capacitor bank to the secondary board.
Bulk Capacitor Preparation and Installation	
 	Trim the leads of the bulk capacitors C1 and C2 leaving only 1mm. Insert the bulk capacitor leads into the castellated holes and solder in place.
X-Capacitor Preparation and Installation	

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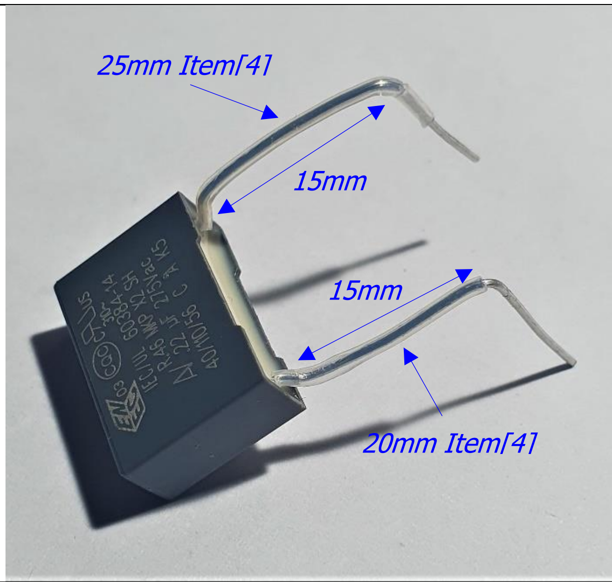
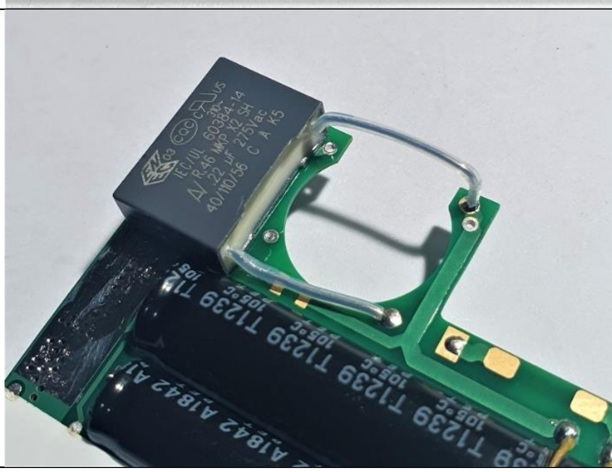
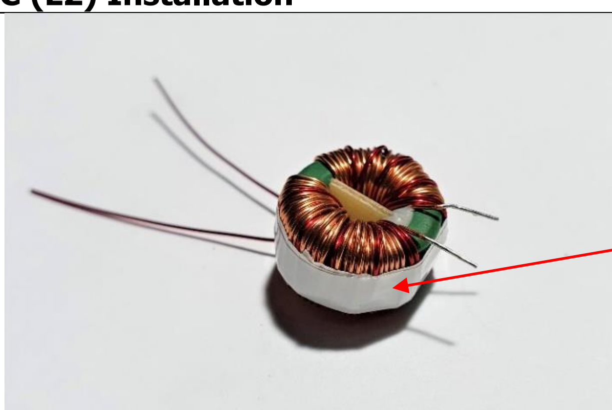
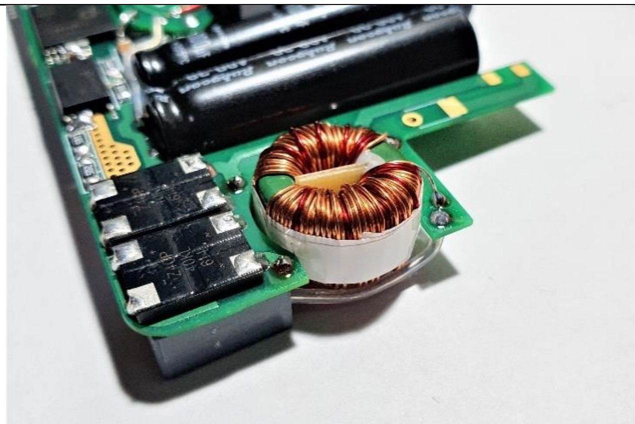
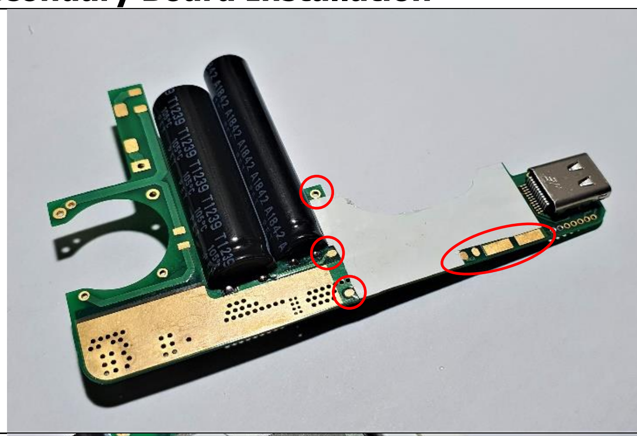
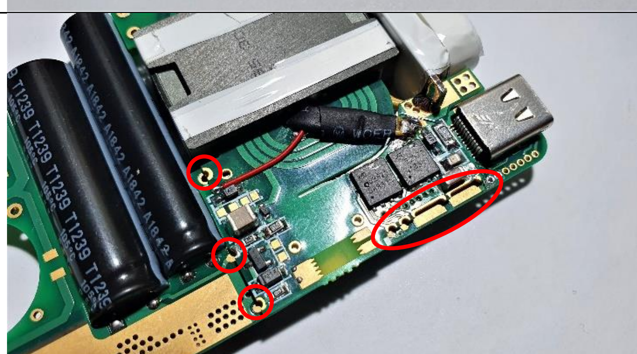
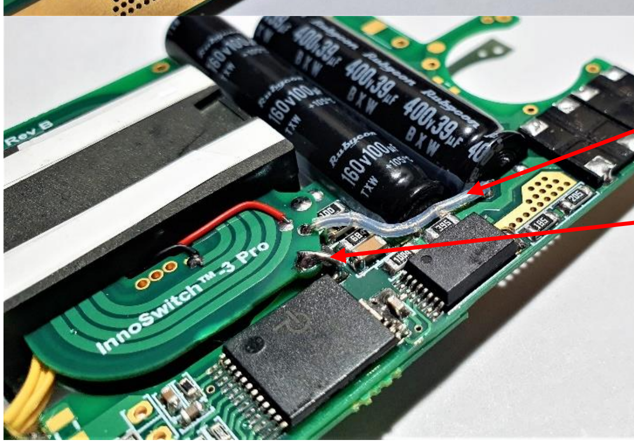
	Use Item [4] to sheath the leads of the X-capacitor C3. Bend the leads of the capacitor as shown.
	Install the X-Capacitor C3 on the main PCB as shown.
CMC (L2) Installation	
	Use Item [2] and tape the perimeter of the CMC.

	Install the CMC as shown and solder in place.
Secondary Board Installation	
	Use 2 layers of Item [3] to insulate the main board from the secondary board as shown. Ensure that the connection points between the 2 PCBs are exposed (marked by red circles)
 	Align the secondary board to the main board using the connection points as guide. Solder connection points together. Use a jumper wire with a Teflon sheath to connect FL11 to the negative node of C1. Connect FL6 to the Drain node of the InnoSwitch3-Pro.

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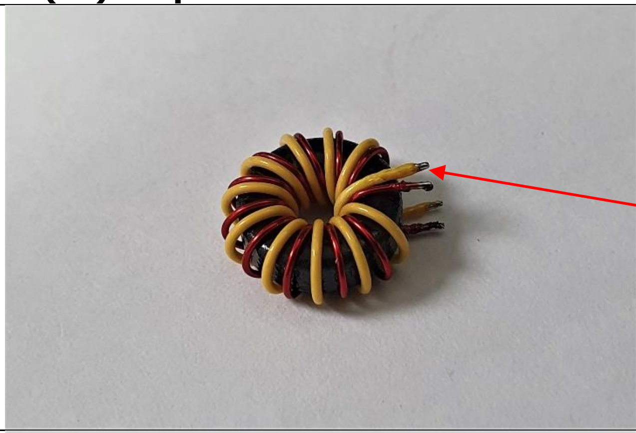
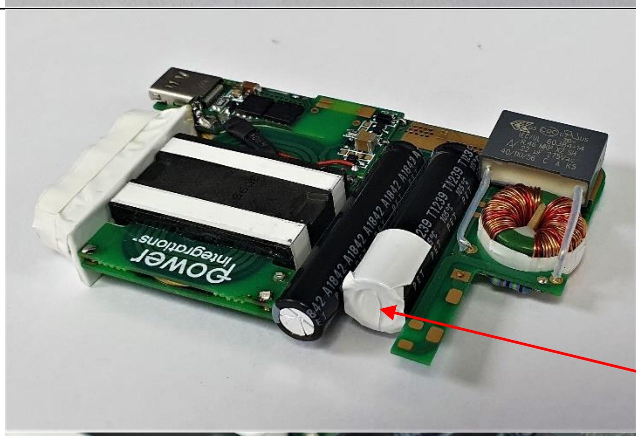
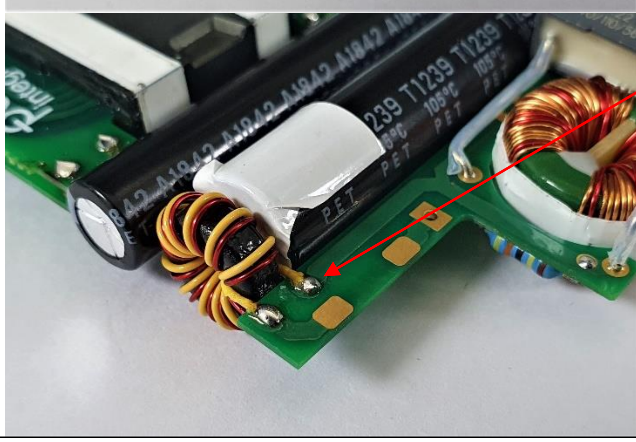
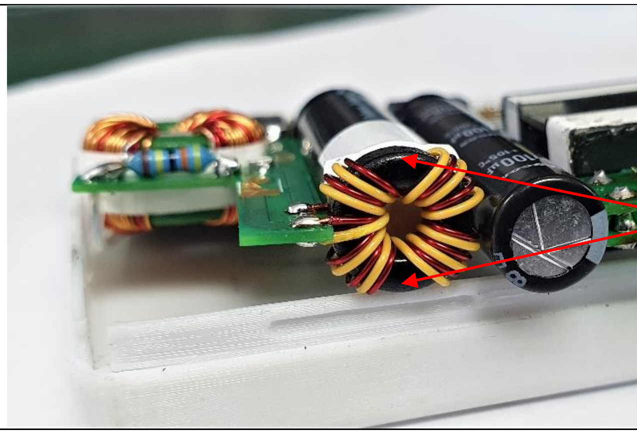
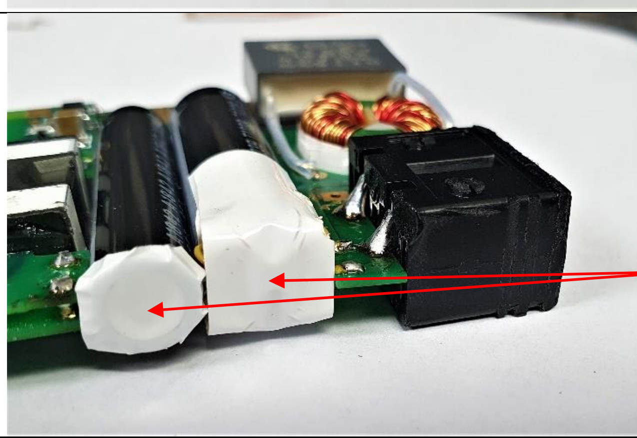
CMC (L1) Preparation and Installation	
	Trim the leads of L1 leaving approximately 2mm. Pre-tin the end of the leads.
 	Use Item [3] to cover the top of the HV Capacitor, C1. Position L1 as shown and solder in place.

	Shove and arrange the windings of L1 to prevent the windings from interfering with the heat spreader.
AC Inlet Preparation and Installation	
 	Bend and trim the leads of the AC Inlet as shown.
	Position and solder the AC inlet in place. Use Item [2] to cover CMC, L1 and the top of C2.

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11 Adapter Case and Heat Spreader Assembly

11.1 *Materials*

Item	Description
[1]	Heat Spreader: Aluminum, 16 mil Thick, PI#: 61-00288-00.
[2]	Insulator: Clear, Mylar Teijin, 2 mil Thick, PI#: 66-00289-00.
[3]	Thermal Pad 1A: PI#: 66-00290-00, (3M, Silicon Pad5519, 2.0 mm Thick, PI#: 66-00377-00).
[4]	Thermal Pad 1B: PI#: 66-00291-00, (3M, Silicon Pad5549s, 1.5 mm Thick, PI#: 66-00231-00).
[5]	Thermal Pad 2A: PI#: 66-00292-00, (3M, Silicon Pad5519, 2.0 mm Thick, PI#: 66-00377-00).
[6]	Thermal Pad 2B: PI#: 66-00293-00, (3M, Silicon Pad5549s, 1.5 mm Thick, PI#: 66-00231-00).
[7]	Thermal Pad 3: Berquist 0.5 mm Thick, PI#: 61-00294-00.
[8]	Thermal Pad 4: Berquist 0.5 mm Thick, PI#: 61-00295-00.
[9]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 21.0 mm Wide.
[10]	Tape: 3M 1298 Polyester Film, 1 mil Thick 6.0 mm Wide.
[11]	Enclosure-Top: PI#: 07-00020-100.
[12]	Enclosure-Bottom: PI#: 07-00021-00.
[13]	AC Inlet Socket: Switchcraft-RAPC322, PI#: 35-00360-00.
[14]	Glue: Loctite-409-Gel, P/N:40904.

11.2 *Adapter Case Dimensions*

Note: Dimensions are in millimeters.

11.2.1 Enclosure Top Half

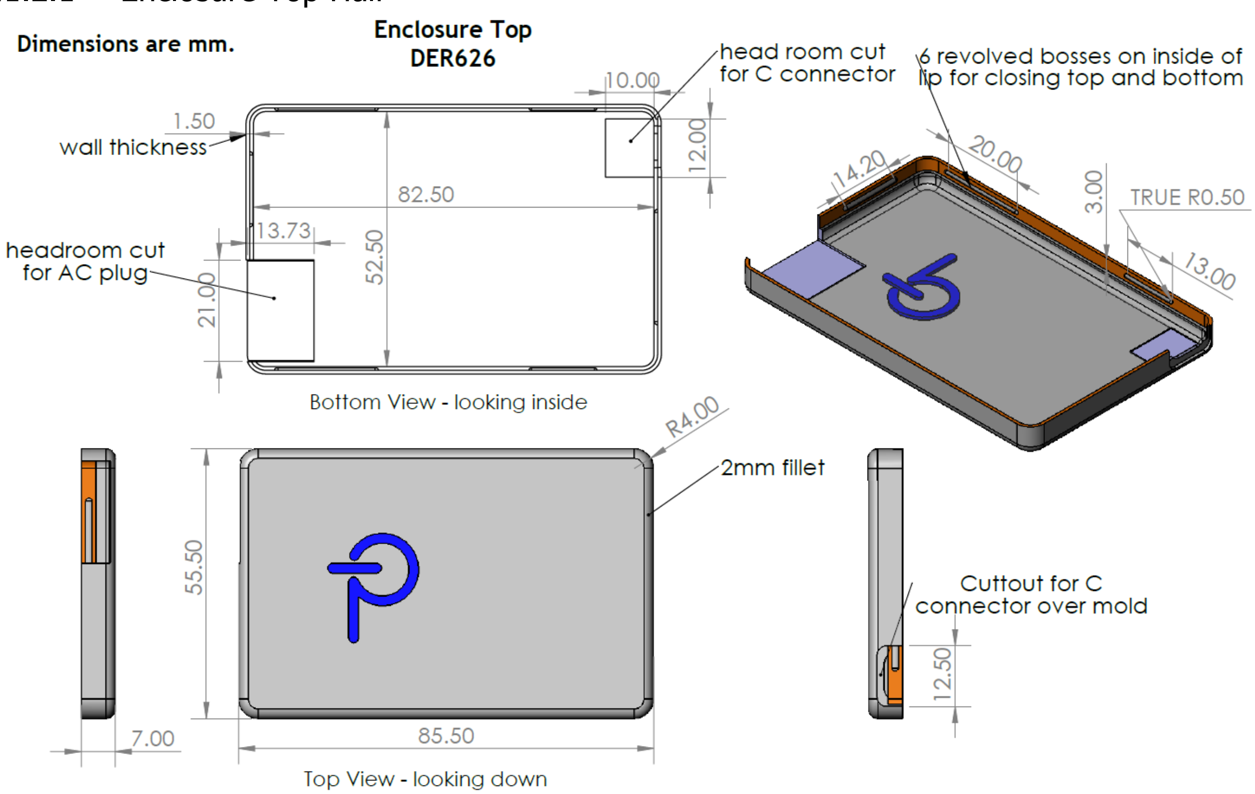

Figure 27 – Enclosure Top Half Dimensions.

Enclosure Bottom Half

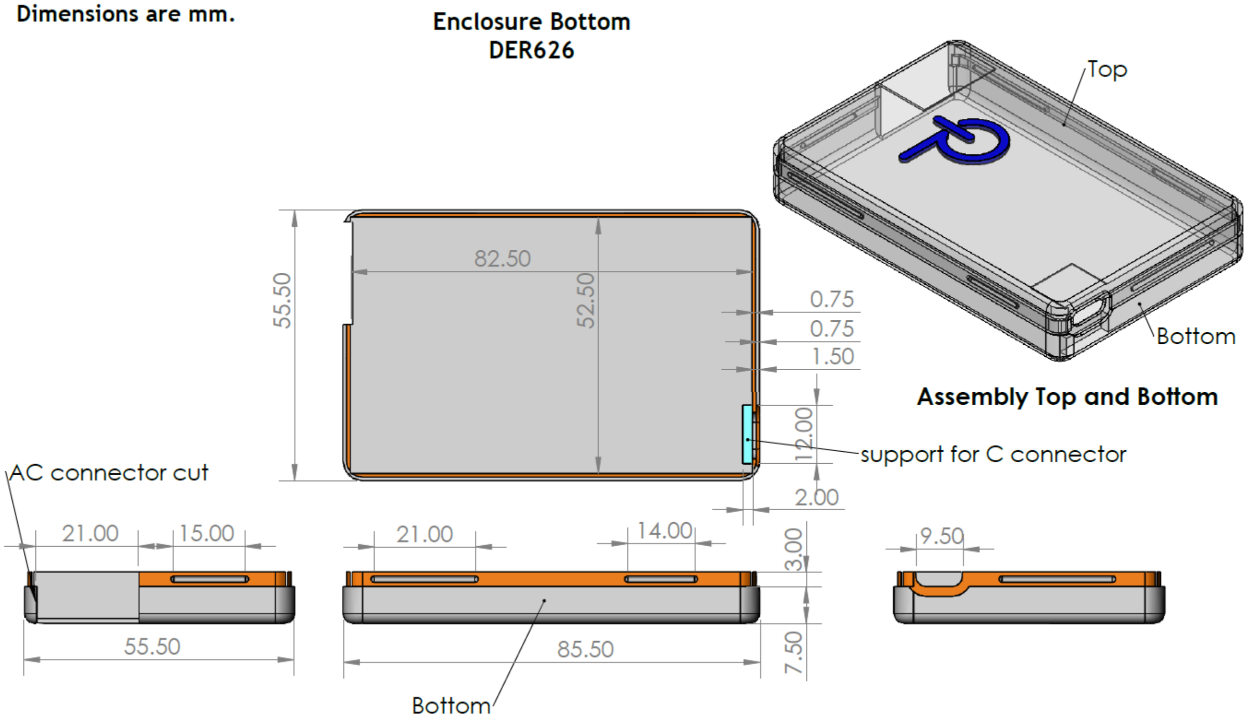

Figure 28 – Enclosure Bottom Half Dimensions.

11.3 *Heat Spreader Dimensions*

Note: Dimensions are in inches.

11.3.1 Aluminum Sheet

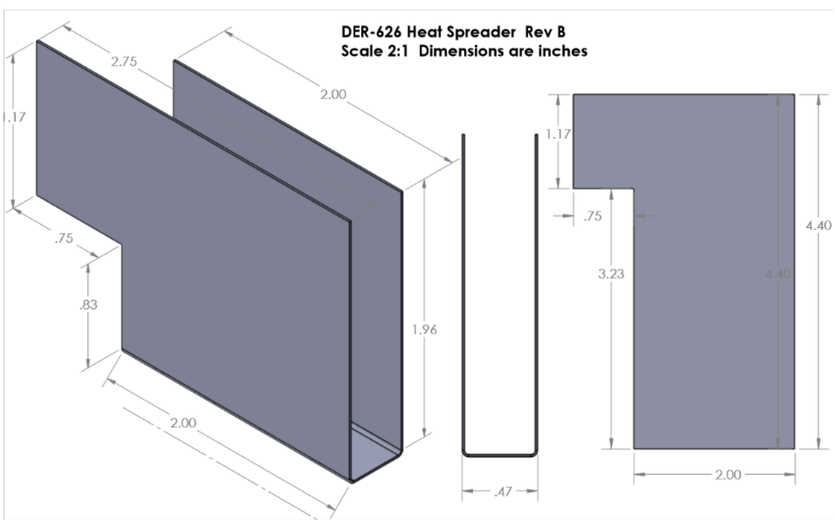

Figure 29 – Aluminum Sheet (25 mils thick) Dimensions.

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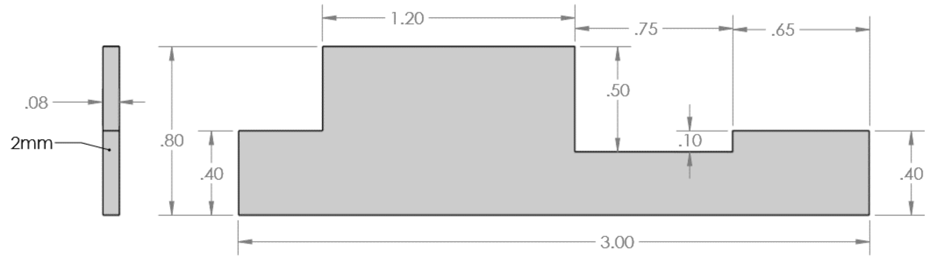
11.3.2 Thermal Pads

Dimensions: inches **Thermal Pad 1 DER 626 Rev B**

Place on PI devices and Bridge



Material:
(1) 3M Silicon Pad 554919 without protective film 2mm thick 66-00377-00. Cut 2.
(2) 3M Silicon Pad 55495 with protective film on top.1.5mm thick 66-00231-00

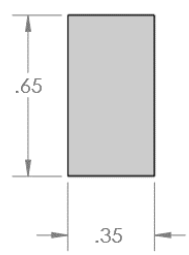
Make 2 thermal pads with material (1) & (2). Then, attach together and place on top of components with material (2) on top.

Figure 30 – Thermal Pad 1 Dimensions.

Dimensions: inches **Thermal Pad 2 DER 626 Rev B**

Put on top of MOSFETs

Material:
(1) 3M Silicon Pad 5519 without protective film 2mm thick 66-00377-00
(2) 3M Silicon Pad 55495 with protective film on top 1.5mm thick 66-00231-00



Note: Make 2 thermal pads with materials (1) and (2). Attach together and place on top of components with material (2) on top.

Figure 31 – Thermal Pad 2 Dimensions.

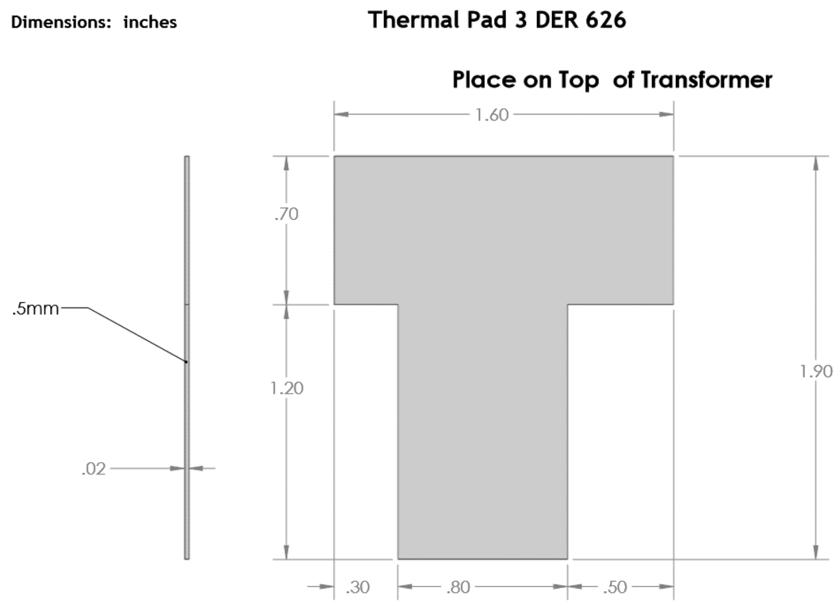


Figure 32 – Thermal Pad 3 Dimensions.

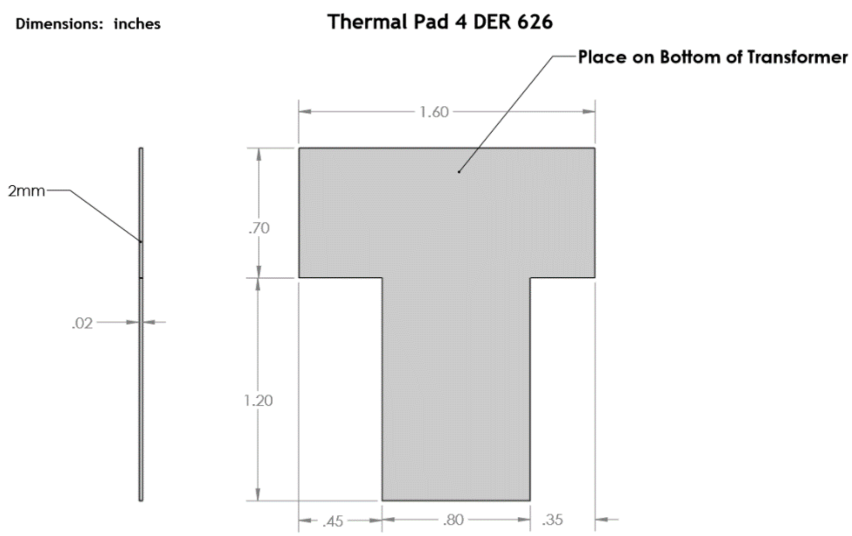


Figure 33 – Thermal Pad 4 Dimensions.

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11.3.3 Mylar Insulator

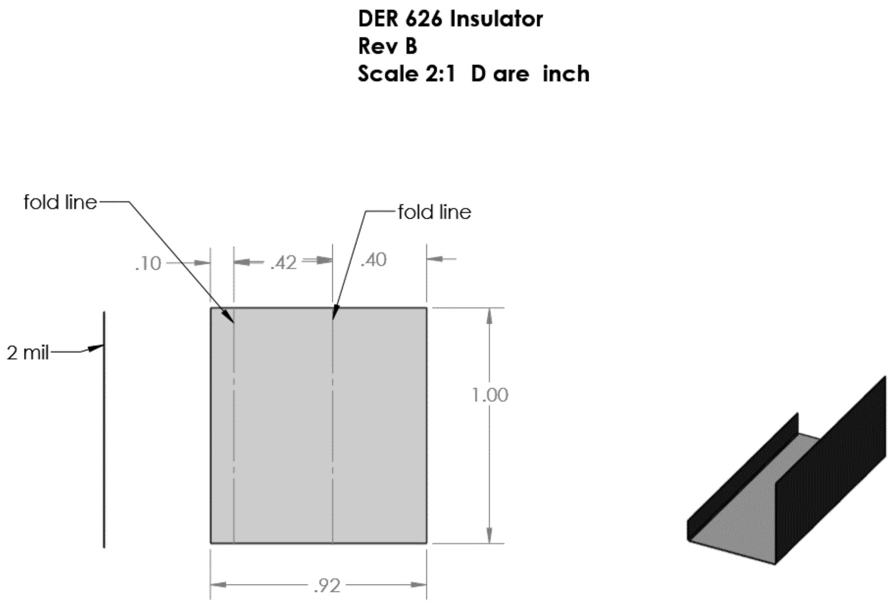
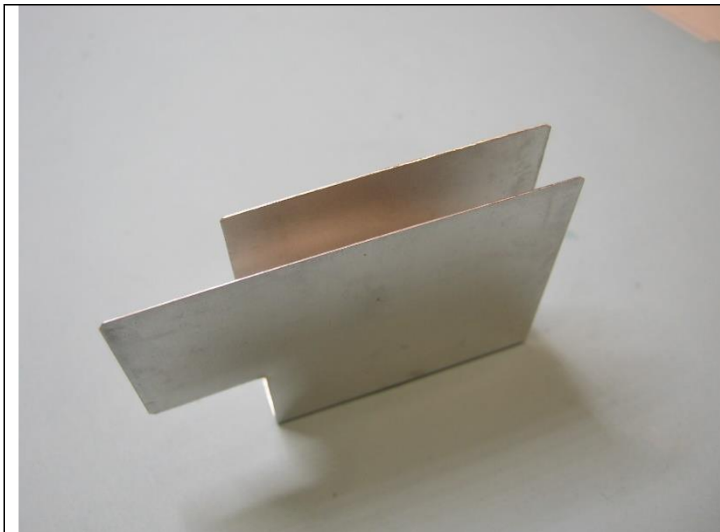
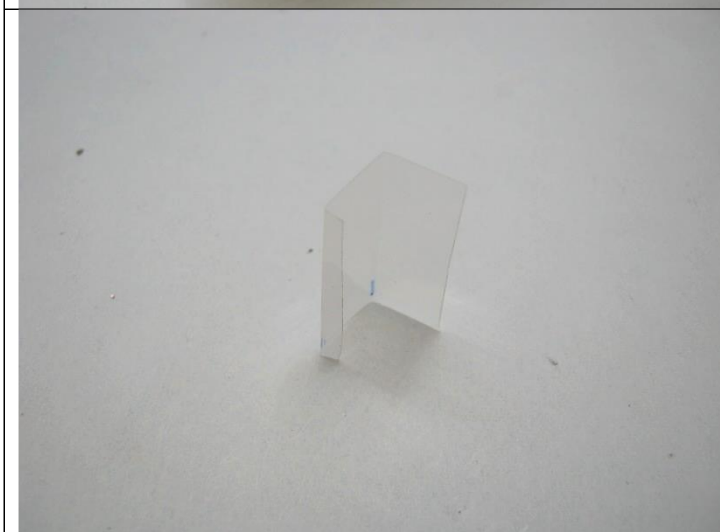
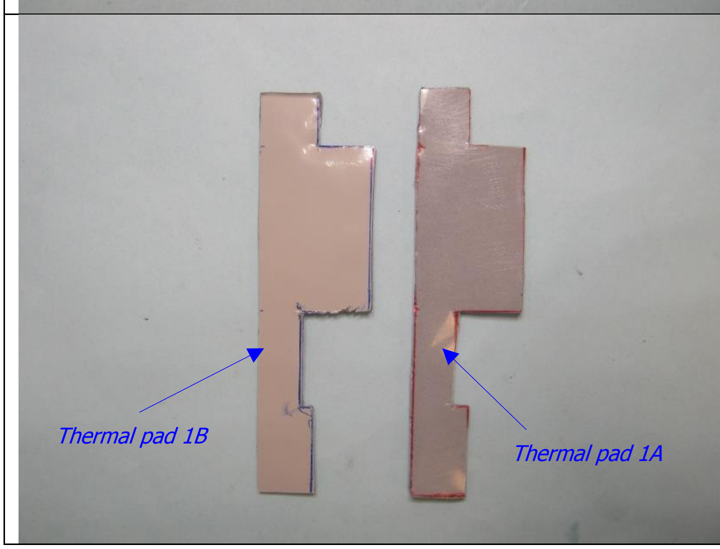


Figure 34 – Mylar Insulator Dimensions.

11.4 *Assembly Illustrations*

	Prepare heat spreader Item [1].
	Prepare insulator Item [2].
	Prepare thermal pad 1A Item [3] and thermal pad 1B Item [4].

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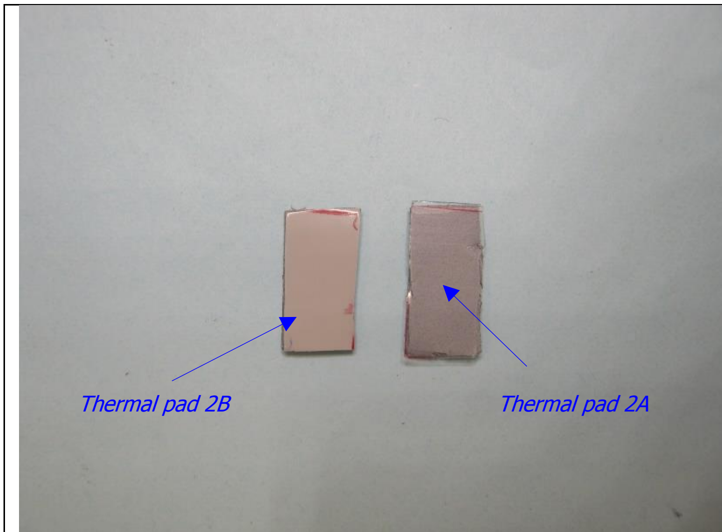
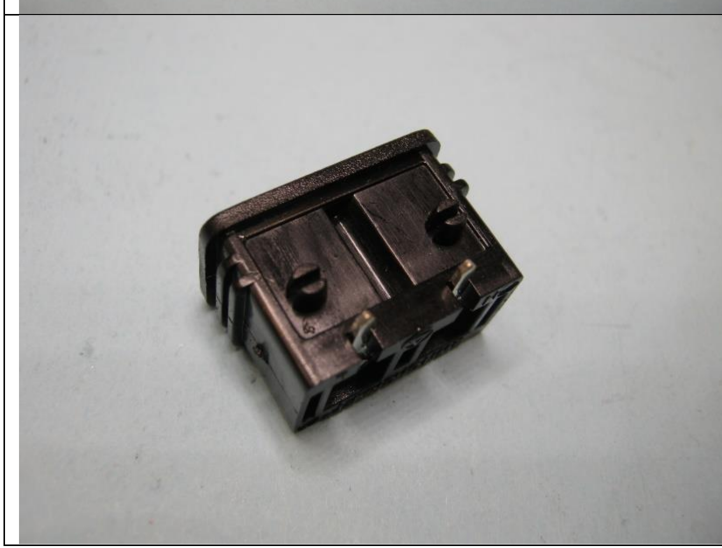
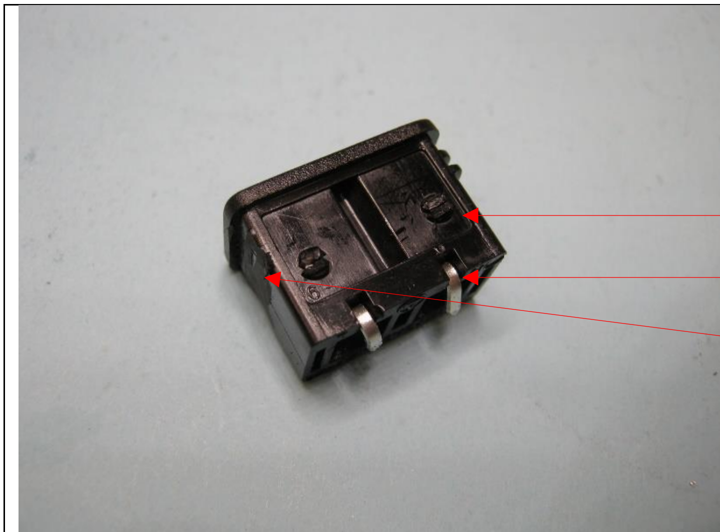
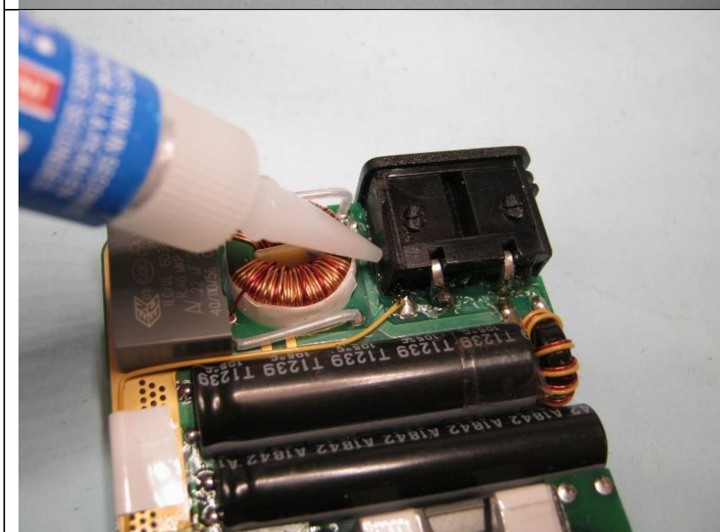
	Prepare thermal pad 2A Item [5] and thermal pad 2B Item [6].
	Prepare 2 thermal pads Item [7] and Item [8].
	AC inlet socket item[13]

	Cut short 2 notches on top. Bend down 2 pins. Trim flush the grooves on left side.
	Solder 2 pins just bent to PCB. Apply glue Item [14] the AC inlet socket to edges of PCB to hold it in place.
	Place thermal pad Item [7] on top of transformer and bulk capacitors.

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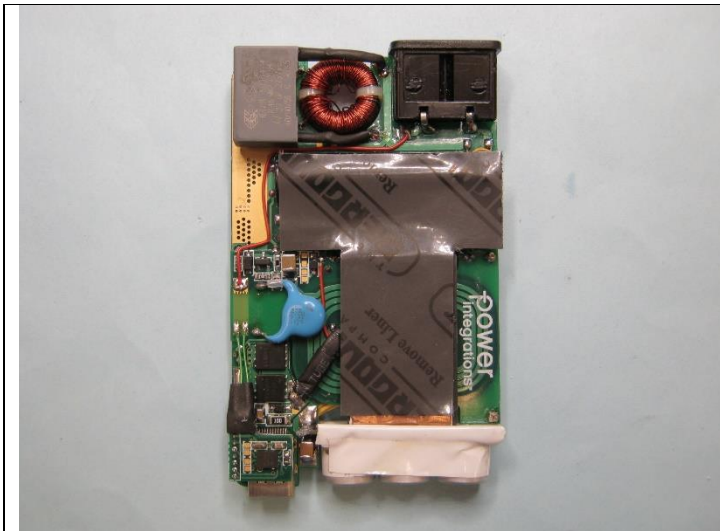
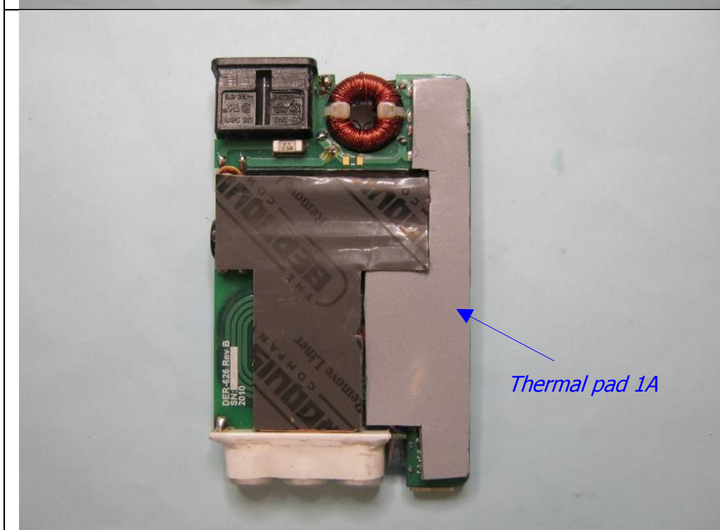
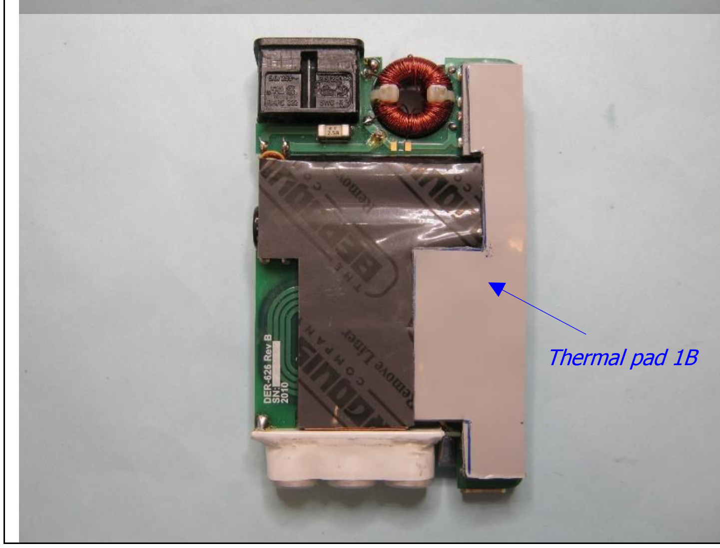
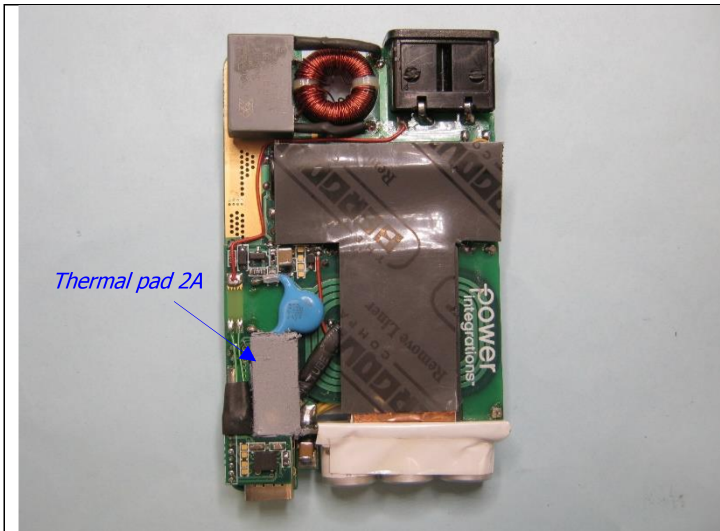
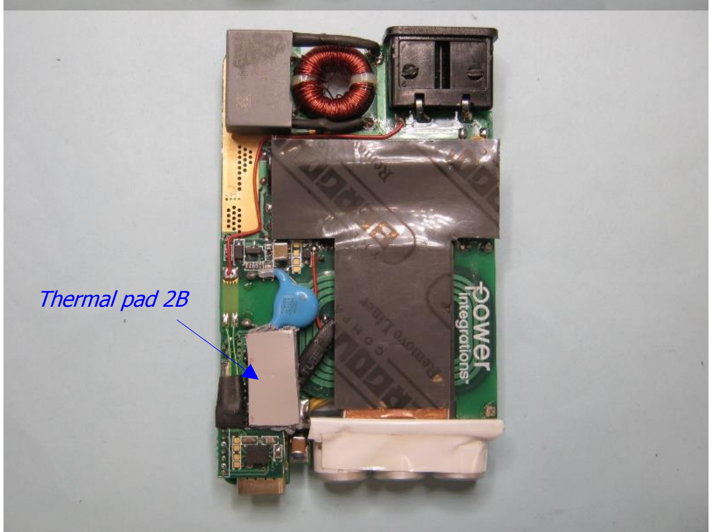
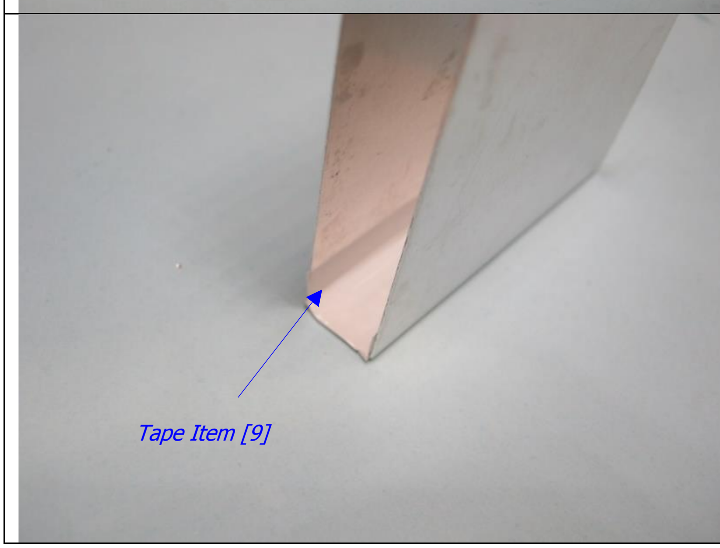
	And thermal pad Item [8] on bottom of transformer and bulk capacitors.
 	Remove plastic covers on both side of thermal pad 1A Item [3] and place on PI devices & bridges. Remove plastic cover of thermal pad 1B Item [4] and place on top of thermal pad 1A which protective film is faced up, see pictures beside.





Do the same step above, place thermal pad 2A Item [5] on top 2 Mosfets, and place thermal pad 2B Item [6] on top of thermal pad as shown in pictures beside.



Now place 1 piece of tape Item [9] inner side of heat spreader Item [1].

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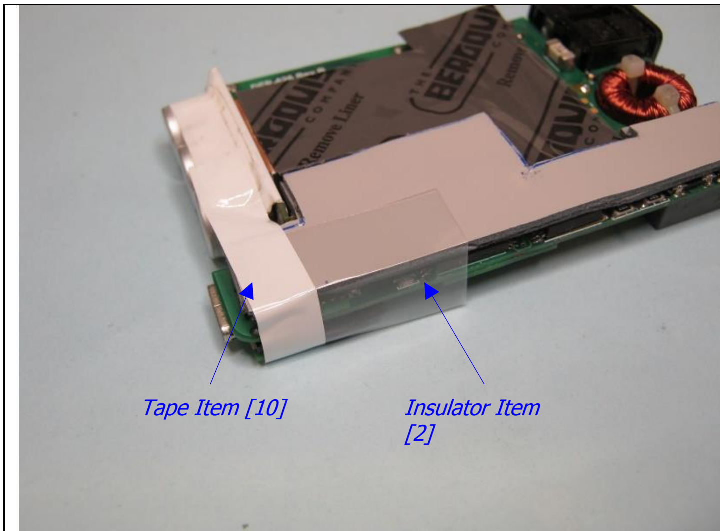
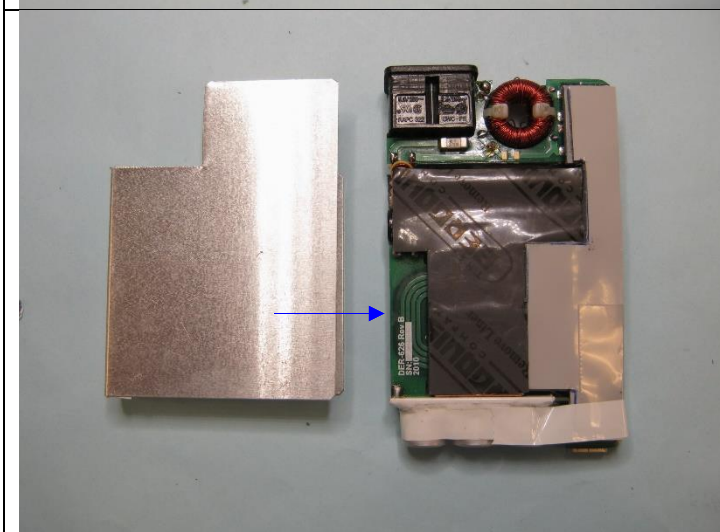
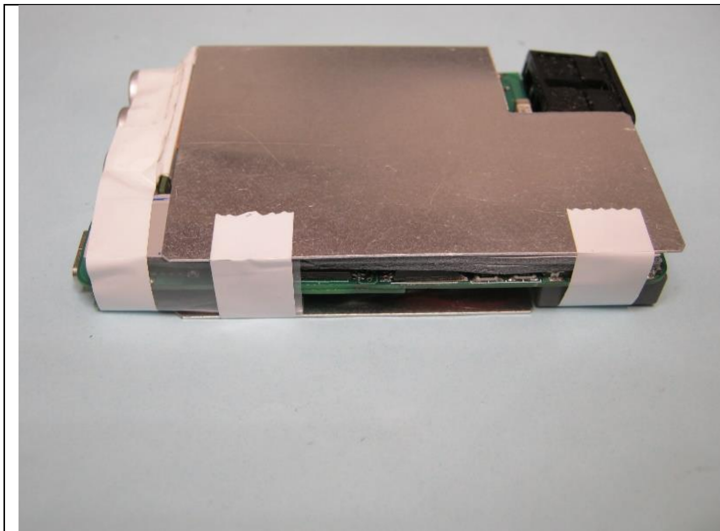
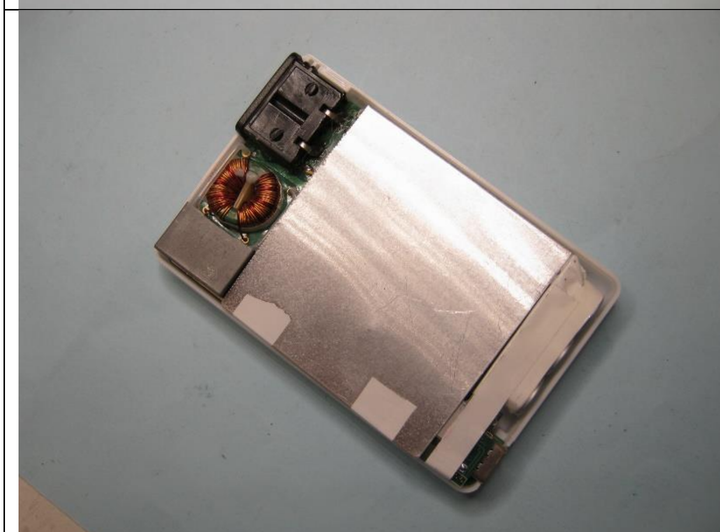
	Use tape Item [10], tape insulator Item [2] to cover a portion-secondary side PCB and surround the Polymer capacitors.
 	Place heat spreader Item [1] and PCB-assembly side by side as shown. Insert heat spreader with direction of arrow. And tape to the side of heat spreader.

	
	Now place whole assembly onto bottom of case Item [12] and snap with top of the case Item [11].
	

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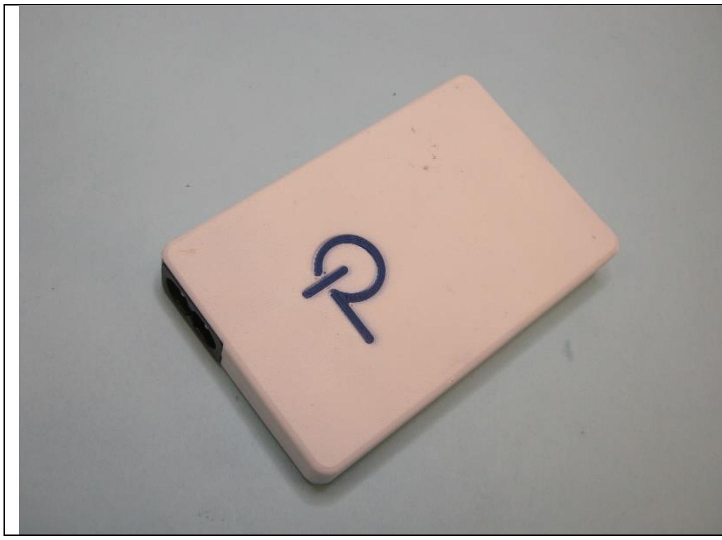

12 Performance Data

Note 1: Output voltages measured on the PCB end.
2: Measurements taken at room temperature (approximately 24 °C).
3: To further minimize No-Load Input Power, a CAPZero IC is recommended to discharge X-capacitor, C3.

12.1 *No-Load Input Power at 5 V_{OUT}*

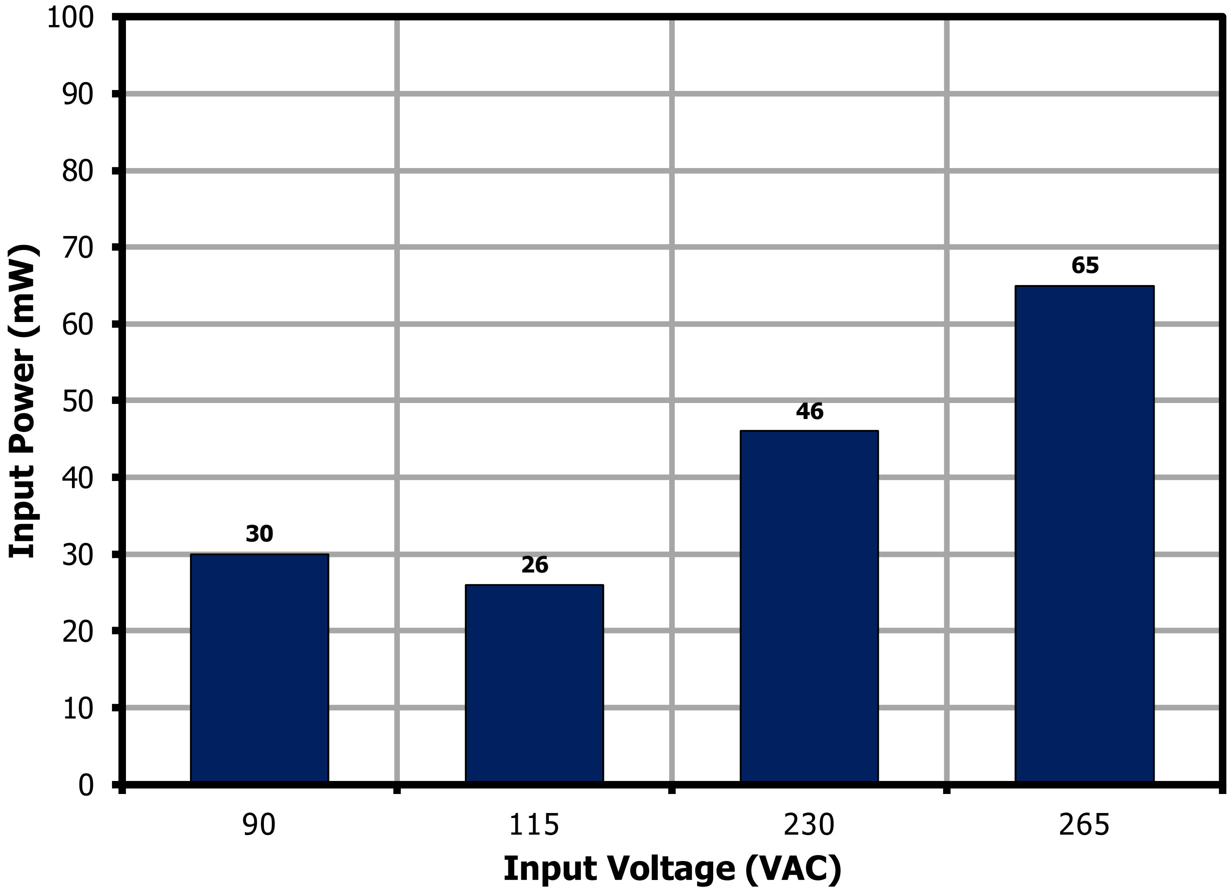

Figure 35 – No-Load Input Power vs. Input Line Voltage.

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12.2 *Average and 10% Load Efficiency*

12.2.1 Efficiency Requirements

		Test Effective	Average 2016	Average Jan-16	10% Load Jan-16
V_{OUT} (V)	Model	Power (W)	New EISA2007	CoC v5 Tier 2	CoC v5 Tier 2
5	<6 V	15	81.4%	81.8%	72.5%
9	>6 V	27	86.6%	87.3%	77.3%
15	>6 V	45	88.0%	88.9%	78.9%
20	>6 V	60	88.0%	89.0%	79.0%

12.2.2 Efficiency Performance Summary (On Board)

V_{OUT} (V)	Power (W)	Average Efficiency (%)		10% Load Efficiency (%)	
		115 VAC	230 VAC	115 VAC	230 VAC
5	15	90.46	87.47	85.46	80.10
9	27	90.68	89.31	85.55	81.37
15	45	90.57	90.29	85.41	82.02
20	65	90.25	90.75	85.63	82.90

12.2.3 Average and 10% Load Efficiency at 115 VAC

12.2.3.1 Output: 5 V / 3 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	15.17	91.11	**90.46**
75	11.42	91.02	
50	7.62	90.52	
25	3.81	88.82	
10	1.53	**85.46**	

12.2.3.2 Output: 9 V / 3 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	27.13	91.20	**90.68**
75	20.38	90.86	
50	13.61	91.20	
25	6.81	89.47	
10	2.73	**88.55**	

12.2.3.3 Output: 15 V / 3 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	44.99	90.98	**90.57**
75	33.77	90.79	
50	22.53	90.88	
25	11.27	89.64	
10	4.51	**85.41**	

12.2.3.4 Output: 20 V / 3.25 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	64.75	89.98	**90.25**
75	48.60	90.59	
50	32.42	90.63	
25	16.22	89.79	
10	6.49	**85.63**	

12.2.4 Average and 10% Load Efficiency at 230 VAC

12.2.4.1 Output: 5 V / 3 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	15.22	89.52	**87.47**
75	11.43	88.88	
50	7.63	87.30	
25	3.82	84.19	
10	1.53	**80.10**	

12.2.4.2 Output: 9 V / 3 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	27.2	91.02	**89.31**
75	20.42	90.49	
50	13.62	89.41	
25	6.81	86.31	
10	2.73	**81.37**	

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12.2.4.3 Output: 15 V / 3 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	45.03	91.72	**90.29**
75	33.81	91.29	
50	22.55	90.47	
25	11.28	87.67	
10	4.51	**82.02**	

12.2.4.4 Output: 20 V / 3.25 A

Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	64.84	91.69	**90.75**
75	48.65	91.60	
50	32.45	90.89	
25	16.23	88.56	
10	6.49	**82.90**	

12.3 *Efficiency Across Load (On Board)*

12.3.1 Output: 5 V / 3 A

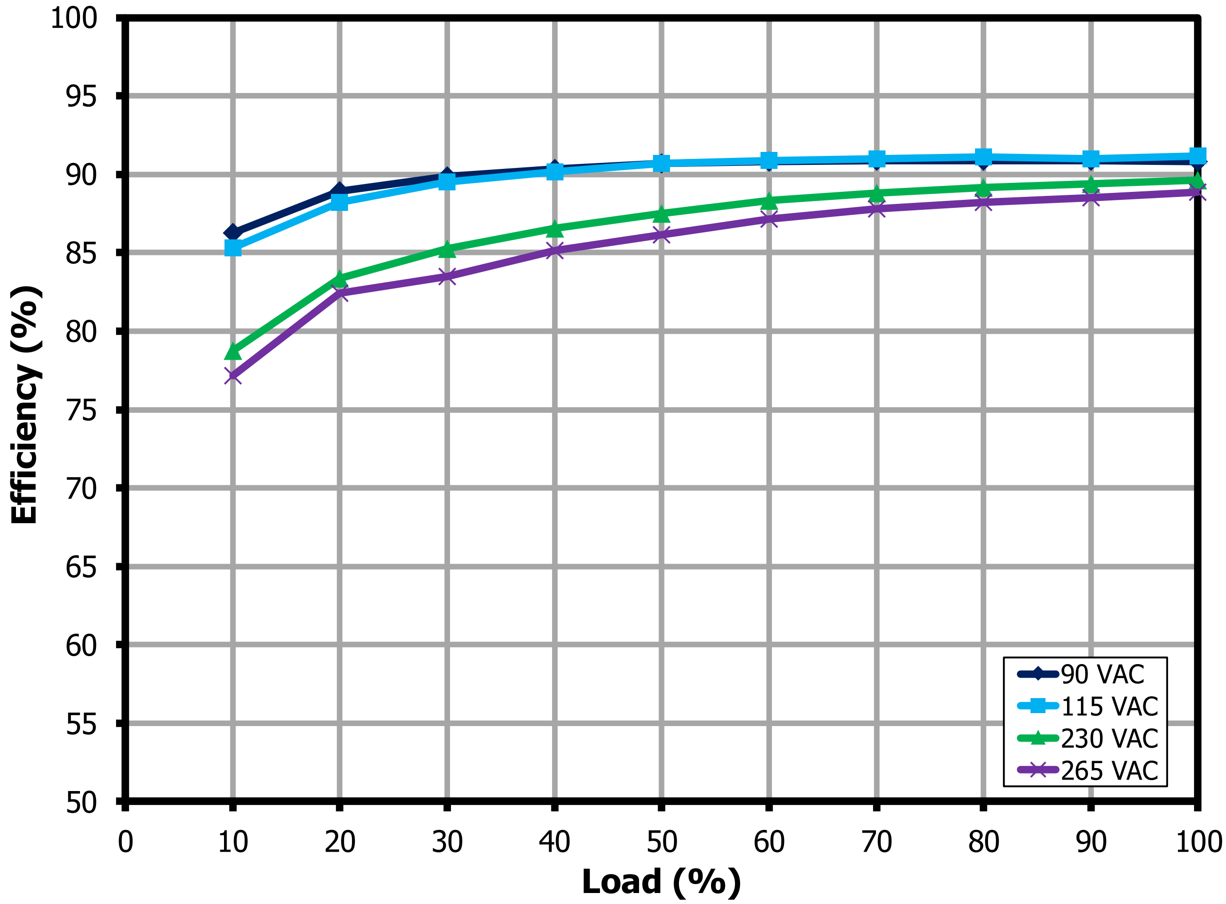

Figure 36 – Efficiency vs. Load for 5 V Output, Room Temperature.

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12.3.2 Output: 9 V / 3 A

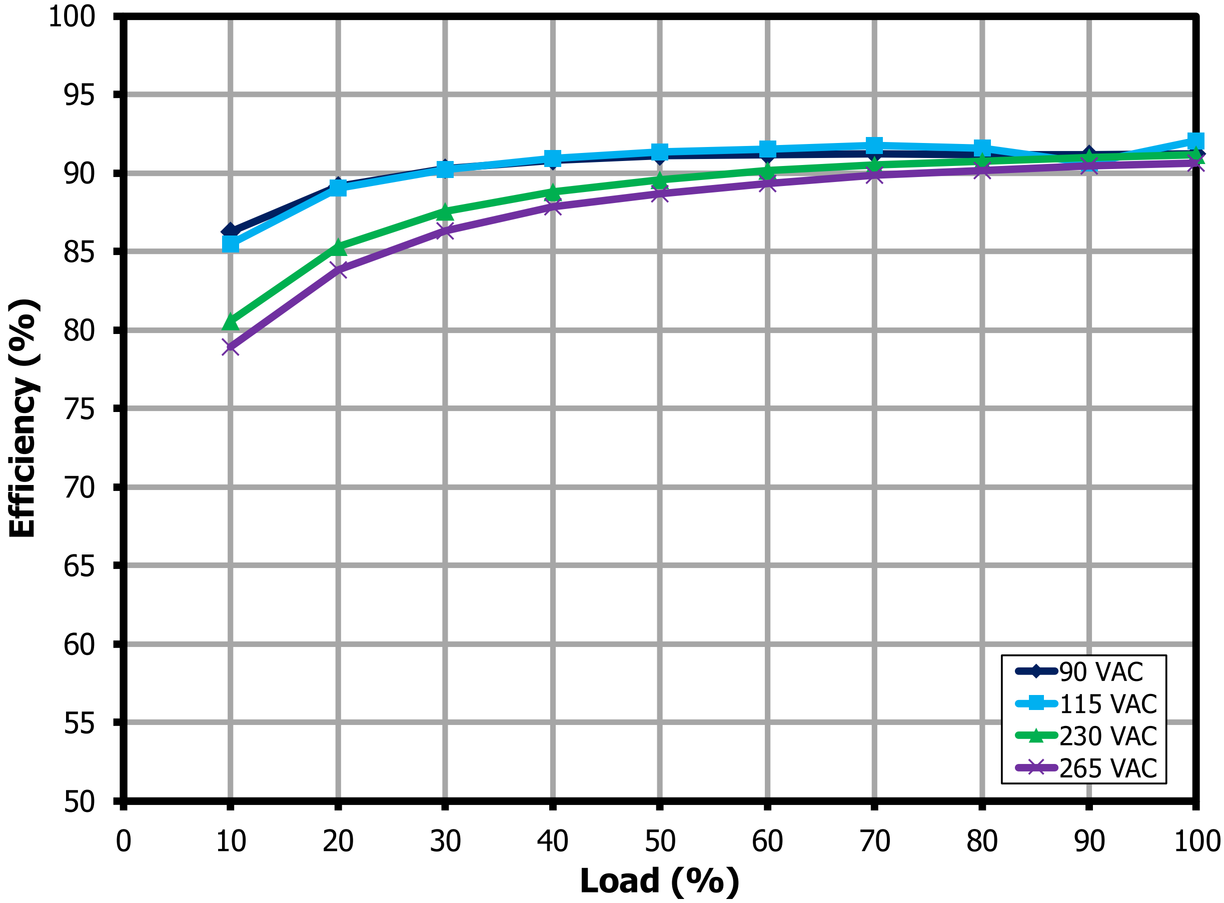

Figure 37 – Efficiency vs. Load for 9 V Output, Room Temperature.

12.3.3 Output: 15 V / 3 A

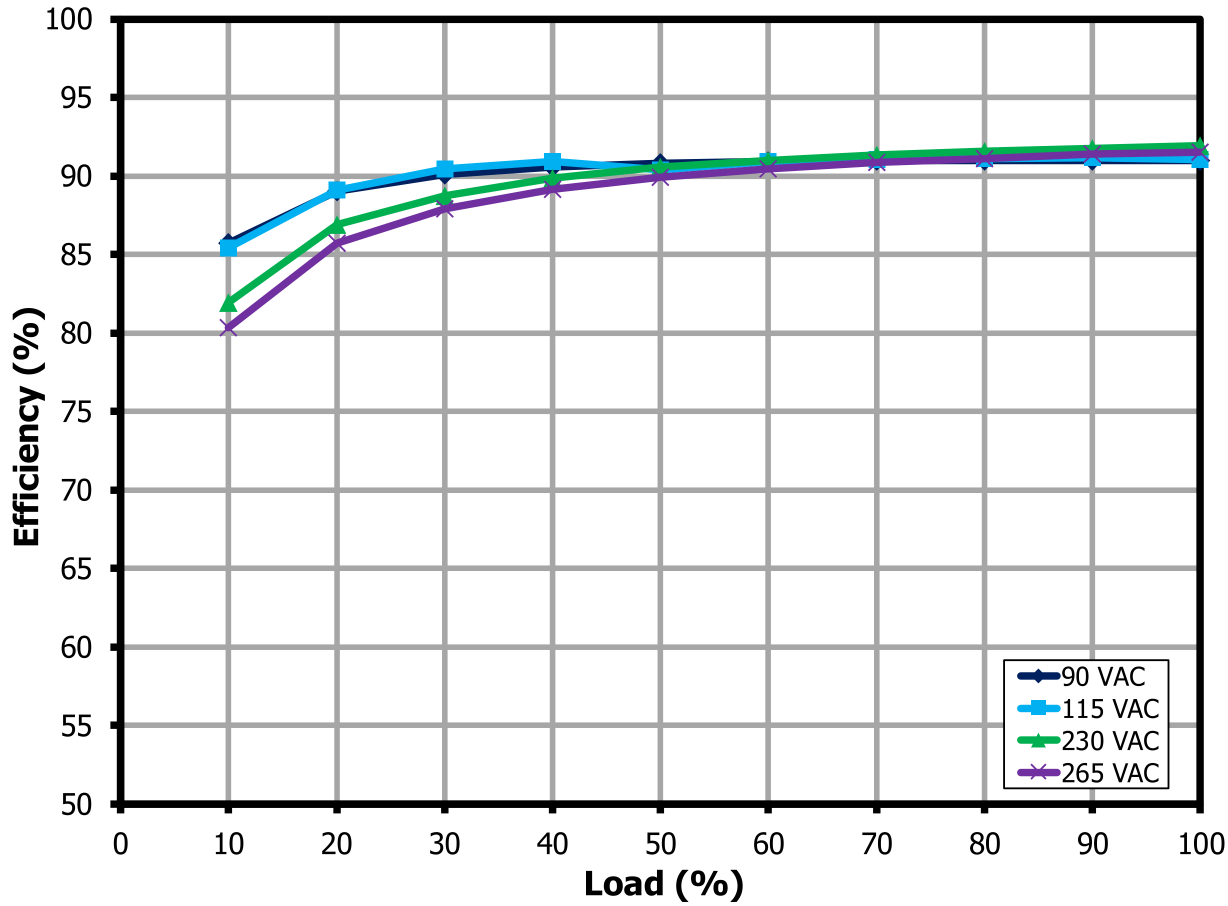

Figure 38 – Efficiency vs. Load for 15 V Output, Room Temperature.

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12.3.4 Output: 20 V / 3.25 A

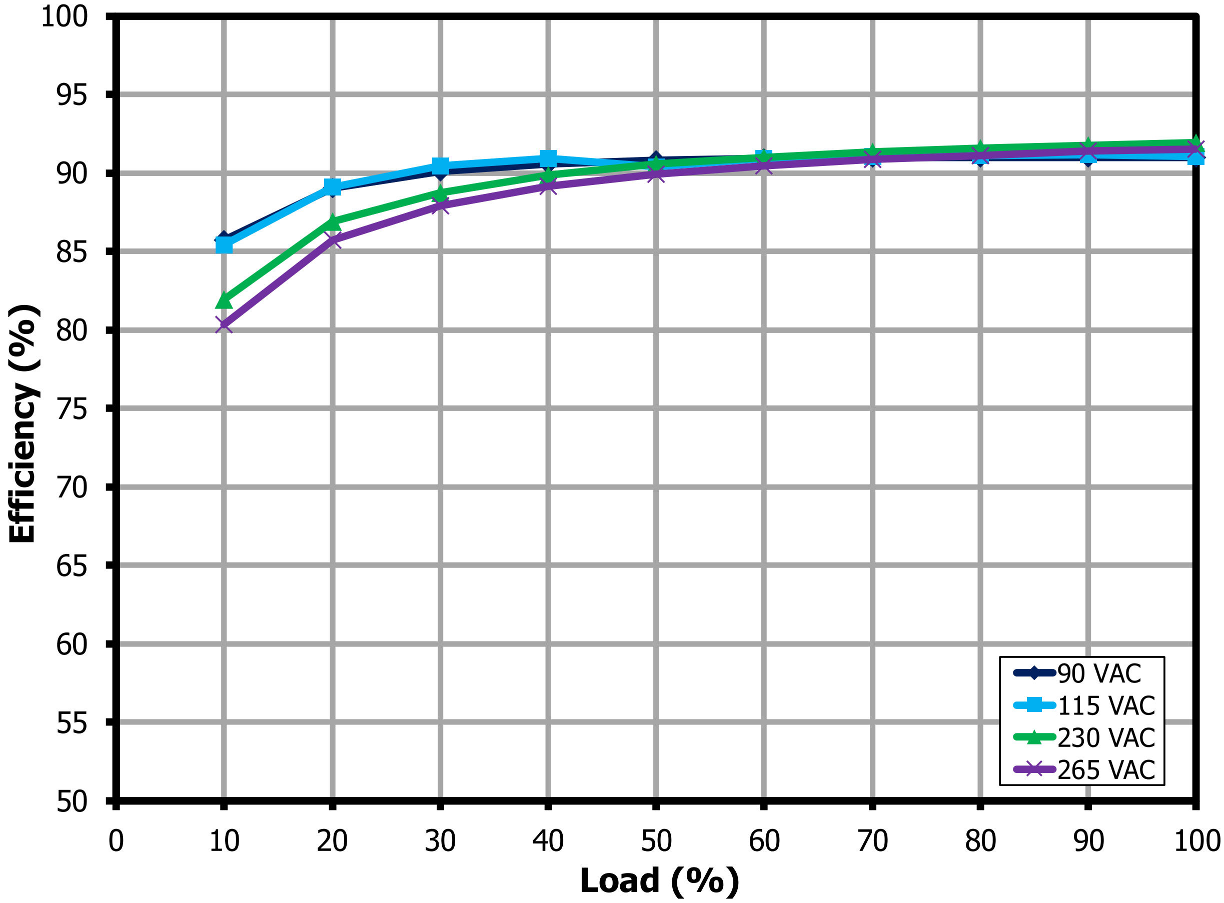

Figure 39 – Efficiency vs. Load for 20 V Output, Room Temperature.

12.4 *Efficiency Across Line (On Board)*

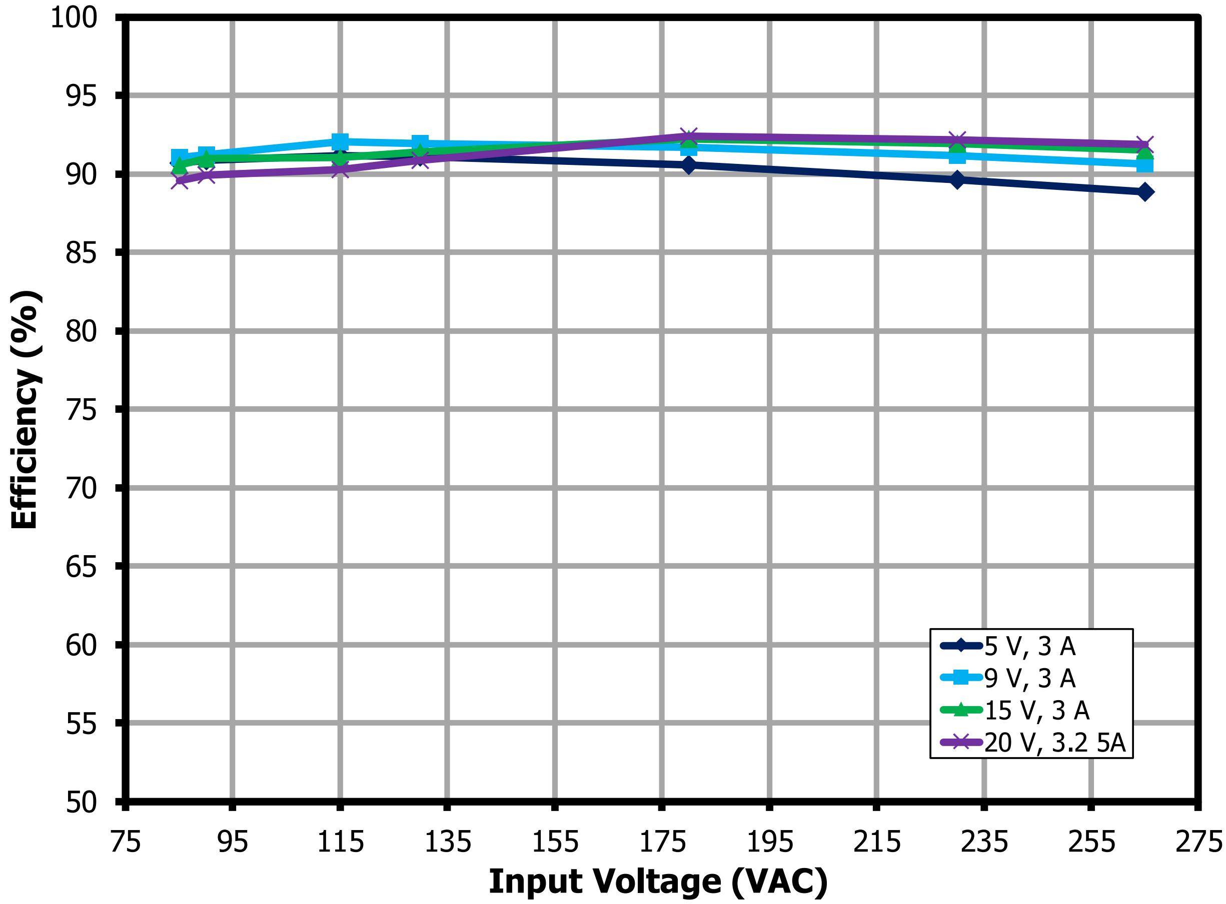

Figure 40 – Full Load Efficiency vs. Input Line for 5 V, 9 V, 15 V, and 20 V Output, Room Temperature.

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12.5 ***Load Regulation (On Board)***

12.5.1 Output: 5 V / 3 A

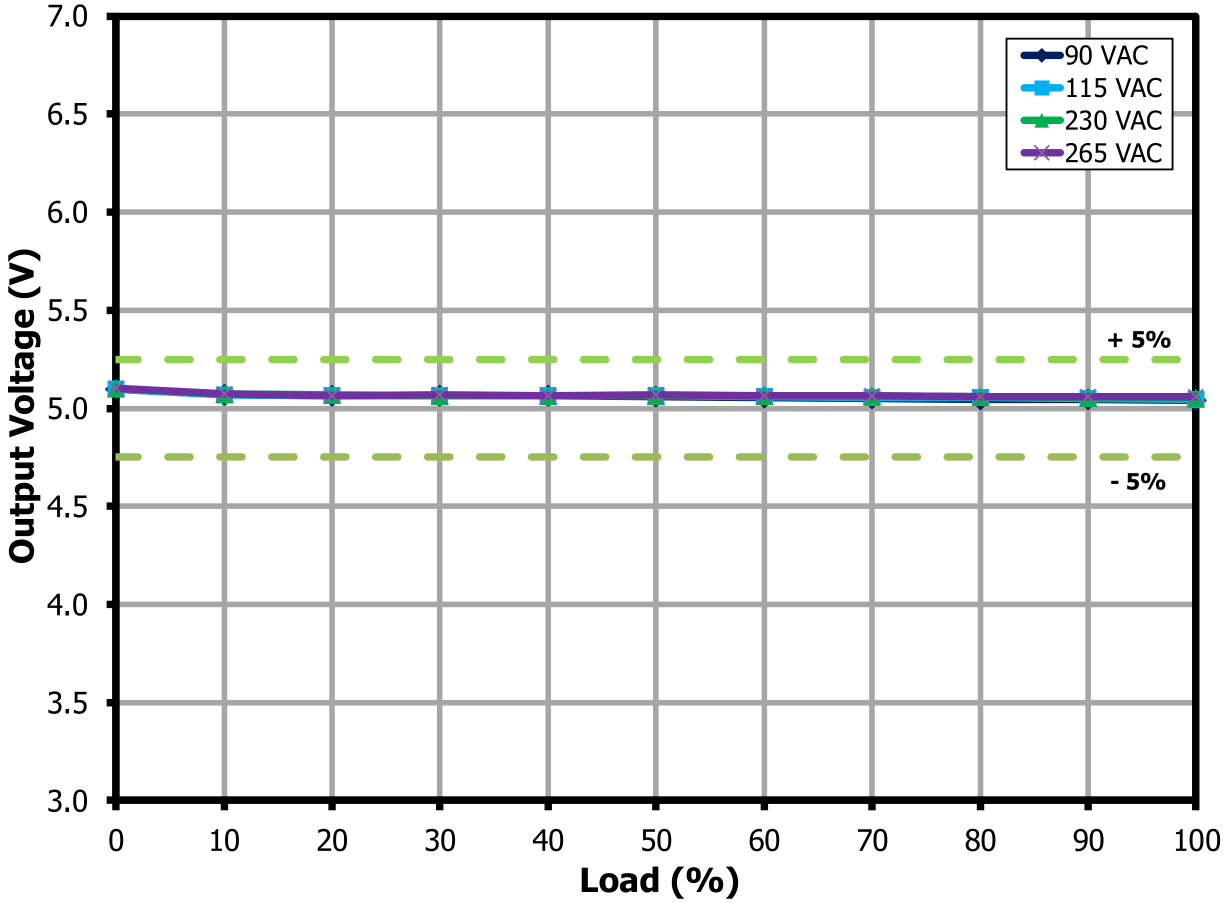

Figure 41 – Output Voltage vs. Output Load for 5 V Output, Room Temperature.

12.5.2 Output: 9 V / 3 A

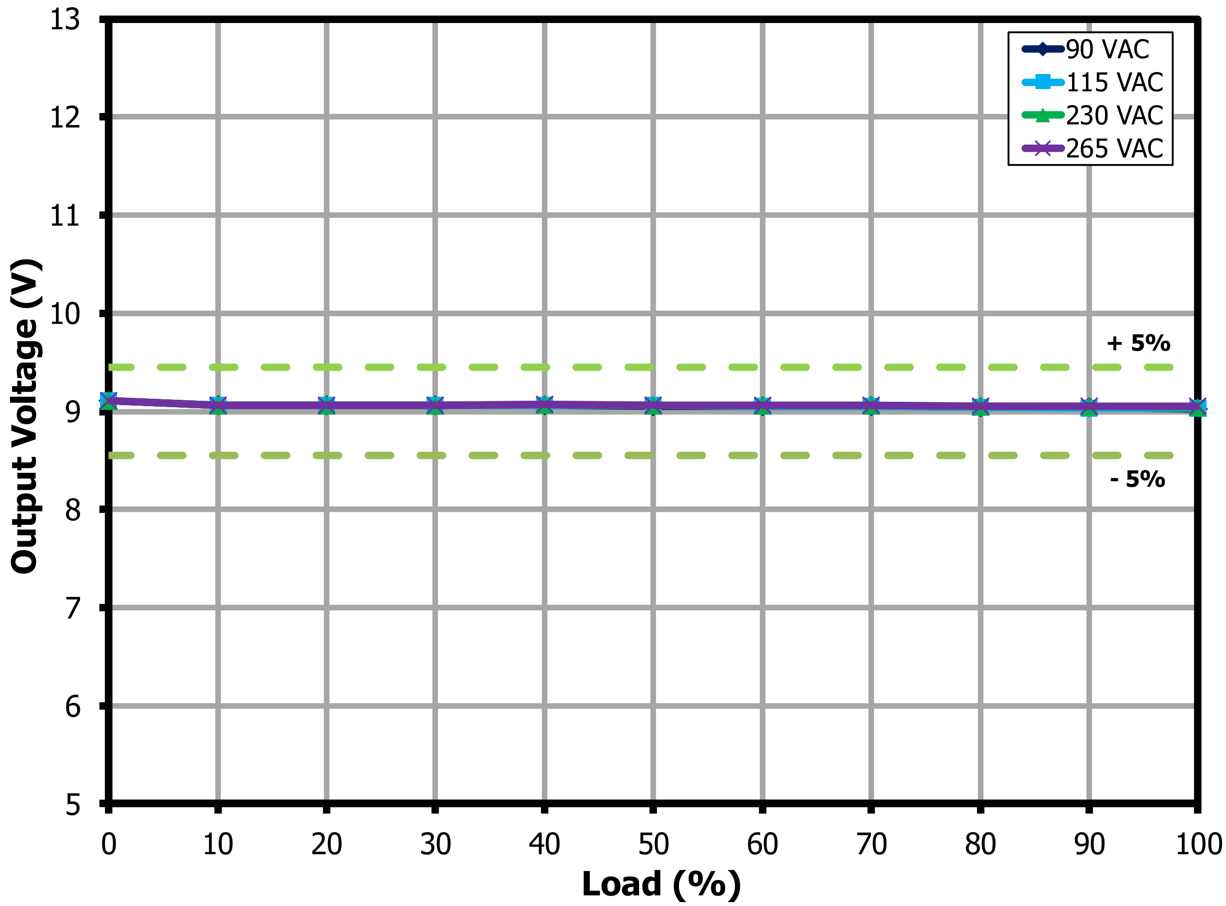

Figure 42 – Output Voltage vs. Output Load for 9 V Output, Room Temperature.

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12.5.3 12.5.3 Output: 15 V / 3 A

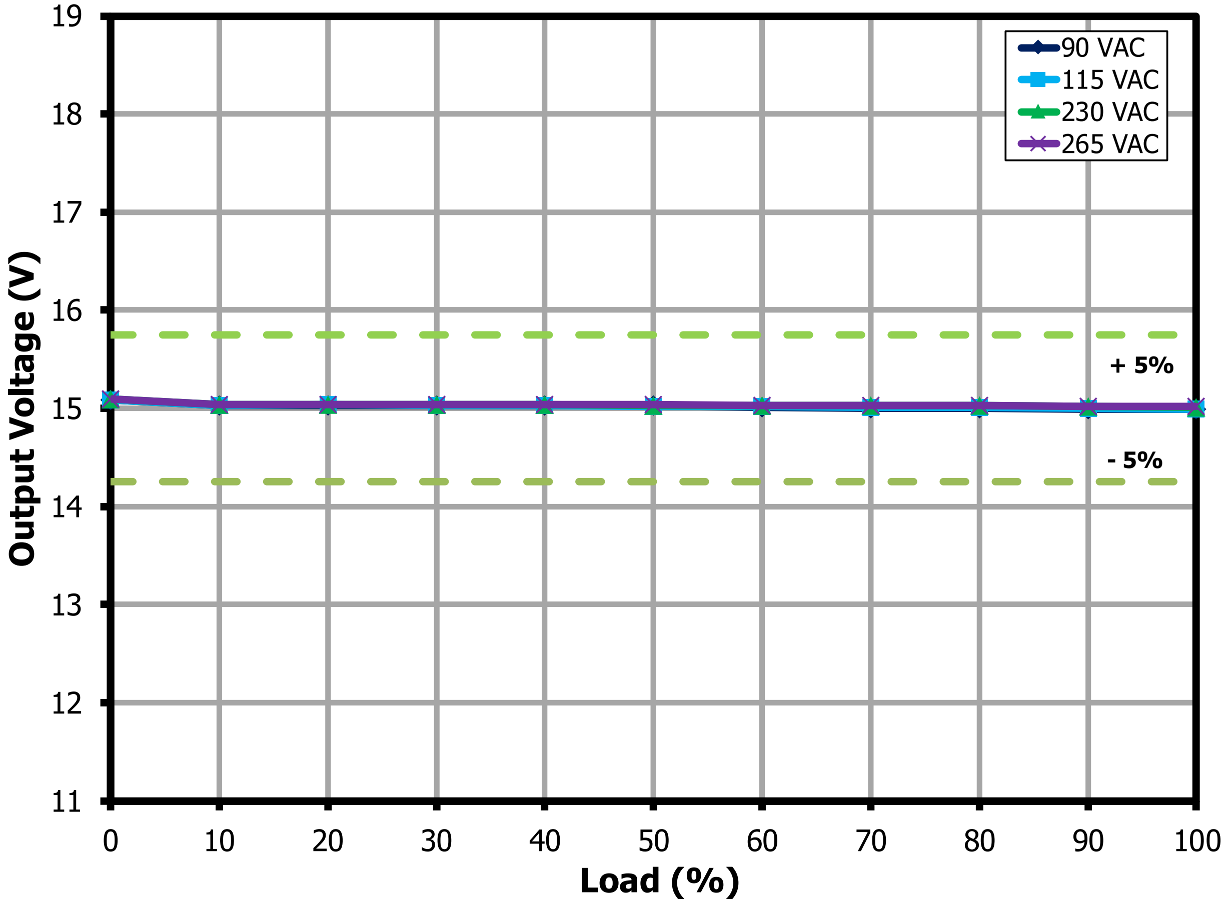

Figure 43 – Output Voltage vs. Output Load for 15 V Output, Room Temperature.

12.5.4 12.5.4 Output: 20 V / 3.25 A

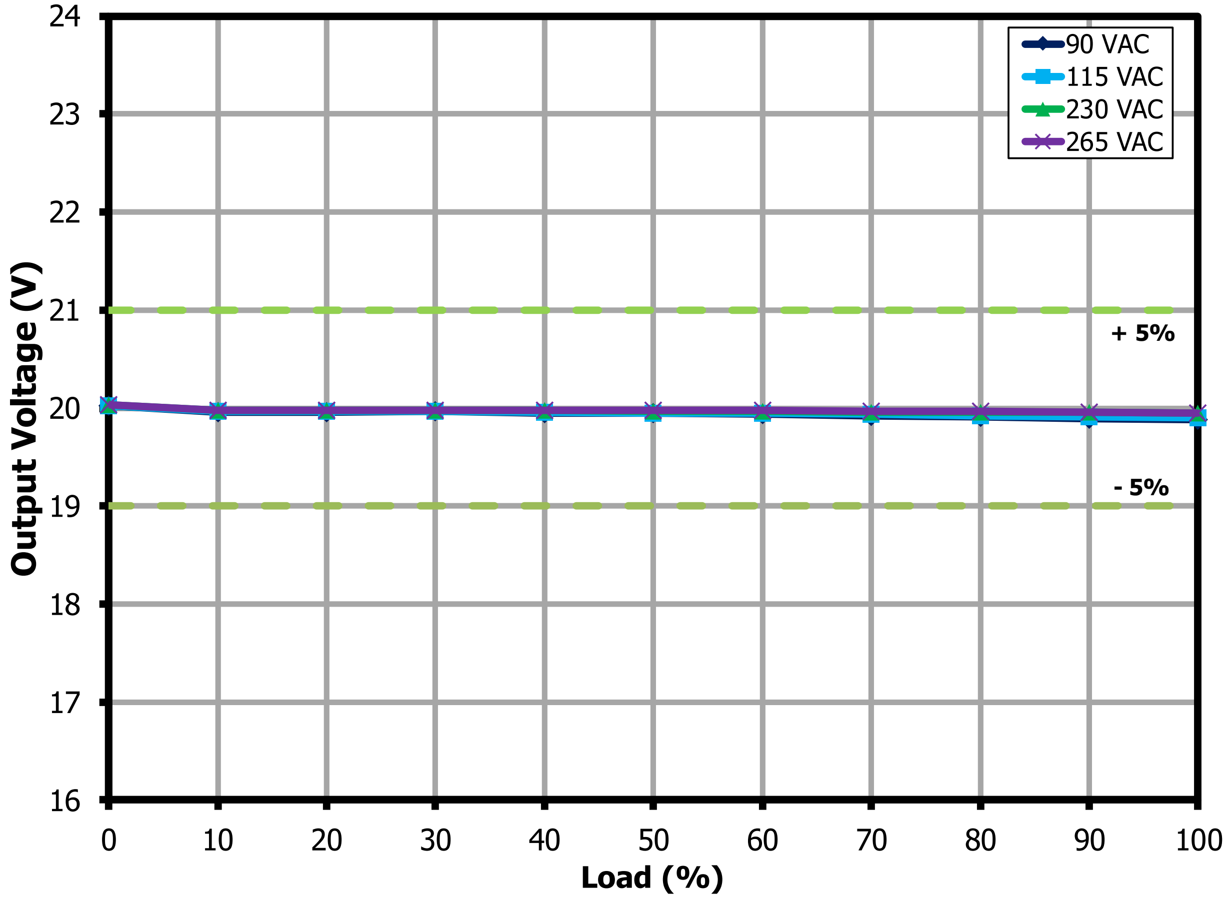

Figure 44 – Output Voltage vs. Output Load for 20 V Output, Room Temperature.

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12.6 ***Line Regulation (On Board)***

12.6.1 Output: 5 V / 3 A

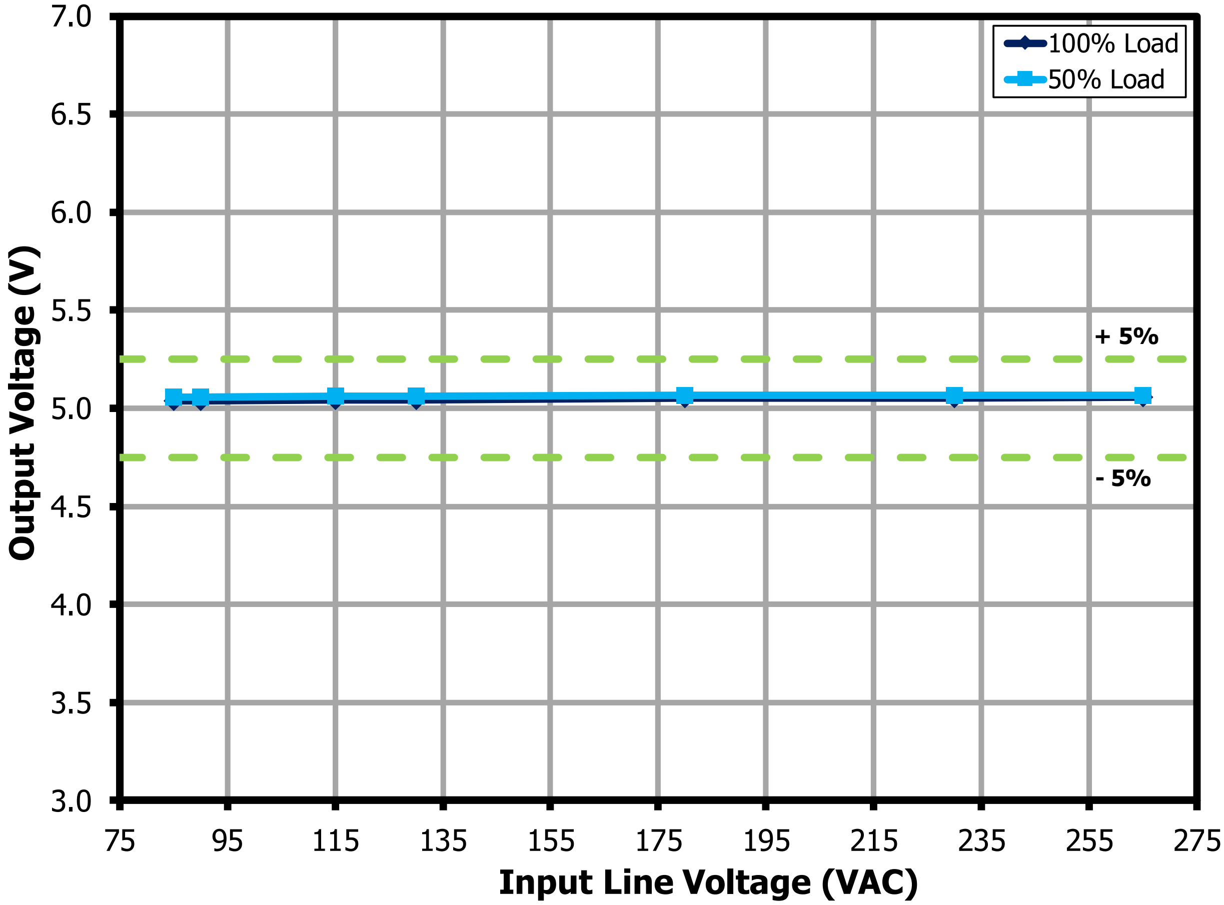

Figure 45 – Output Voltage vs. Input Line Voltage for 5 V Output, Room Temperature.

12.6.2 Output: 9 V / 3 A

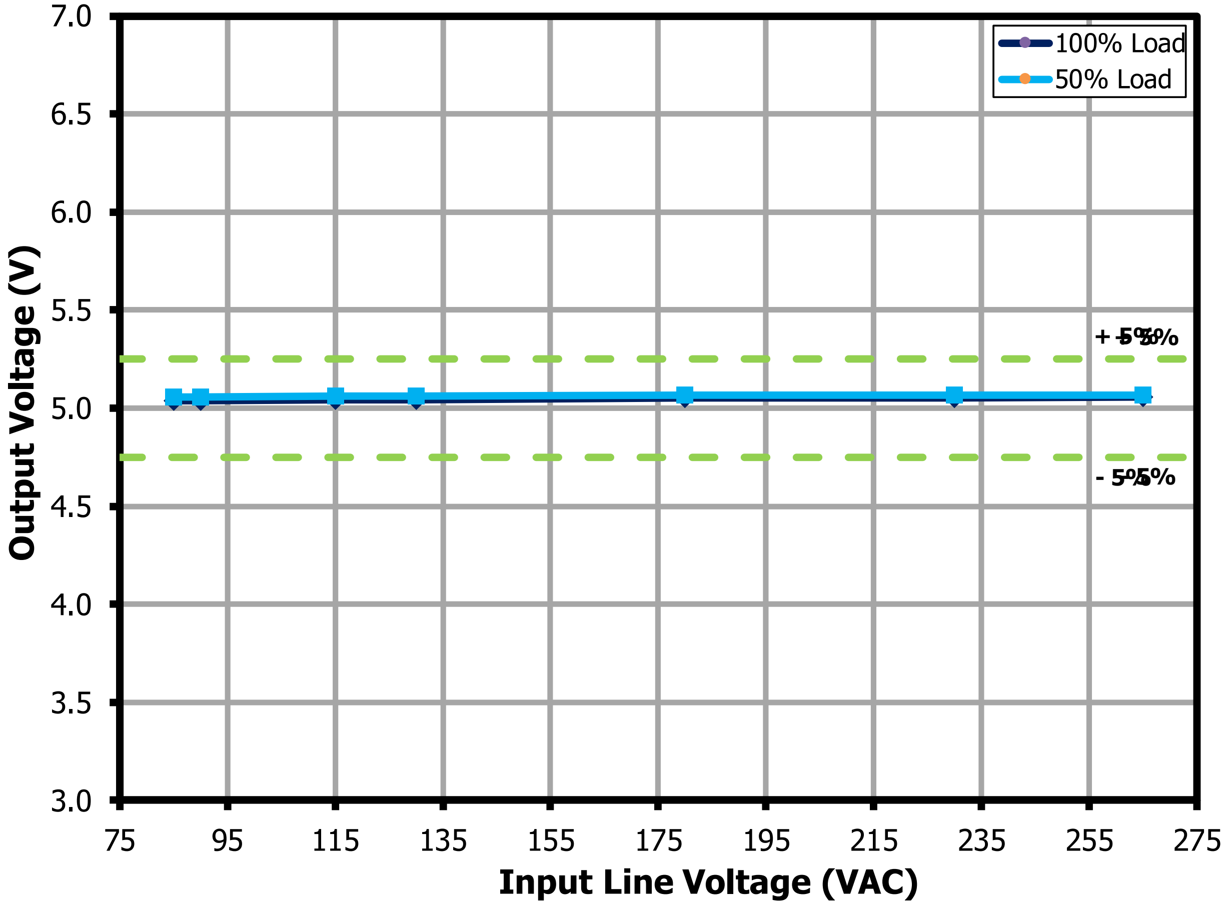

Figure 46 – Output Voltage vs. Input Line Voltage for 9 V Output, Room Temperature.

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12.6.3 Output: 15 V / 3 A

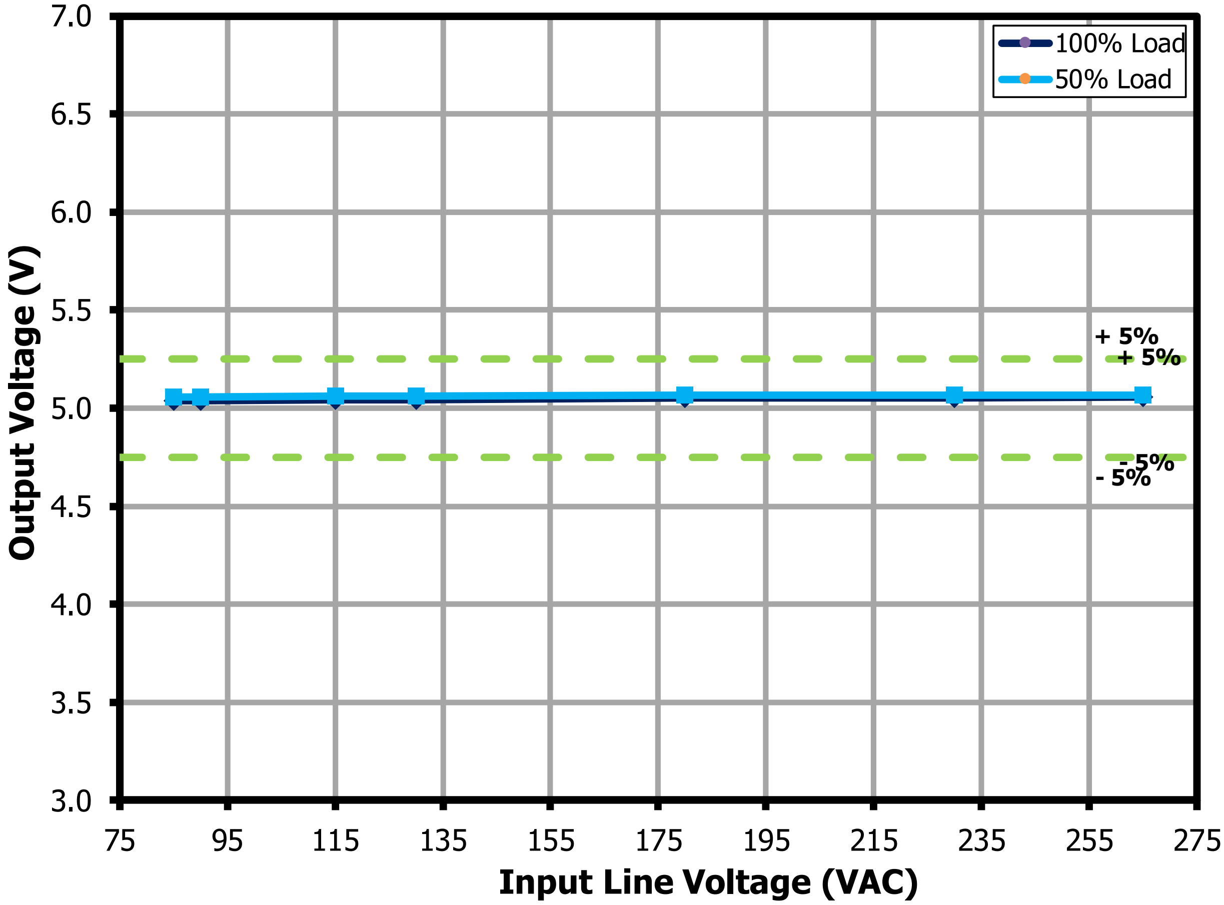

Figure 47 – Output Voltage vs. Input Line Voltage for 15 V Output, Room Temperature.

12.6.4 Output: 20 V / 3.25 A

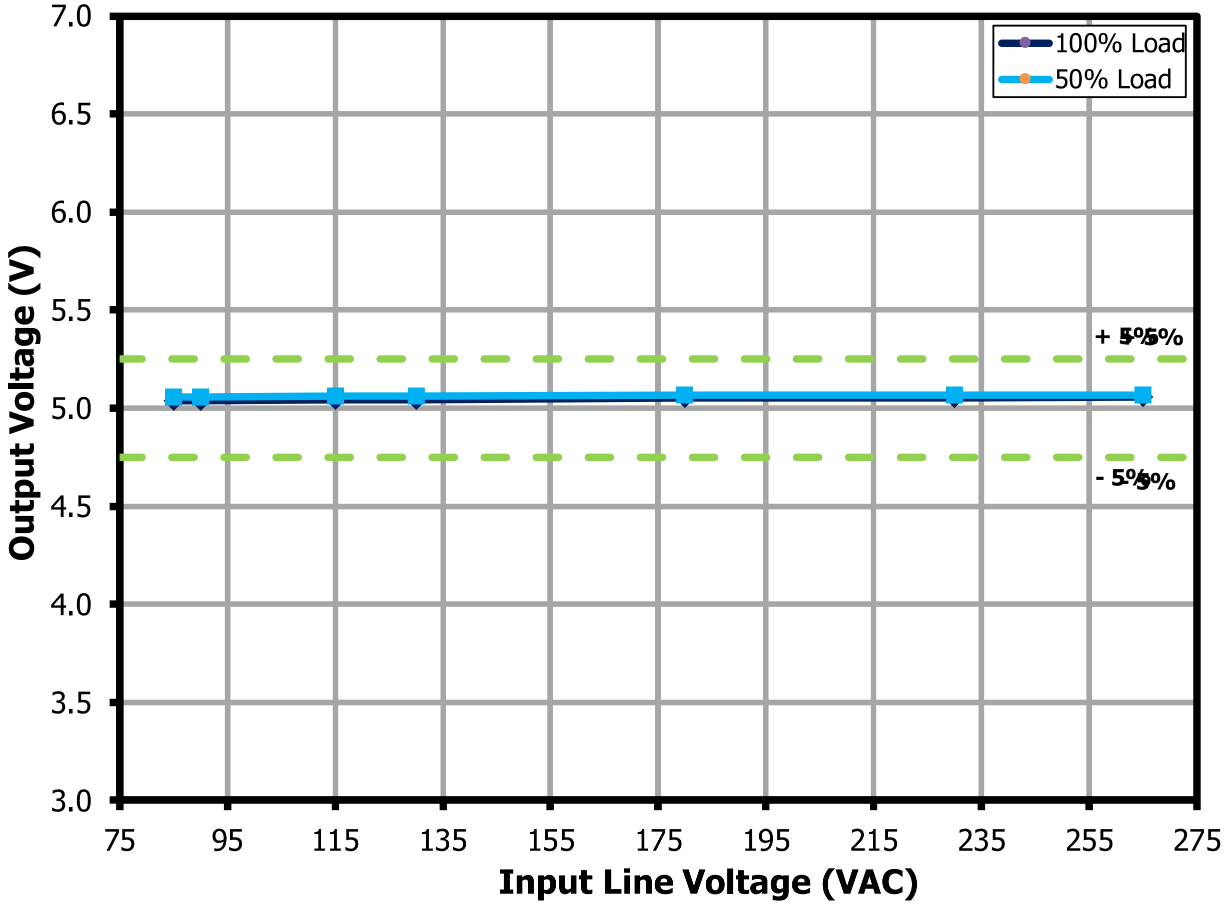

Figure 48 – Output Voltage vs. Input Line Voltage for 20 V Output, Room Temperature.

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13 Thermal Performance

13.1 *Thermal Performance in Open Case*

Note 1: Measurements taken at room temperature (approximately 24 °C).

13.1.1 Output: 20 V / 3.25 A (90 VAC)

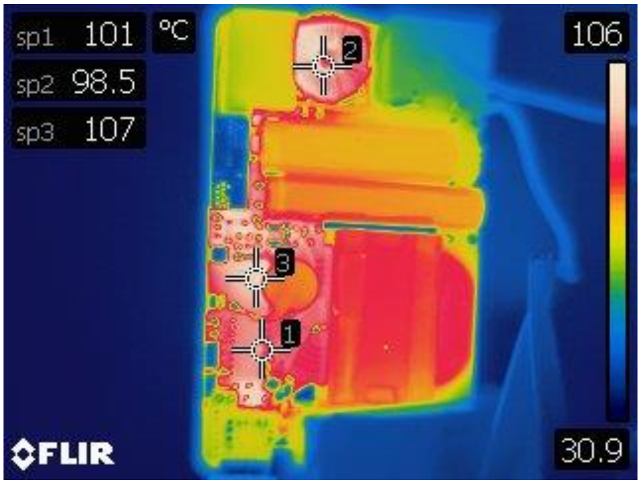

Figure 49 – Top Thermal Image.
SP1: SR FETs = 107 ºC.
SP2: CMC L2 = 98.5 ºC.
SP3: PCB below InnoSwitch3-Pro and MinE-CAP = 111 ºC.

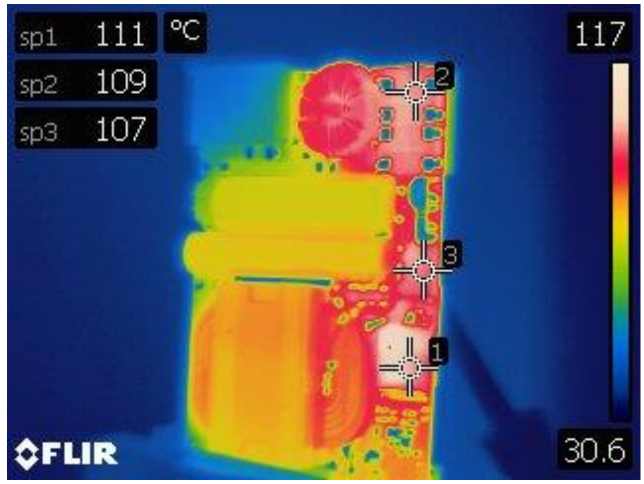

Figure 50 – Bottom Thermal Image.
SP1: InnoSwitch3-Pro = 111 ºC.
SP2: Rectifier = 109 ºC.
SP3: MinE-CAP = 107 ºC.

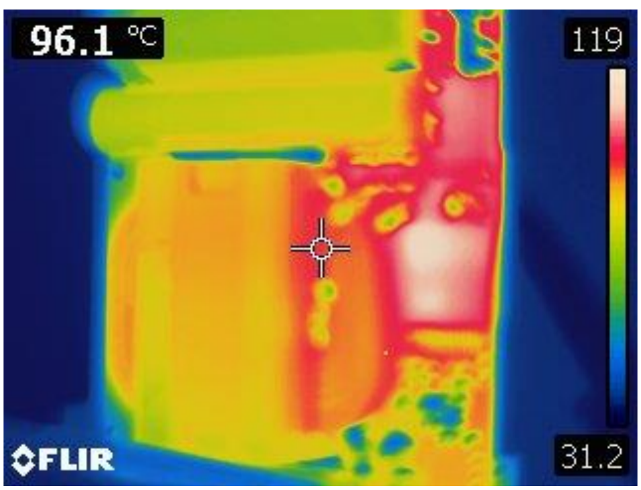

Figure 51 – Transformer Thermal Image.
Transformer PCB = 96.1 ºC.

13.1.2 Output: 20 V / 3.25 A (265 VAC)

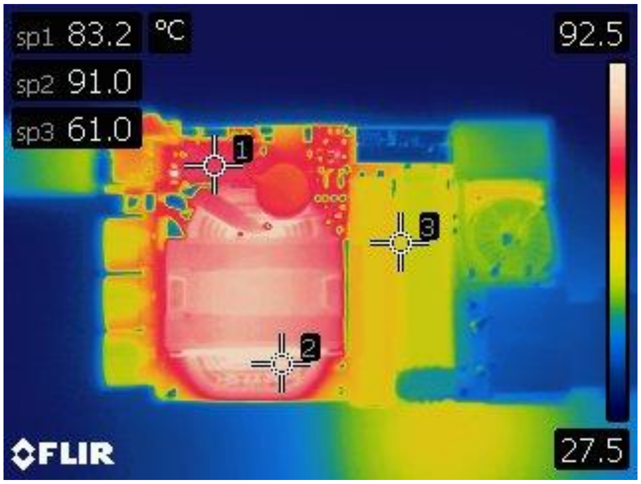

Figure 52 – Top Thermal Image.
SP1: SR FETs = 83.2 ºC.
SP2: Bulk Capacitors = 91.0 ºC.
SP3: Winding PCB = 61.0 ºC.

Figure 53 – Bottom Thermal Image.
SP1: Transformer Core = 92.0 ºC.
SP2: InnoSwitch3-Pro = 98.6 ºC.
SP3: MinE-CAP = 75.1 ºC.

Figure 54 – Bottom Thermal Image.
SP1: Output Capacitors = 60.7 ºC.
SP2: InnoSwitch3-Pro = 95.0 ºC.
SP3: CMC L2 = 75.1 ºC.

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13.2 ***Thermal Performance with Adapter Case Enclosure***

13.2.1 Output: 20 V / 3.25 A (90 VAC) at 27 °C Ambient Temperature

Component	**Steady-State Temperature (°C)**
CMC, L2	87.4
Bridge Rectifier, BR1	90.3
MinE-CAP, U2	90.2
InnoSwitch3-Pro, U1	94.1
Pass FET, Q1	84.7
Transformer, T1	91.7
Input Capacitor, C1	78.7
SR FET, Q2	89.1
Enclosure	72.5

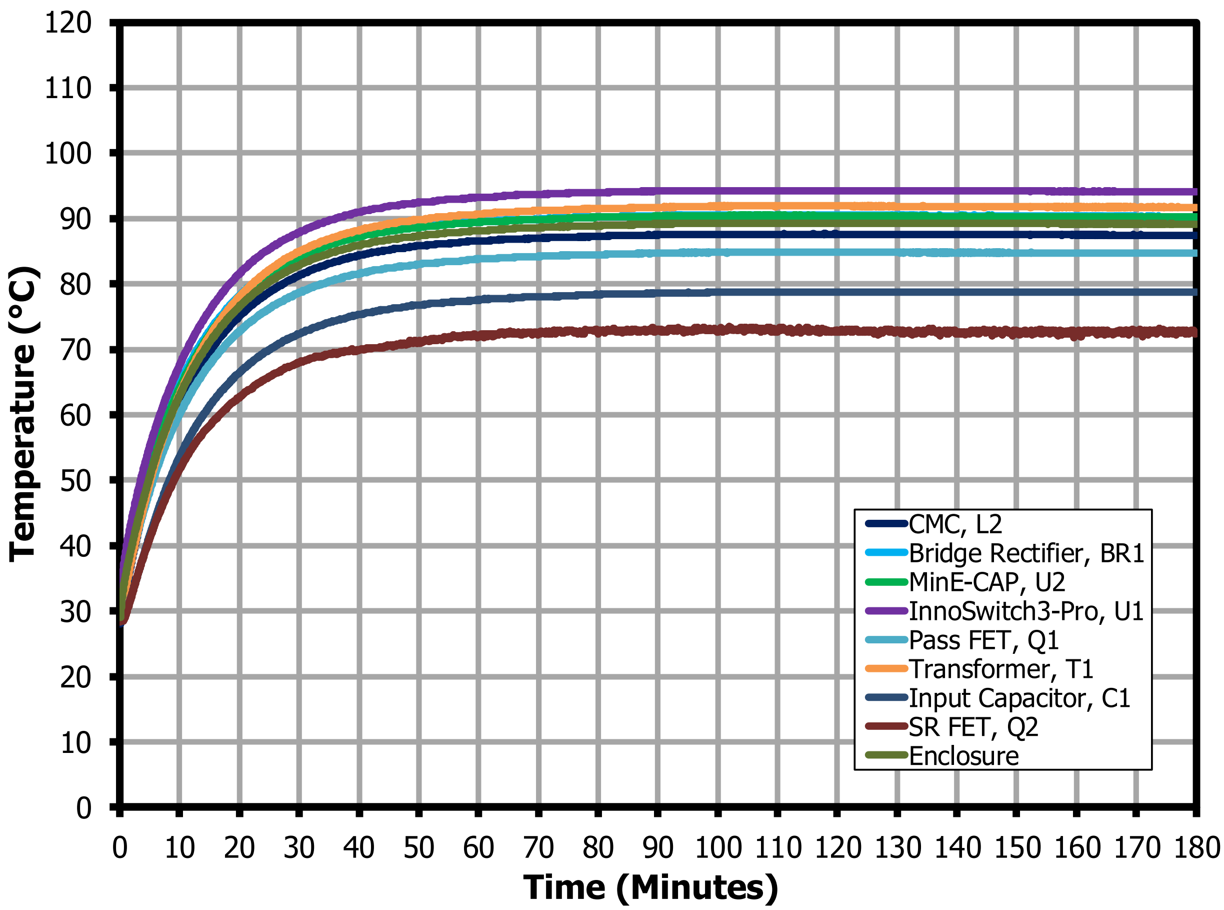

Figure 55 –Unit Thermal Performance at 90 VAC with Case, Room Temperature.

13.2.2 Output: 20 V / 3.25 A (265 VAC) at 27 °C Ambient Temperature

Component	Steady-state Temperature (°C)
CMC, L2	75.6
Bridge Rectifier, BR1	79.5
MinE-CAP, U2	81.3
InnoSwitch3-Pro, U1	87.1
Pass FET, Q1	83.1
Transformer, T1	91.1
Input Capacitor, C1	77.8
SR FET, Q2	85.9
Enclosure	64.7

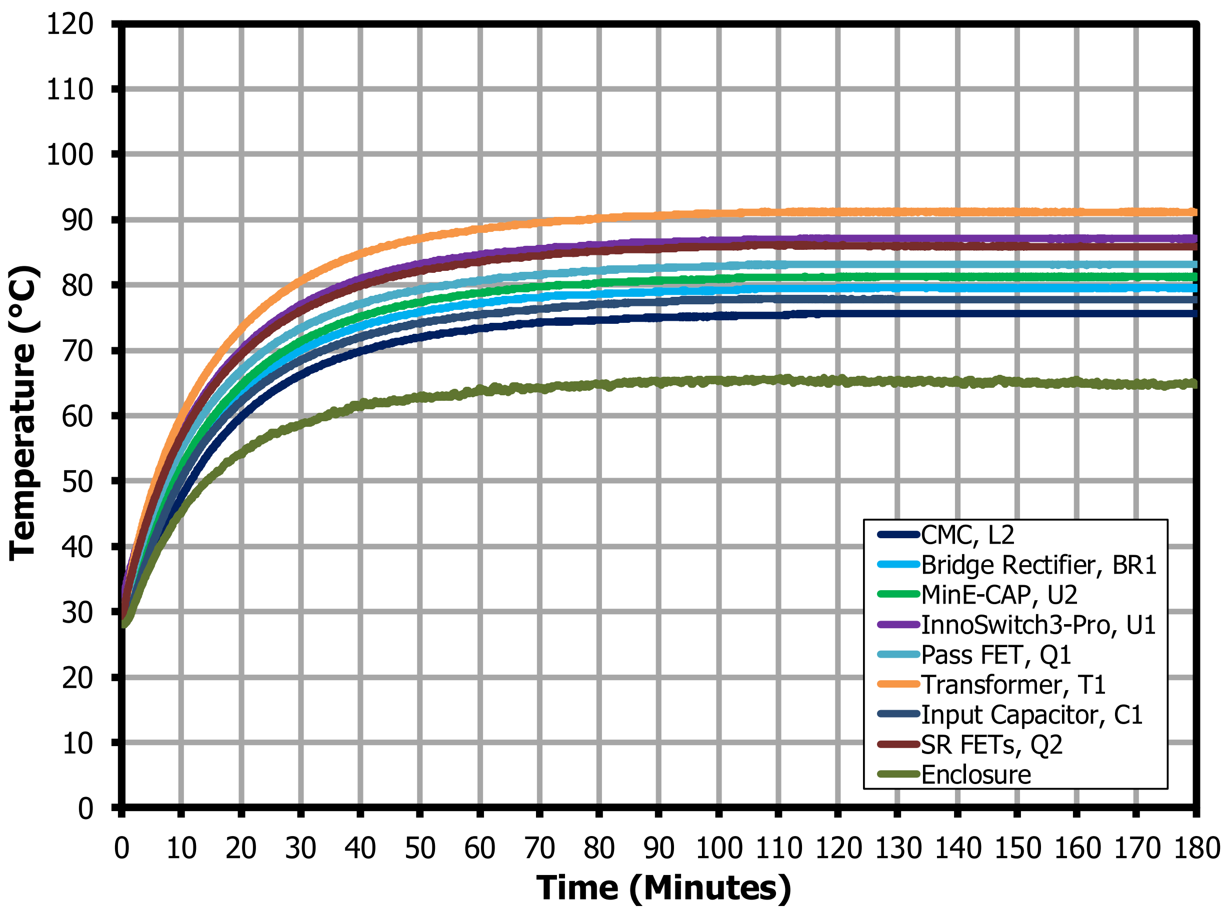

Figure 56 – Unit Thermal Performance at 265 VAC with Case, Room Temperature.

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13.2.3 13.3.3 Output: 20 V / 3.25 A (115 VAC) at 40 °C Ambient Temperature

Component	Steady-state Temperature (°C)
CMC, L2	97.5
Bridge Rectifier, BR1	100.5
MinE-CAP, U2	102
InnoSwitch3-Pro, U1	106.6
Pass FET, Q1	98
Transformer, T1	105.4
Input Capacitor, C1	93.2
SR FET, Q2	102.3
Enclosure	82.2

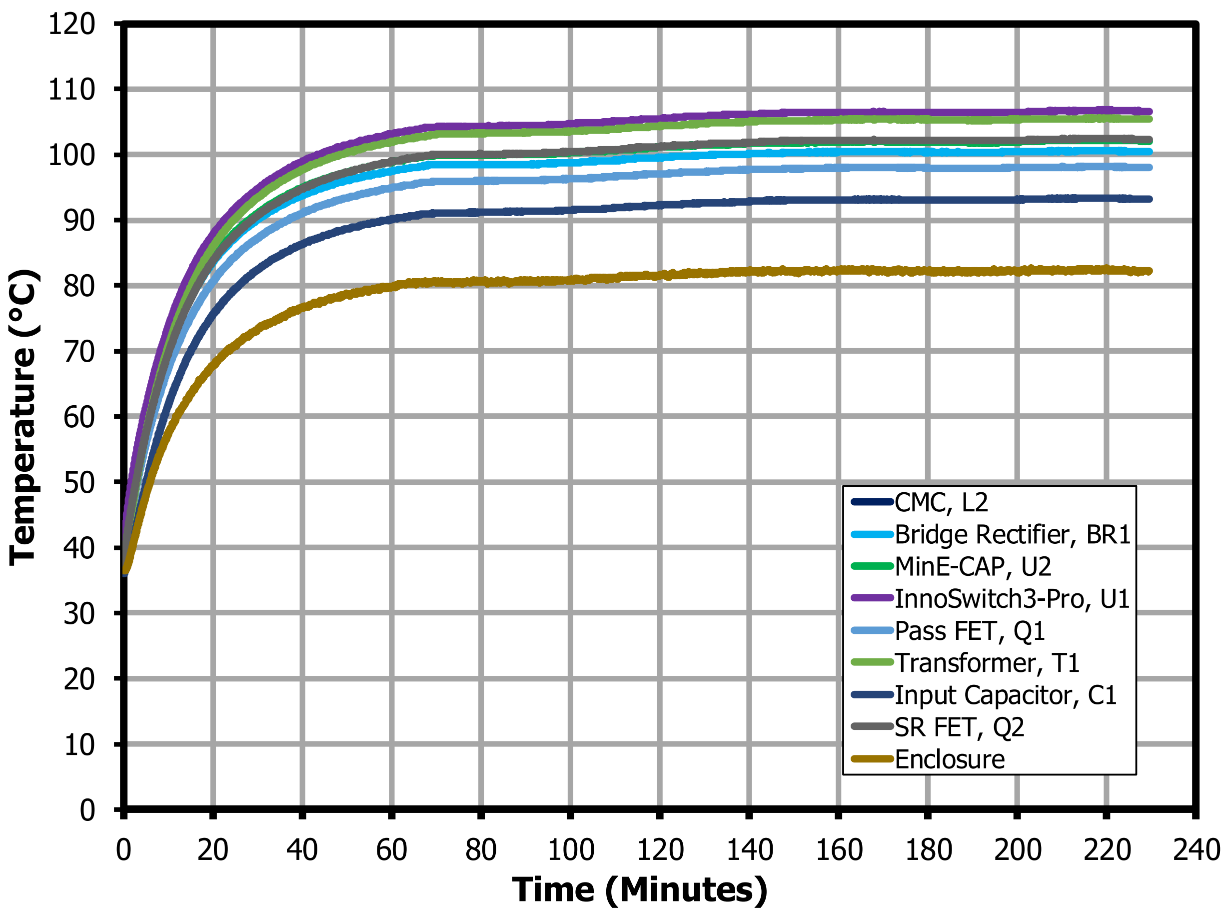

Figure 57 – Unit Thermal Performance at 115 VAC with Case, 40 °C Ambient Temperature.

13.2.4 13.3.4 Output: 20 V / 3.25 A (230 VAC) at 40 °C Ambient Temperature

Component	Steady-state Temperature (°C)
CMC, L2	74.5
Bridge Rectifier, BR1	78.9
MinE-CAP, U2	80.3
InnoSwitch3-Pro, U1	86.3
Pass FET, Q1	83.6
Transformer, T1	92
Input Capacitor, C1	82
SR FETs, Q2	87.1
Enclosure	70.9

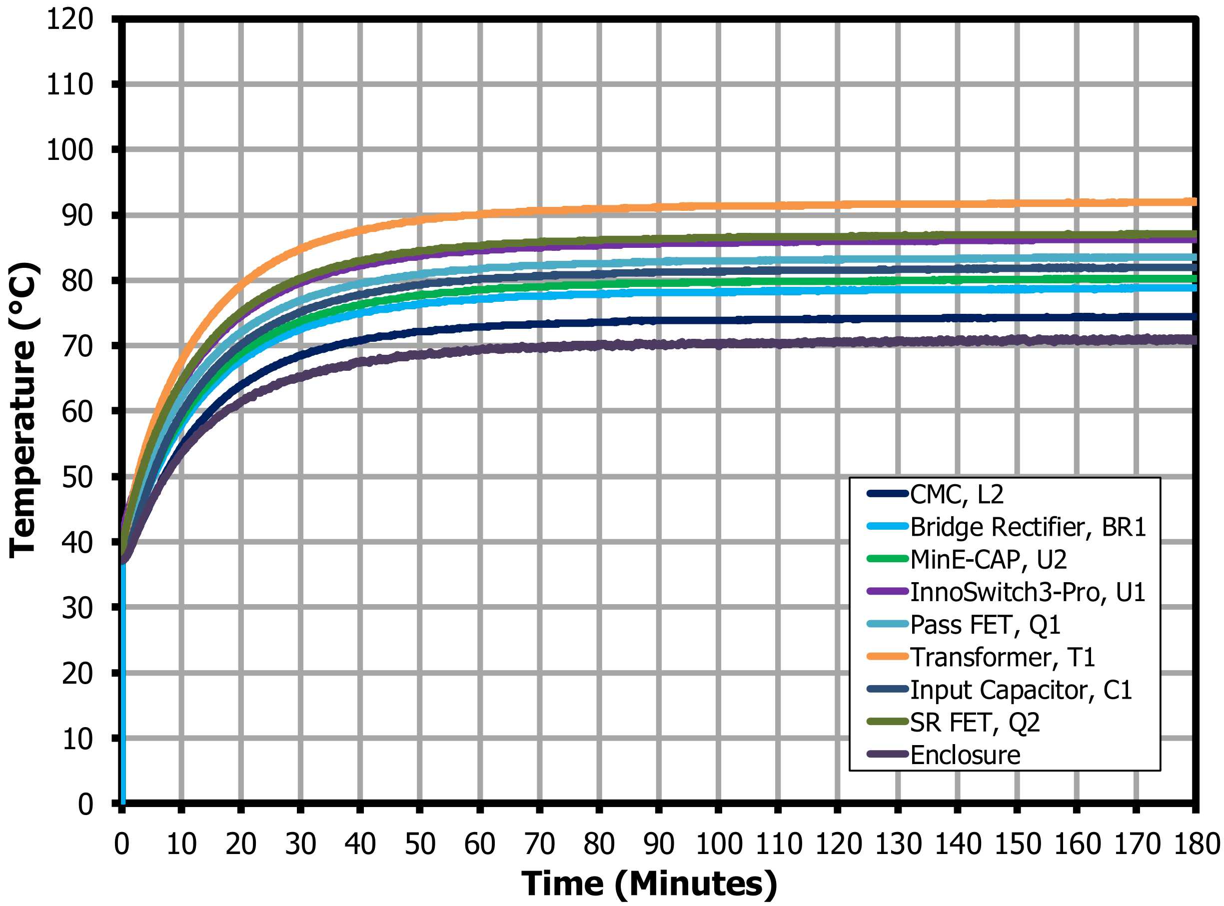

Figure 58 – Unit Thermal Performance at 230 VAC with Case, 40 °C Ambient Temperature.

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14 **Waveforms**

Note: Measurements taken at room temperature (approximately 24 °C).

14.1 ***Start-up Waveforms***

14.1.1 Output Voltage and Current

Note: Output voltages captured at the end of 100 mΩ cable.

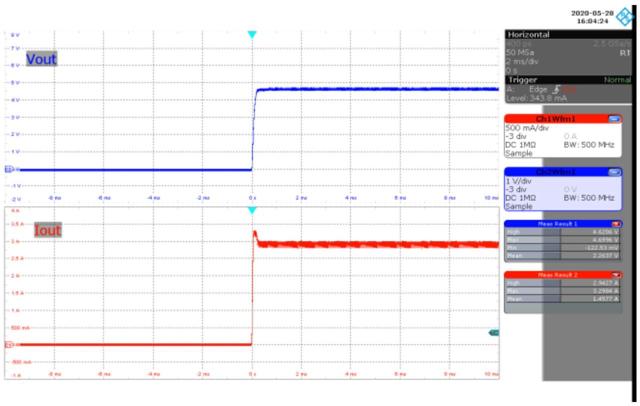

Figure 59 – Output Voltage and Current.
90 VAC, 5.0 V, 3 A Load (4.69 V_{MAX}).
CH4: V_{OUT}, 1 V / div.
CH1: I_{LOAD}, 0.5 A / div.
Time: 2 ms / div.

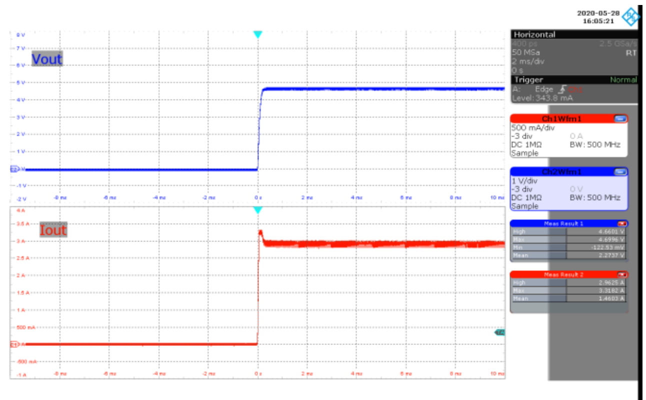

Figure 60 – Output Voltage and Current.
265 VAC, 5.0 V, 3 A Load (4.69 V_{MAX}).
CH4: V_{OUT}, 1 V / div.
CH1: I_{LOAD}, 0.5 A / div.
Time: 2 ms / div.

14.1.2 Primary Drain Voltage and Current

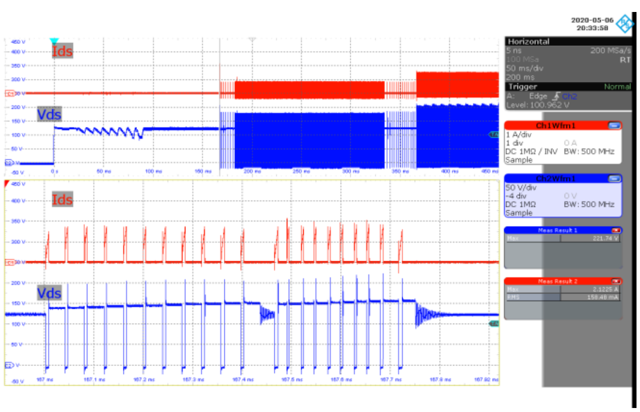

Figure 61 – Primary Drain Voltage and Current.
90 VAC, 5.0 V, 3 A Load (222 V_{MAX}).
CH2: V_{DRAIN}, 50 V / div.
CH1: I_{DRAIN}, 1 A / div.
Time: 50 ms / div. (100 µs / div. Zoom).

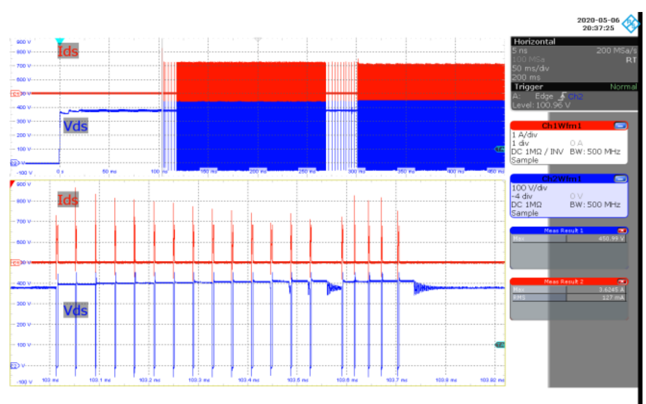

Figure 62 – Primary Drain Voltage and Current.
265 VAC, 5.0 V, 3 A Load (452 V_{MAX}).
CH2: V_{DRAIN}, 100 V / div.
CH1: I_{DRAIN}, 1 A / div.
Time: 50 ms / div. (100 µs / div. Zoom).

14.1.3 SR FET Drain Voltage and Current

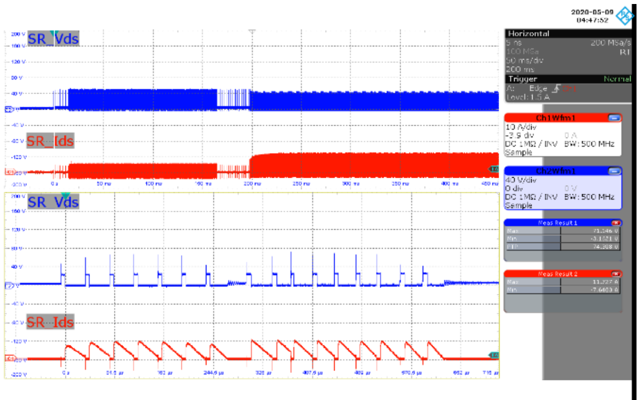

Figure 63 – SR FET Drain Voltage and Current.
90 VAC, 5.0 V, 3 A Load (71 V_{MAX}).
CH2: $V_{DRAIN(SR)}$, 40 V / div.
CH1: $I_{DRAIN(SR)}$, 10 A / div.
Time: 50 ms / div. (125 µs / div. Zoom).

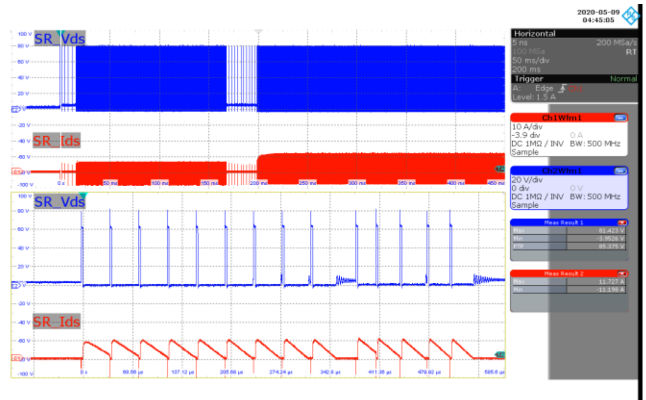

Figure 64 – SR FET Drain Voltage and Current.
265 VAC, 5.0 V, 3 A Load (81 V_{MAX}).
CH2: $V_{DRAIN(SR)}$, 20 V / div.
CH1: $I_{DRAIN(SR)}$, 10 A / div.
Time: 50 ms / div. (125 µs / div. Zoom).

14.1.4 MinE-CAP Start-up HV Capacitor, LV Capacitor and MinE-CAP Drain Current

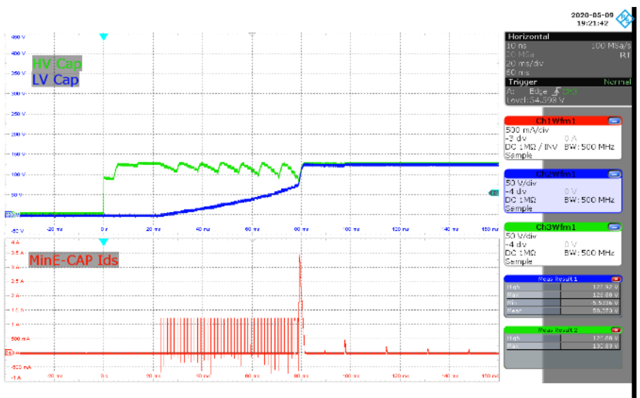

Figure 65 – MinE-CAP Start-up Active Charge.
90 VAC, 5.0 V, 3 A Load.
CH1: $I_{DRAIN(MinE\text{-}CAP)}$, 0.5 A / div.
CH2: $V_{CLV(MinE\text{-}CAP)}$, 50 V / div.
CH3: $V_{CHV(MinE\text{-}CAP)}$, 50 V / div.
Time: 10 ms / div.

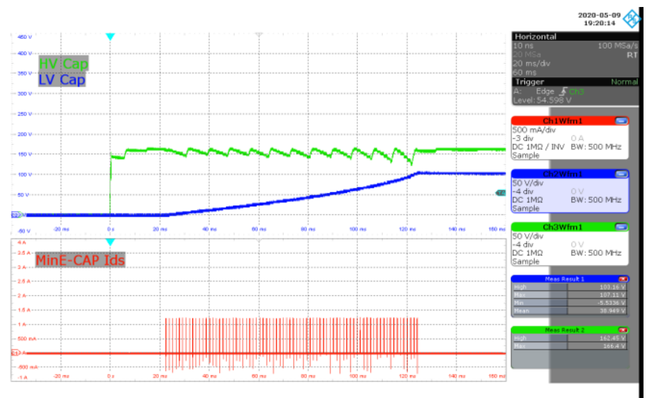

Figure 66 – MinE-CAP Start-up Active Charge.
115 VAC, 5.0 V, 3 A Load.
CH1: $I_{DRAIN(MinE\text{-}CAP)}$, 0.5 A / div.
CH2: $V_{CLV(MinE\text{-}CAP)}$, 50 V / div.
CH3: $V_{CHV(MinE\text{-}CAP)}$, 50 V / div.
Time: 10 ms / div.

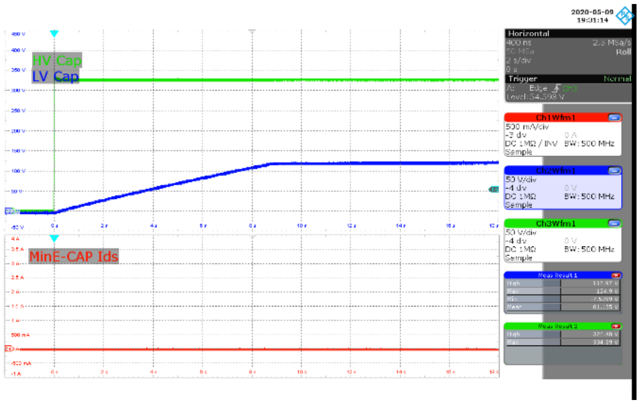

Figure 67 – MinE-CAP Start-up Trickle Charge.
230 VAC, 5.0 V, 3 A Load.
CH1: $I_{DRAIN(MinE-CAP)}$, 0.5 A / div.
CH2: $V_{CLV(MinE-CAP)}$, 50 V / div.
CH3: $V_{CHV(MinE-CAP)}$, 50 V / div.
Time: 2 s / div.

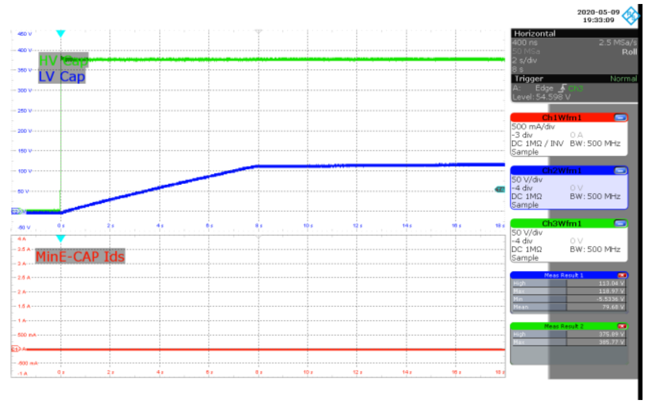

Figure 68 – MinE-CAP Start-up Trickle Charge.
265 VAC, 5.0 V, 3 A Load.
CH1: $I_{DRAIN(MinE-CAP)}$, 0.5 A / div.
CH2: $V_{CLV(MinE-CAP)}$, 50 V / div.
CH3: $V_{CHV(MinE-CAP)}$, 50 V / div.
Time: 2 s / div.

14.2 *Load Transient Response*

Note: Output voltages captured at the end of 100 mΩ cable.

14.2.1 Output: 5 V / 3 A

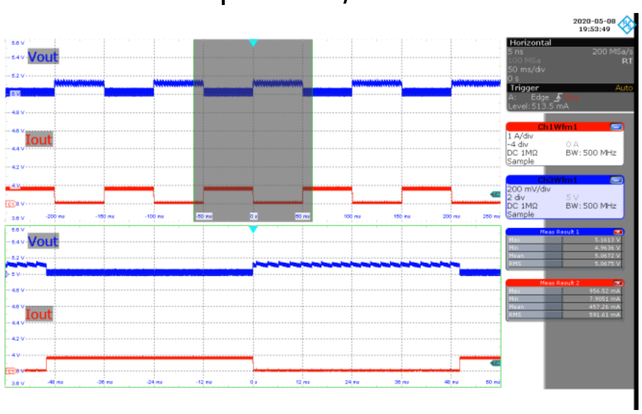

Figure 69 – Transient Response.
90 VAC, 5.0 V, 0 – 0.75 A Load Step.
V_{MIN}: 4.963V, V_{MAX}: 5.161 V.
CH3: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom).

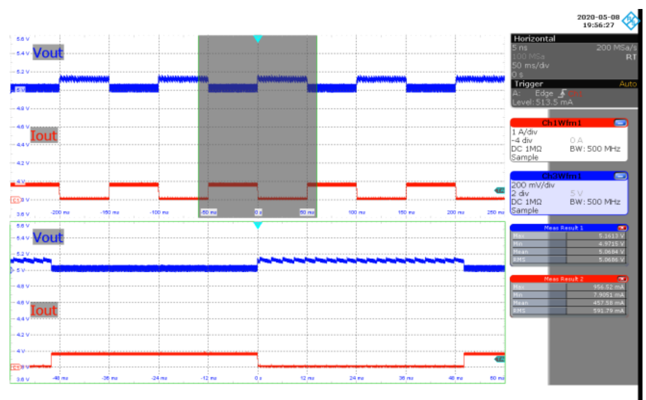

Figure 70 – Transient Response.
265 VAC, 5.0 V, 0 – 0.75 A Load Step.
V_{MIN}: 4.97 V, V_{MAX}: 5.161 V.
CH3: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom).

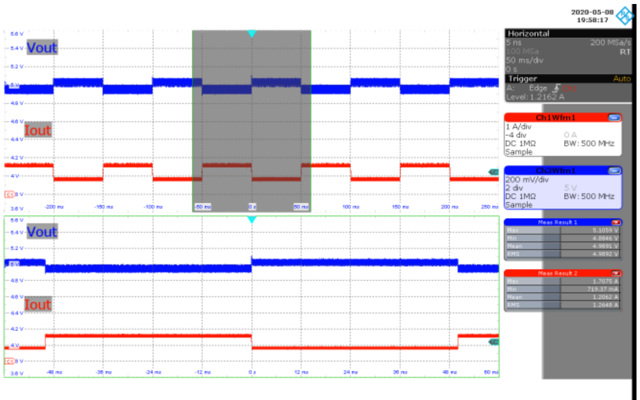

Figure 71 – Transient Response.
90 VAC, 5.0 V, 0.75 – 1.5 A Load Step.
V_{MIN}: 4.884 V, V_{MAX}: 5.105 V.
CH3: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom).

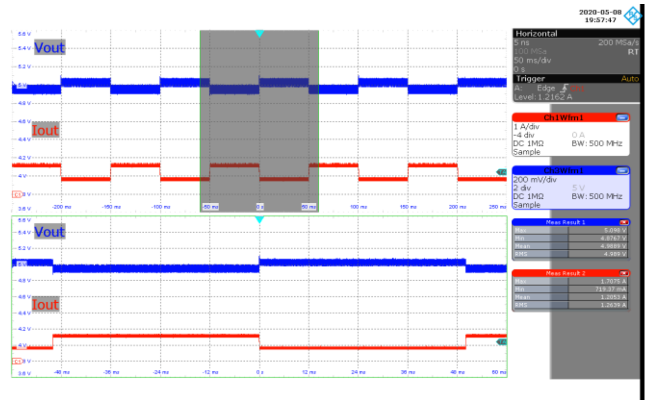

Figure 72 – Transient Response.
265 VAC, 5.0 V, 0.75 – 1.5 A Load Step.
V_{MIN}: 4.876 V, V_{MAX}: 5.098 V.
CH3: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom).

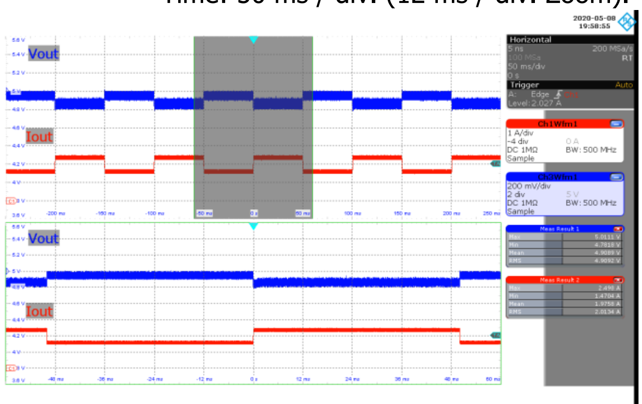

Figure 73 – Transient Response.
90 VAC, 5.0 V, 1.5 – 2.25 A Load Step.
V_{MIN}: 4.781 V, V_{MAX}: 5.011 V.
CH3: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom).

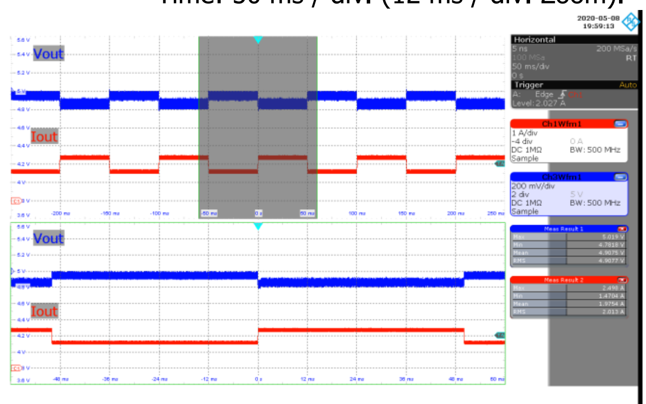

Figure 74 – Transient Response.
265 VAC, 5.0 V, 1.5 – 2.25 A Load Step.
V_{MIN}: 4.781 V, V_{MAX}: 5.019 V.
CH3: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom).

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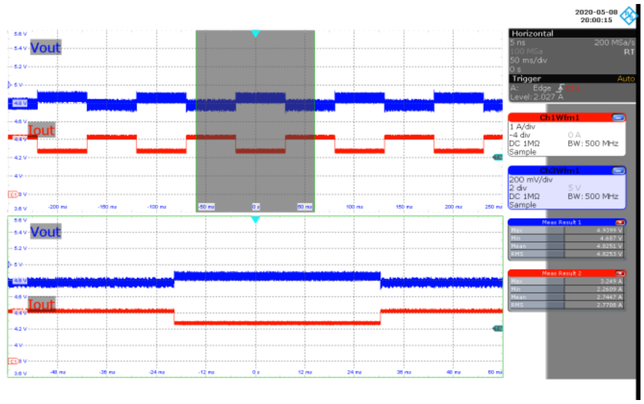

Figure 75 – Transient Response.
90 VAC, 5.0 V, 2.25 – 3 A Load Step.
V_{MIN}: 4.687 V, V_{MAX}: 4.939 V.
CH3: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom).

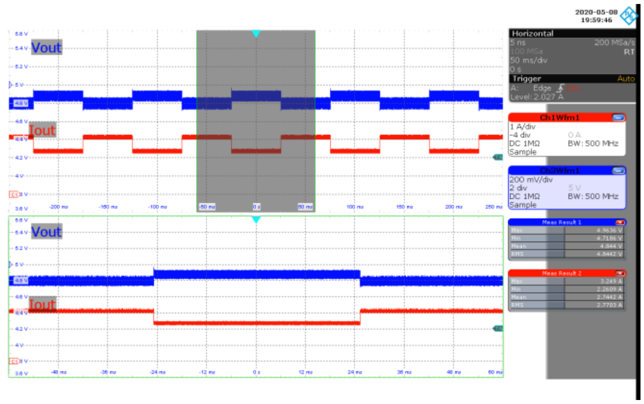

Figure 76 – Transient Response.
265 VAC, 5.0 V, 2.25 – 3 A Load Step.
V_{MIN}: 4.718 V, V_{MAX}: 4.963 V.
CH3: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom).

14.2.2 Output: 9 V / 3 A

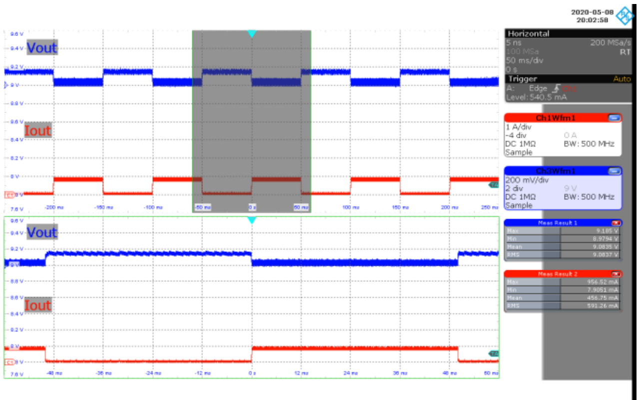

Figure 77 – Transient Response.
90 VAC, 9.0 V, 0 – 0.75 A Load Step.
V_{MIN}: 8.979 V, V_{MAX}: 9.185 V.
CH3: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (15 ms / div. Zoom).

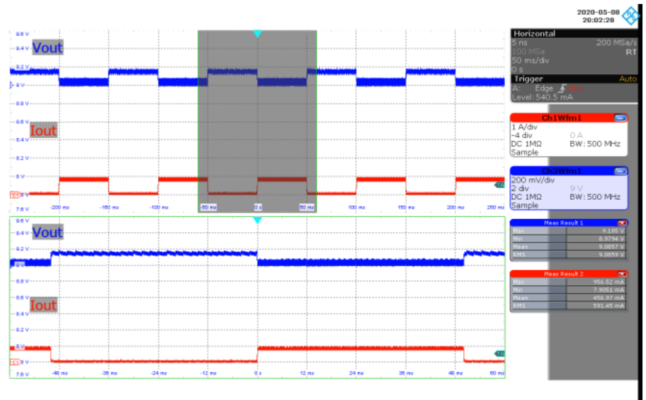

Figure 78 – Transient Response.
265 VAC, 9.0 V, 0 – 0.75 A Load Step.
V_{MIN}: 8.979 V, V_{MAX}: 9.185 V.
CH3: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (15 ms / div. Zoom).

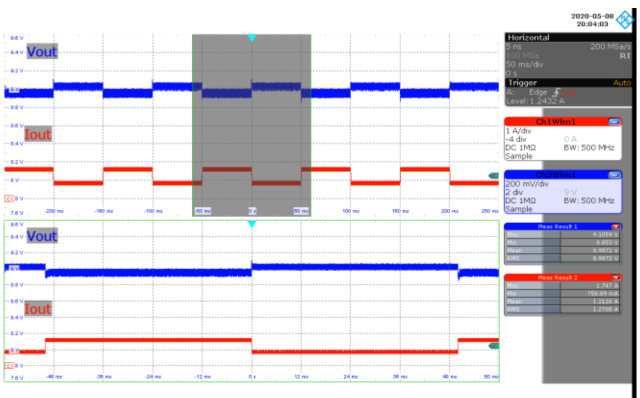

Figure 79 – Transient Response.
90 VAC, 9.0 V, 0.75 – 1.5 A Load Step.
V_{MIN}: 8.853 V, V_{MAX}: 9.105 V.
CH3: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom).

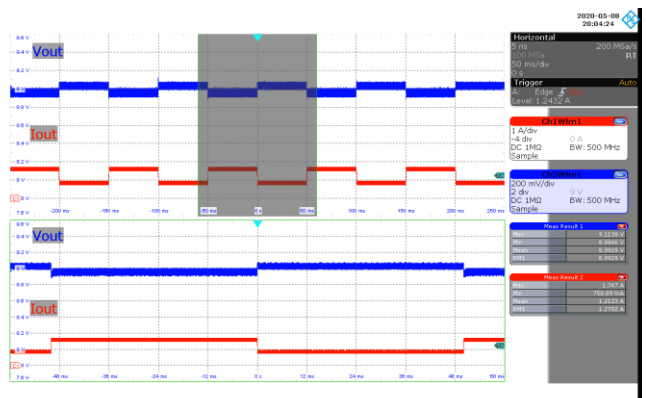

Figure 80 – Transient Response.
265 VAC, 9.0 V, 0.75 – 1.5 A Load Step.
V_{MIN}: 8.884 V, V_{MAX}: 9.113 V.
CH3: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom).

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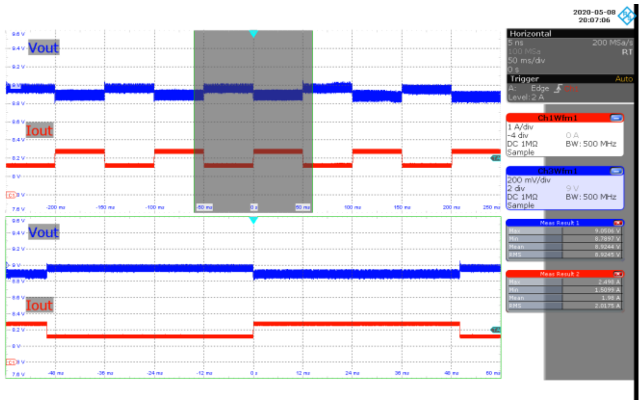

Figure 81 – Transient Response.
90 VAC, 9.0 V, 1.5 – 2.25 A Load Step.
V_{MIN}: 8.789 V, V_{MAX}: 9.050 V.
CH3: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom).

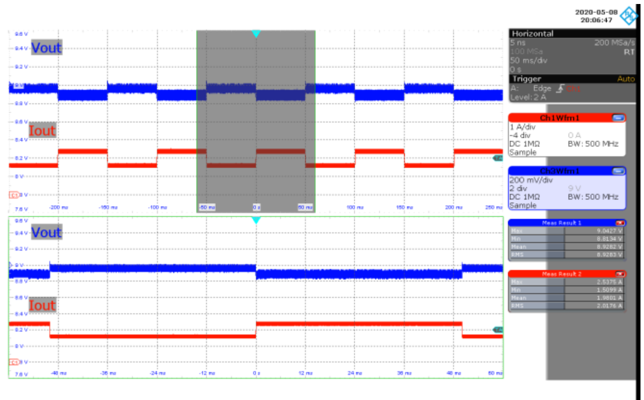

Figure 82 – Transient Response.
265 VAC, 9.0 V, 1.5 – 2.25 A Load Step.
V_{MIN}: 8.813 V, V_{MAX}: 9.042 V.
CH3: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom).

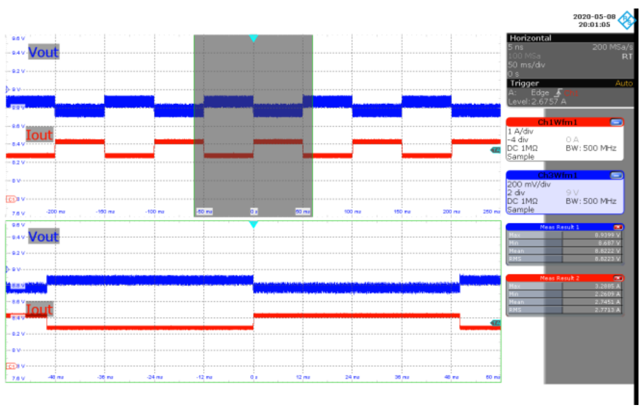

Figure 83 – Transient Response.
90 VAC, 9.0 V, 2.25 –3 A Load Step.
V_{MIN}: 8.687 V, V_{MAX}: 8.939 V.
CH3: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom).

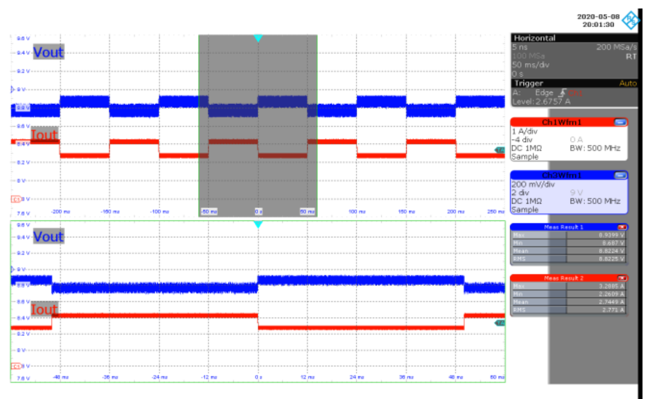

Figure 84 – Transient Response.
265 VAC, 9.0 V, 2.25 – 3 A Load Step.
V_{MIN}: 8.687 V, V_{MAX}: 8.939 V.
CH3: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom).

14.2.3 Output: 15 V / 3 A

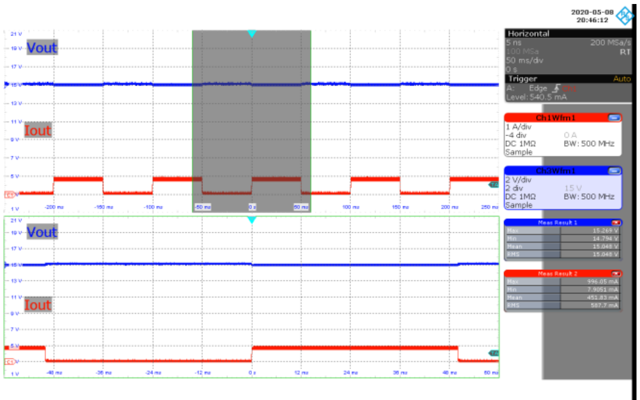

Figure 85 – Transient Response.
90 VAC, 15.0 V, 0 – 0.75 A Load Step.
V_{MIN}: 14.794 V, V_{MAX}: 15.269 V.
CH3: V_{OUT}, 2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom).

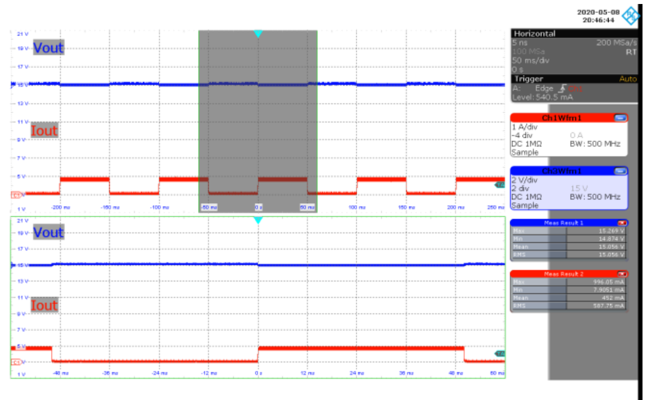

Figure 86 – Transient Response.
265 VAC, 15.0 V, 0 – 0.75 A Load Step.
V_{MIN}: 14.874 V, V_{MAX}: 15.269 V.
CH3: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom).

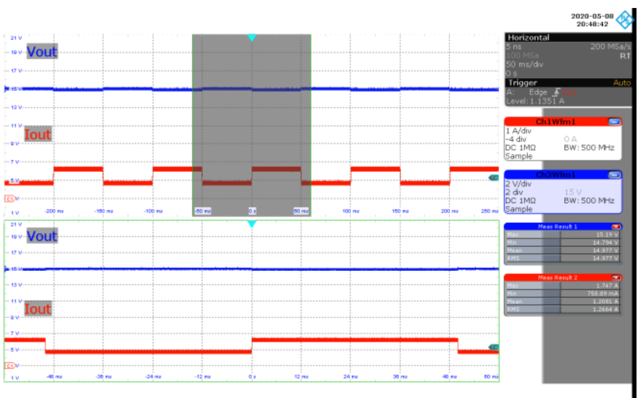

Figure 87 – Transient Response.
90 VAC, 15.0 V, 0.75 – 1.5 A Load Step.
V_{MIN}: 14.794 V, V_{MAX}: 15.19 V.
CH3: V_{OUT}, 2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom..

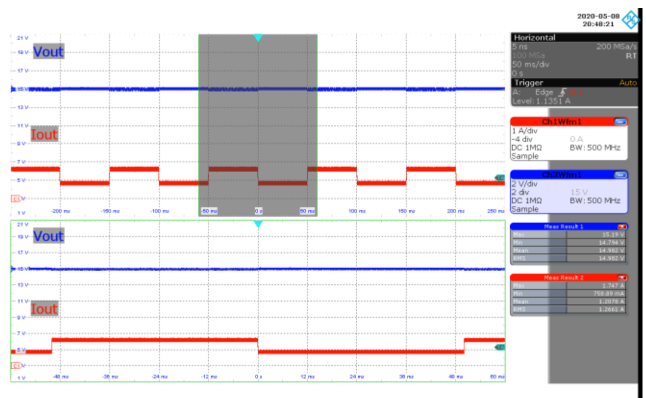

Figure 88 – Transient Response.
265 VAC, 15.0 V, 0.75 – 1.5 A Load Step.
V_{MIN}: 14.794 V, V_{MAX}: 15.19 V.
CH3: V_{OUT}, 2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom).

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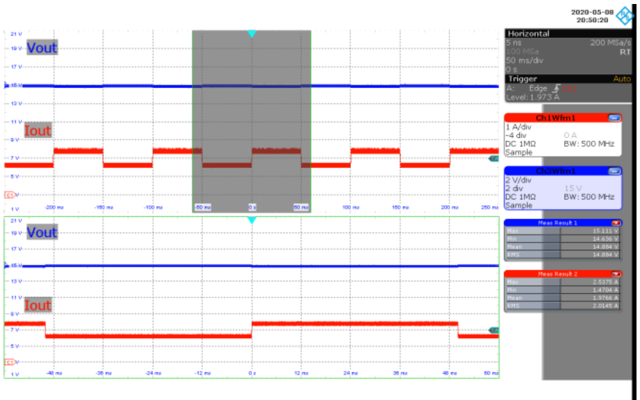

Figure 89 – Transient Response.
90 VAC, 15.0 V, 1.5 – 2.25 A Load Step.
V_{MIN}: 14.636 V, V_{MAX}: 15.111 V.
CH3: V_{OUT}, 2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom).

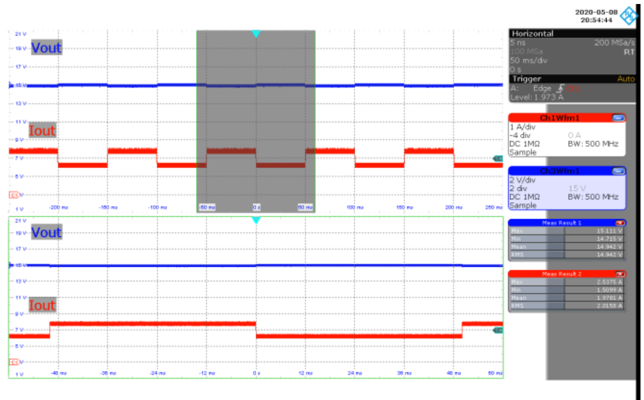

Figure 90 – Transient Response.
265 VAC, 15.0 V, 1.5 – 2.25 A Load Step.
V_{MIN}: 14.715 V, V_{MAX}: 15.111 V.
CH3: V_{OUT}, 2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom).

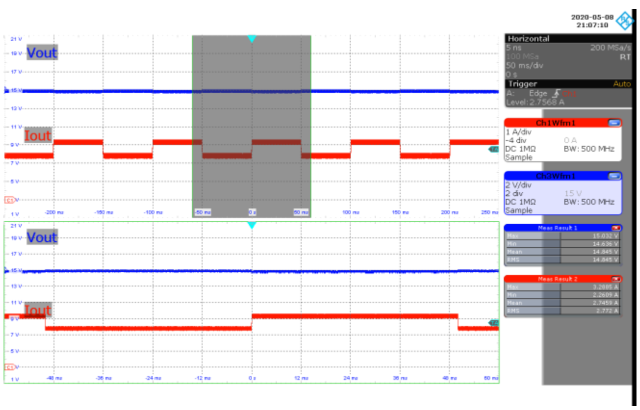

Figure 91 – Transient Response.
90 VAC, 15.0 V, 2.25 – 3 A Load Step.
V_{MIN}: 14.636 V, V_{MAX}: 15.032 V.
CH3: V_{OUT}, 2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom).

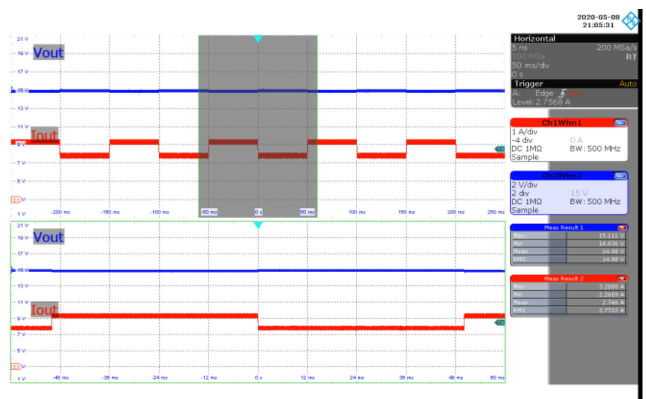

Figure 92 – Transient Response.
265 VAC, 15.0 V, 2.25 – 3 A Load Step.
V_{MIN}: 14.636 V, V_{MAX}: 15.111 V.
CH3: V_{OUT}, 2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom).

14.2.4 Output: 20 V / 3.25 A

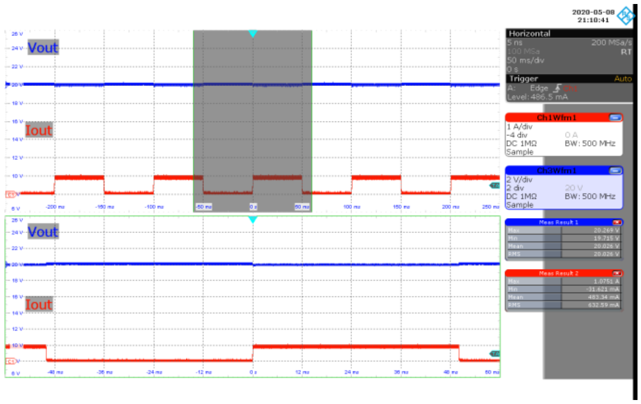

Figure 93 – Transient Response.
90 VAC, 20.0 V, 0 – 0.812 A Load Step.
V_{MIN}: 19.715 V, V_{MAX}: 20.269 V.
CH3: V_{OUT}, 2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom).

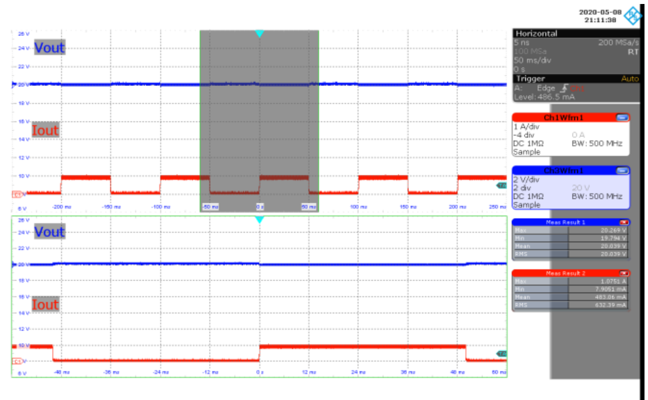

Figure 94 – Transient Response.
265 VAC, 20.0 V, 0 – 0.812 A Load Step.
V_{MIN}: 19.794 V, V_{MAX}: 20.269 V.
CH3: V_{OUT}, 2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom).

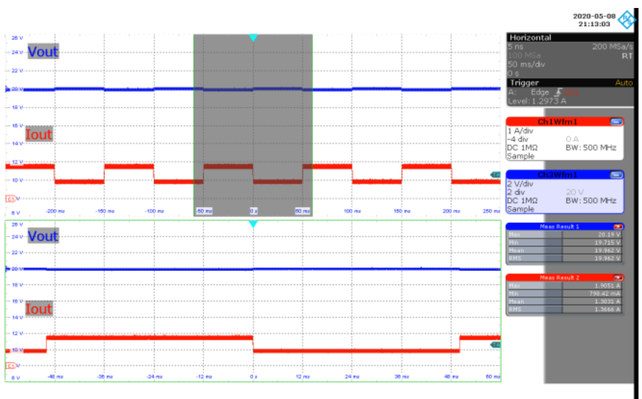

Figure 95 – Transient Response.
90 VAC, 20.0V, 0.812–1.32 A Load Step.
V_{MIN}: 19.715 V, V_{MAX}: 20.19 V.
CH3: V_{OUT}, 2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom).

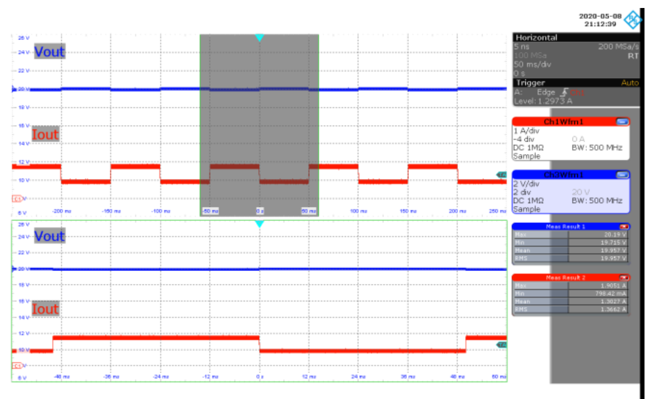

Figure 96 – Transient Response.
265 VAC, 20.0V, 0.812–1.32 A Load Step.
V_{MIN}: 19.715 V, V_{MAX}: 20.19 V.
CH3: V_{OUT}, 2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom).

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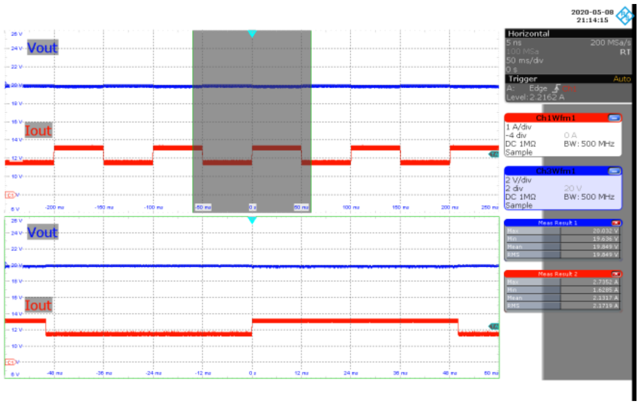

Figure 97 – Transient Response.
90 VAC, 20.0 V, 1.32–2.44 A Load Step.
V_{MIN}: 19.636 V, V_{MAX}: 20.032 V.
CH3: V_{OUT}, 2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom).

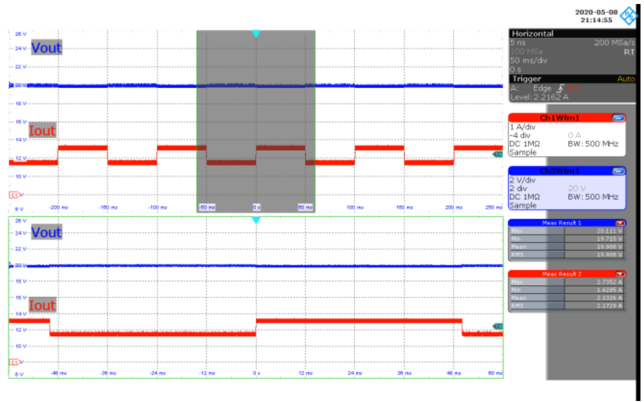

Figure 98 – Transient Response.
265 VAC, 20.0 V, 1.32–2.44 A Load Step.
V_{MIN}: 19.715 V, V_{MAX}: 20.111 V.
CH3: V_{OUT}, 2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom).

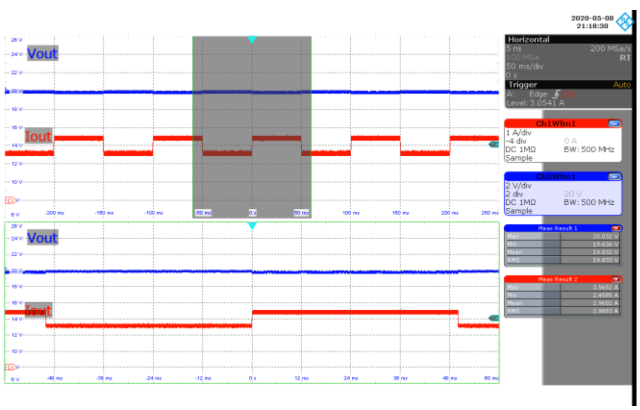

Figure 99 – Transient Response.
90 VAC, 20.0 V, 2.44–3.25 A Load Step.
V_{MIN}: 19.636 V, V_{MAX}: 20.032 V.
CH3: V_{OUT}, 2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom).

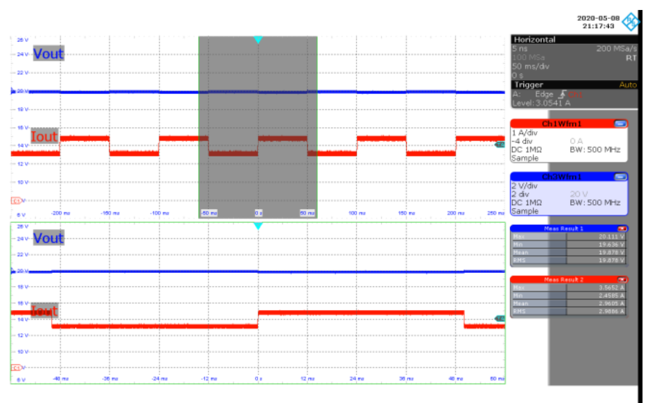

Figure 100 – Transient Response.
265 VAC, 20.0 V, 2.44–3.25 A Load Step.
V_{MIN}: 19.636 V, V_{MAX}: 20.111 V.
CH3: V_{OUT}, 2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (12 ms / div. Zoom).

14.3 *MinE-CAP HV Capacitor, LV Capacitor and MinE-CAP Switch Waveforms (Step Load Response)*

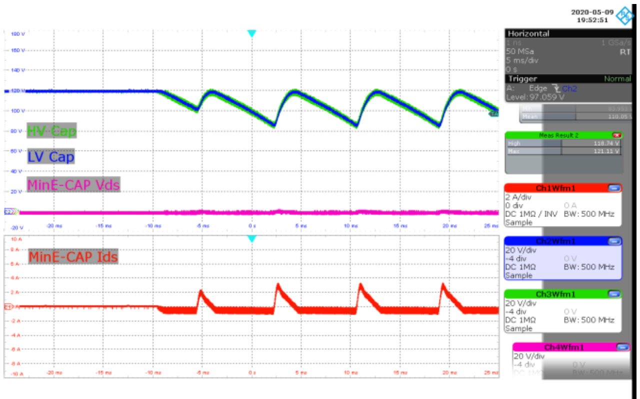

Figure 101 – MinE-CAP Step-Load Response.
90 VAC, 20 V, 0 – 3.25 A Load Step.
CH1: $I_{DRAIN(MinE\text{-}CAP)}$, 2 A / div.
CH2: $V_{CLV(MinE\text{-}CAP)}$, 20 V / div.
CH3: $V_{CHV(MinE\text{-}CAP)}$, 20 V / div.
CH4: $V_{DS(MinE\text{-}CAP)}$, 20 V / div.
Time: 5 ms / div.

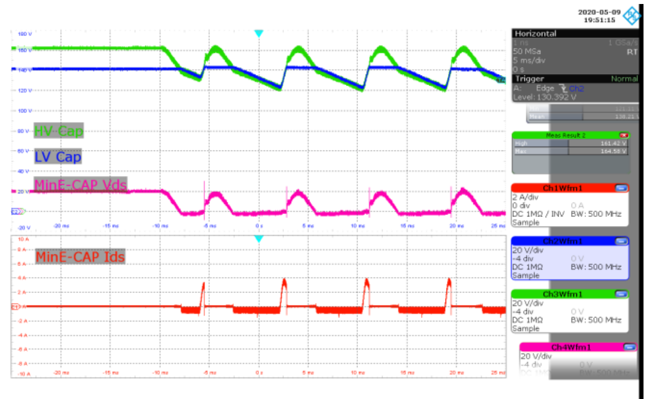

Figure 102 – MinE-CAP Start-up Active Charge.
115 VAC, 20 V, 0 – 3.25 A Load Step.
CH1: $I_{DRAIN(MinE\text{-}CAP)}$, 2 A / div.
CH2: $V_{CLV(MinE\text{-}CAP)}$, 20 V / div.
CH3: $V_{CHV(MinE\text{-}CAP)}$, 20 V / div.
CH4: $V_{DS(MinE\text{-}CAP)}$, 20 V / div.
Time: 5 ms / div.

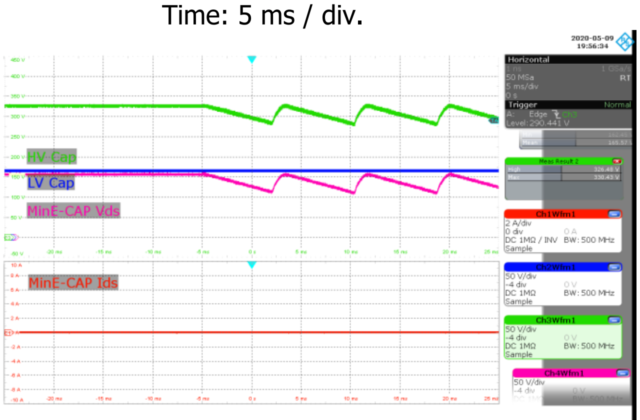

Figure 103 – MinE-CAP Start-up Active Charge.
230 VAC, 20 V, 0 – 3.25 A Load Step.
CH1: $I_{DRAIN(MinE\text{-}CAP)}$, 2 A / div.
CH2: $V_{CLV(MinE\text{-}CAP)}$, 50 V / div.
CH3: $V_{CHV(MinE\text{-}CAP)}$, 50 V / div.
CH4: $V_{DS(MinE\text{-}CAP)}$, 50 V / div.
Time: 5 ms / div.

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14.4 ***Primary Drain Voltage and Current (Steady-State)***

14.4.1 Output: 5 V / 3 A

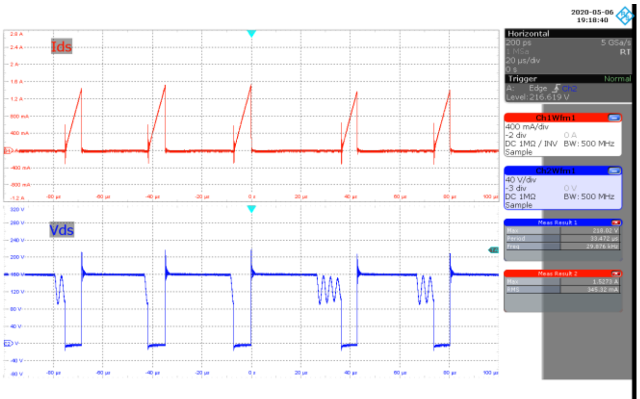

Figure 104 – Primary Drain Voltage and Current.
90 VAC, 5.0 V, 3 A Load (218 V_{MAX}).
CH2: V_{DRAIN}, 40 V / div.
CH1: I_{DRAIN}, 0.4 A / div.
Time: 20 µs / div.

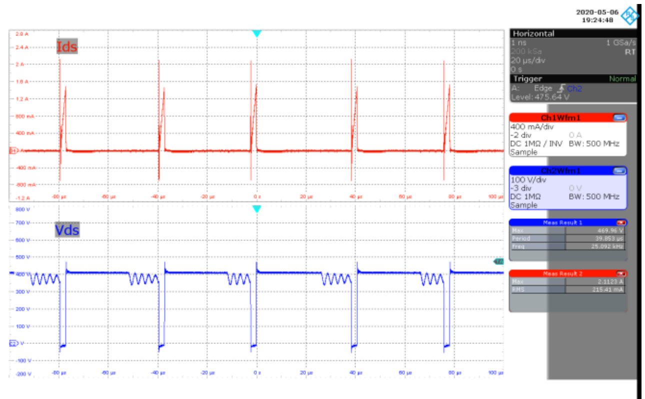

Figure 105 – Primary Drain Voltage and Current.
265 VAC, 5.0 V, 3 A Load (470 V_{MAX}).
CH2: V_{DRAIN}, 100 V / div.
CH1: I_{DRAIN}, 0.4 A / div.
Time: 20 µs / div.

14.4.2 Output: 9 V / 3 A

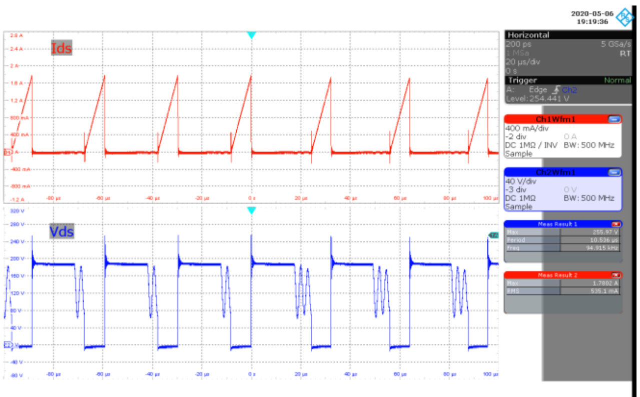

Figure 106 – Primary Drain Voltage and Current.
90 VAC, 9.0 V, 3 A Load (256 V_{MAX}).
CH2: V_{DRAIN}, 40 V / div.
CH1: I_{DRAIN}, 0.4 A / div.
Time: 20 µs / div.

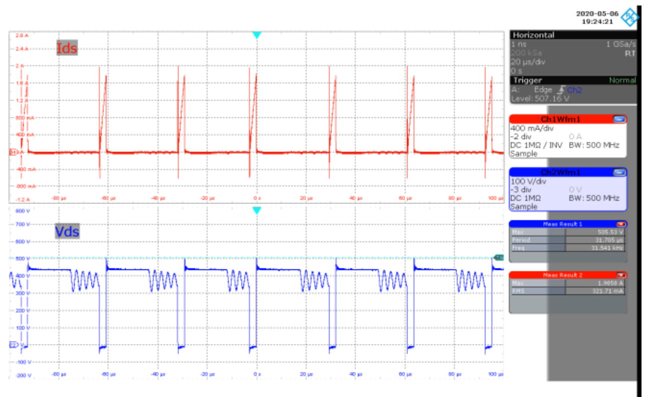

Figure 107 – Primary Drain Voltage and Current.
265 VAC, 9.0 V, 3 A Load (506 V_{MAX}).
CH2: V_{DRAIN}, 100 V / div.
CH1: I_{DRAIN}, 0.4 A / div.
Time: 20 µs / div.

14.4.3 Output: 15 V / 3 A

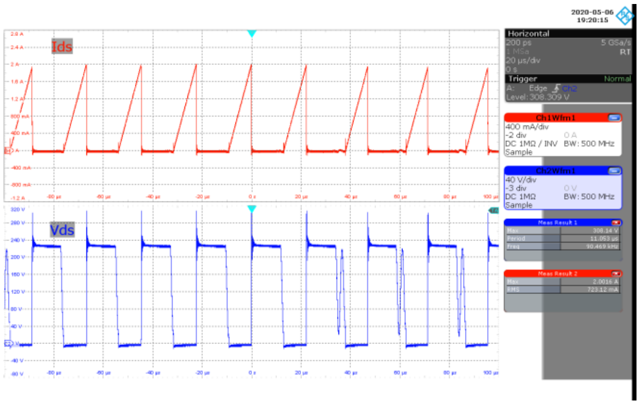

Figure 108 – Primary Drain Voltage and Current.
90 VAC, 15.0 V, 3 A Load (308 V_{MAX}).
CH4: V_{DRAIN}, 40 V / div.
CH1: I_{DRAIN}, 0.4 A / div.
Time: 20 μs / div.

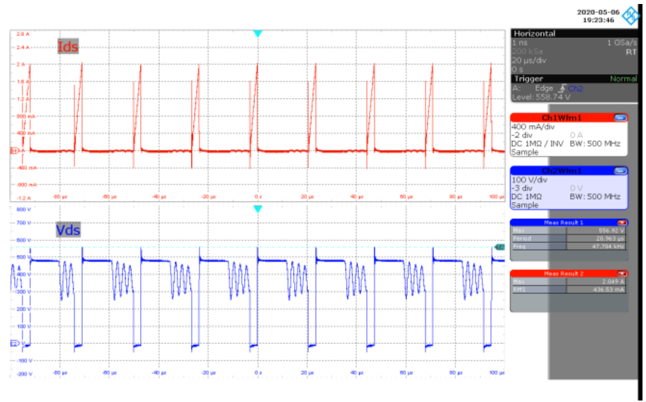

Figure 109 – Primary Drain Voltage and Current.
265 VAC, 15.0 V, 3 A Load (557 V_{MAX}).
CH4: V_{DRAIN}, 100 V / div.
CH1: I_{DRAIN}, 0.4 A / div.
Time: 20 μs / div.

14.4.4 Output: 20 V / 3.25 A

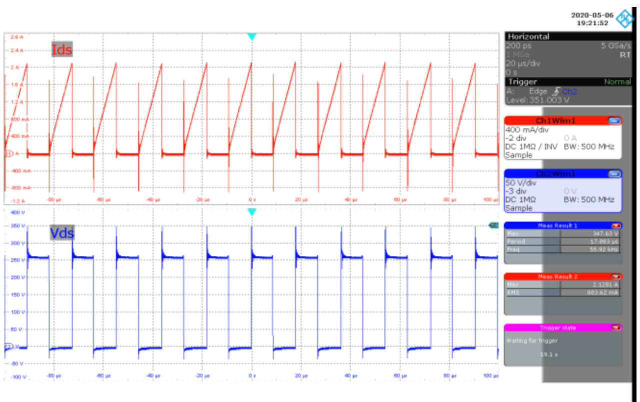

Figure 110 – Primary Drain Voltage and Current.
90 VAC, 20.0 V, 3.25 A Load (348 V_{MAX}).
CH4: V_{DRAIN}, 50 V / div.
CH1: I_{DRAIN}, 0.4 A / div.
Time: 20 μs / div.

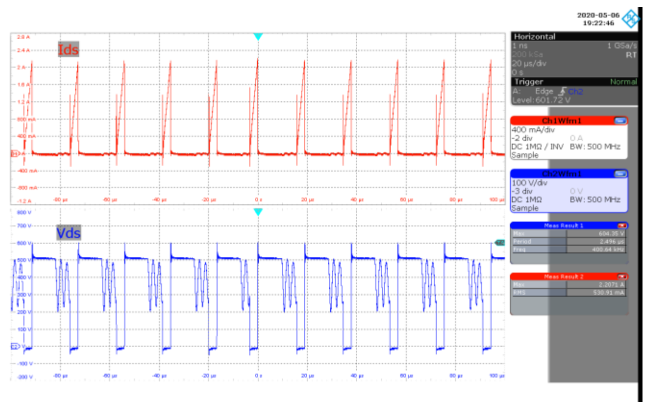

Figure 111 – Primary Drain Voltage and Current.
265 VAC, 20.0 V, 3.25 A Load (604 V_{MAX}).
CH4: V_{DRAIN}, 100 V / div.
CH1: I_{DRAIN}, 0.4 A / div.
Time: 20 μs / div.

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14.5 ***SR FET Drain Voltage and Current (Steady-State)***

14.5.1 Output: 5 V / 3 A

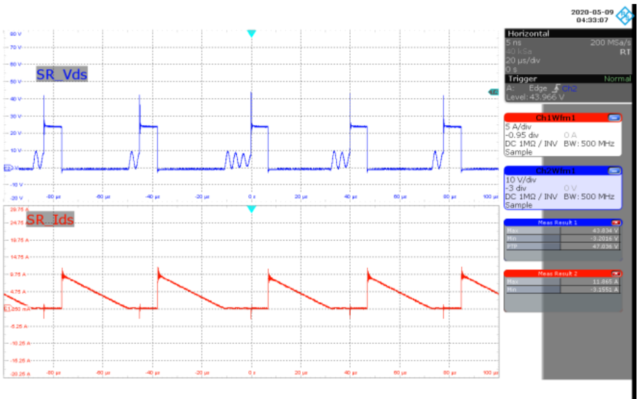

Figure 112 – SR FET Drain Voltage and Current.
90 VAC, 5.0 V, 3 A Load (43.8 V_{MAX}).
CH2: $V_{DRAIN(SR)}$, 10 V / div.
CH1: $I_{DRAIN(SR)}$, 5 A / div.
Time: 20 µs / div.

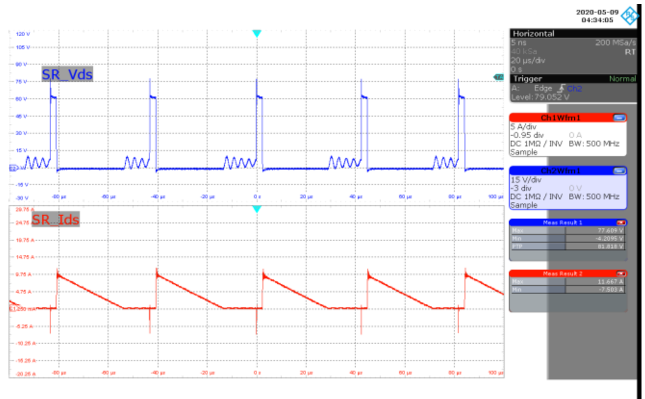

Figure 113 – SR FET Drain Voltage and Current.
265 VAC, 5.0 V, 3 A Load (77.6 V_{MAX}).
CH2: $V_{DRAIN(SR)}$, 15 V / div.
CH1: $I_{DRAIN(SR)}$, 5 A / div.
Time: 20 µs / div.

14.5.2 Output: 9 V / 3 A

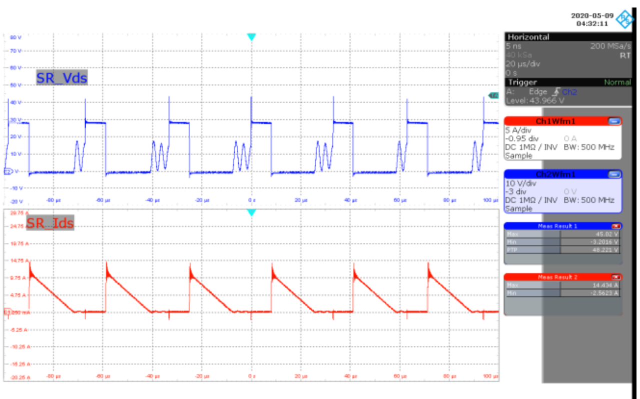

Figure 114 – SR FET Drain Voltage and Current.
90 VAC, 9.0 V, 3 A Load (45.0 V_{MAX}).
CH2: $V_{DRAIN(SR)}$, 10 V / div.
CH1: $I_{DRAIN(SR)}$, 5 A / div.
Time: 20 µs / div.

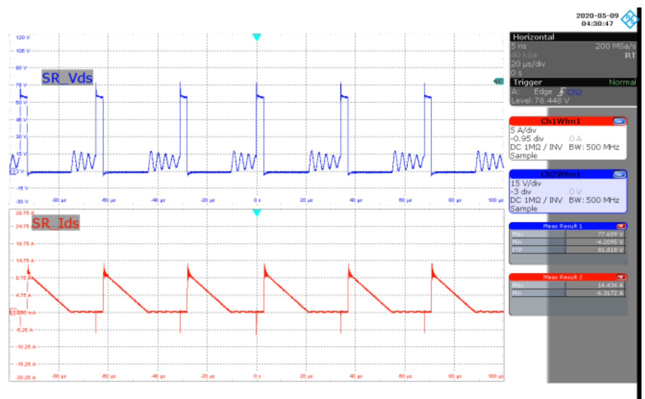

Figure 115 – SR FET Drain Voltage and Current.
265 VAC, 5.0 V, 3 A Load (77.6 V_{MAX}).
CH2: $V_{DRAIN(SR)}$, 15 V / div.
CH1: $I_{DRAIN(SR)}$, 5 A / div.
Time: 20 µs / div.

14.5.3 Output: 15 V / 3 A

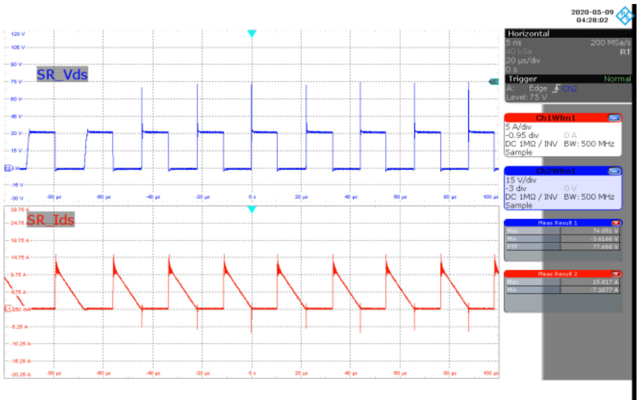

Figure 116 – SR FET Drain Voltage and Current.
90 VAC, 15.0 V, 3 A Load (74.0 V_{MAX}).
CH2: $V_{DRAIN(SR)}$, 15 V / div.
CH1: $I_{DRAIN(SR)}$, 5 A / div.
Time: 20 μs / div.

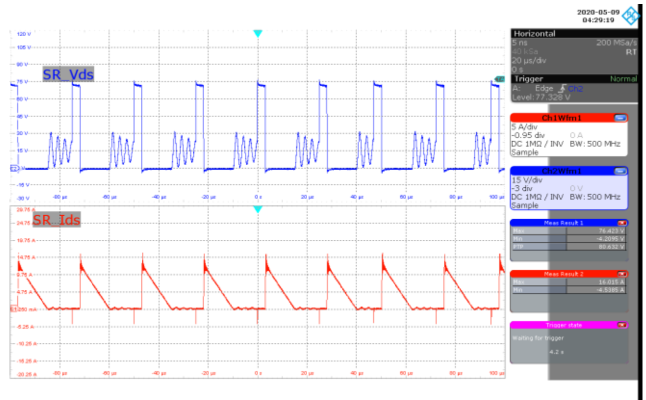

Figure 117 – SR FET Drain Voltage and Current.
265 VAC, 15.0 V, 3 A Load (76.4 V_{MAX}).
CH2: $V_{DRAIN(SR)}$, 15 V / div.
CH1: $I_{DRAIN(SR)}$, 5 A / div.
Time: 20 μs / div.

14.5.4 Output: 20 V / 3.25 A

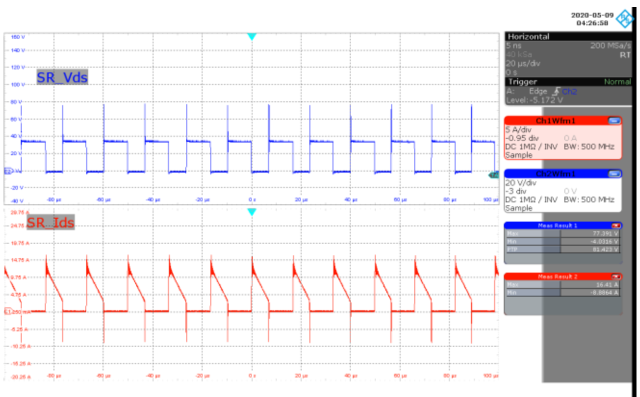

Figure 118 – SR FET Drain Voltage and Current.
90 VAC, 20.0 V, 3 A Load (77.3 V_{MAX}).
CH2: $V_{DRAIN(SR)}$, 20 V / div.
CH1: $I_{DRAIN(SR)}$, 5 A / div.
Time: 20 μs / div.

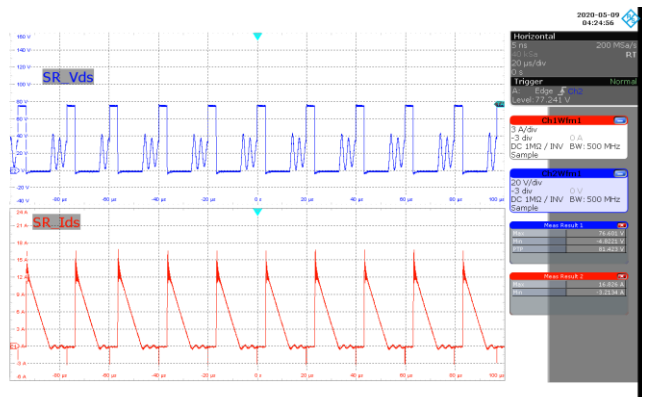

Figure 119 – SR FET Drain Voltage and Current.
265 VAC, 20.0 V, 3 A Load (76.6 V_{MAX}).
CH2: $V_{DRAIN(SR)}$, 20 V / div.
CH1: $I_{DRAIN(SR)}$, 3 A / div.
Time: 20 μs / div.

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14.6 *MinE-CAP HV Capacitor, LV Capacitor and MinE-CAP Switch Waveforms (Steady-State)*

14.6.1 Output: 5 V / 3 A

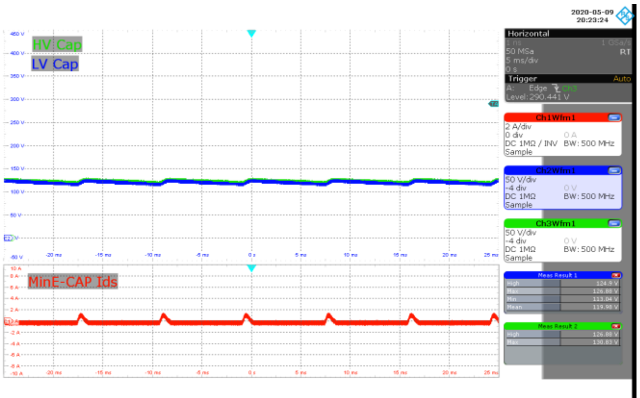

Figure 120 – MinE-CAP Steady-state Waveforms.
90 VAC, 5 V, 3 A Load.
CH1: $I_{DRAIN(MinE\text{-}CAP)}$, 2 A / div.
CH2: $V_{CLV(MinE\text{-}CAP)}$, 50 V / div.
CH3: $V_{CHV(MinE\text{-}CAP)}$, 50 V / div.
Time: 5 ms / div.

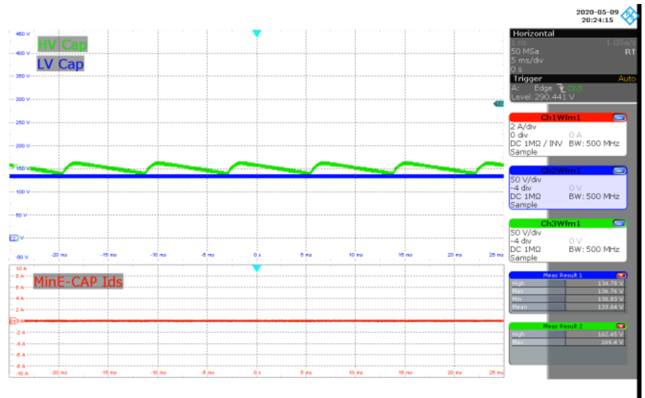

Figure 121 – MinE-CAP Steady-state Waveforms.
115 VAC, 5 V, 3 A Load.
CH1: $I_{DRAIN(MinE\text{-}CAP)}$, 2 A / div.
CH2: $V_{CLV(MinE\text{-}CAP)}$, 50 V / div.
CH3: $V_{CHV(MinE\text{-}CAP)}$, 50 V / div.
Time: 5 ms / div.

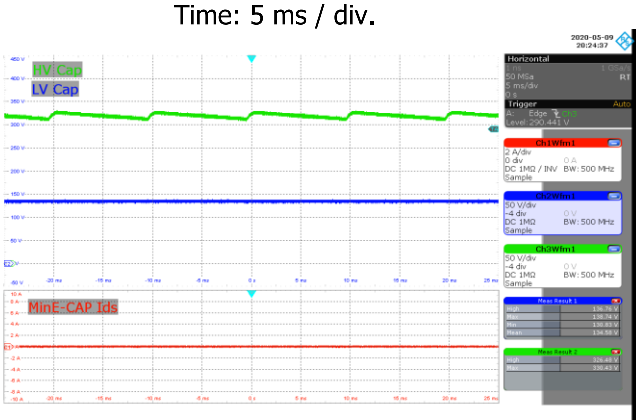

Figure 122 – MinE-CAP Steady-state Waveforms.
230 VAC, 5 V, 3 A Load.
CH1: $I_{DRAIN(MinE\text{-}CAP)}$, 2 A / div.
CH2: $V_{CLV(MinE\text{-}CAP)}$, 50 V / div.
CH3: $V_{CHV(MinE\text{-}CAP)}$, 50 V / div.
Time: 5 ms / div.

14.6.2 Output: 9 V / 3 A

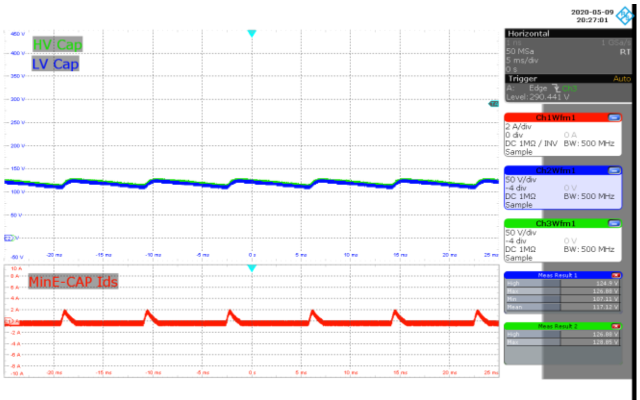

Figure 123 – MinE-CAP Step-Load Response.
90 VAC, 9 V, 3 A Load.
CH1: $I_{DRAIN(MinE-CAP)}$, 2 A / div.
CH2: $V_{CLV(MinE-CAP)}$, 50 V / div.
CH3: $V_{CHV(MinE-CAP)}$, 50 V / div.
Time: 5 ms / div.

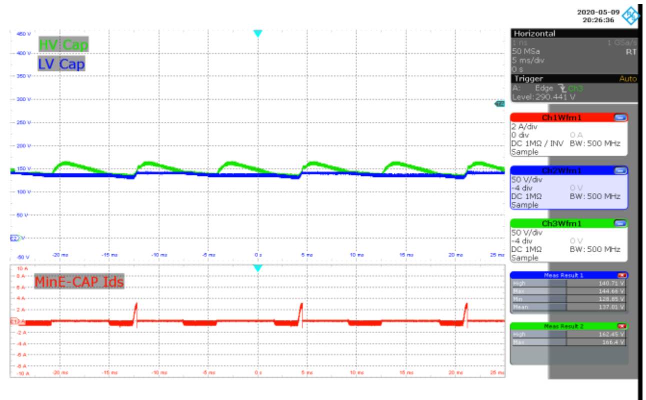

Figure 124 – MinE-CAP Start-up Active Charge.
115 VAC, 9 V, 3 A Load.
CH1: $I_{DRAIN(MinE-CAP)}$, 2 A / div.
CH2: $V_{CLV(MinE-CAP)}$, 50 V / div.
CH3: $V_{CHV(MinE-CAP)}$, 50 V / div.
Time: 5 ms / div.

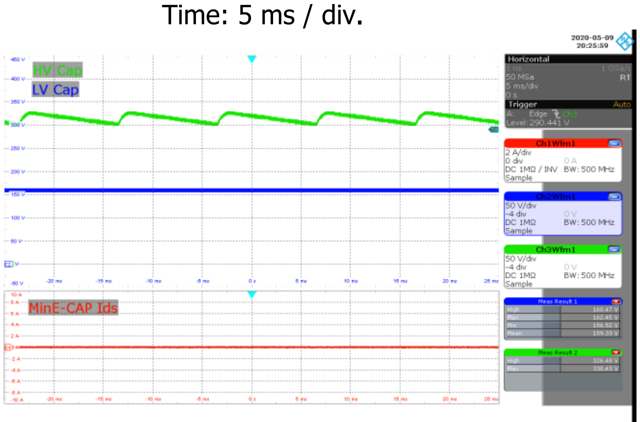

Figure 125 – MinE-CAP Start-up Active Charge.
230 VAC, 9 V, 3 A Load.
CH1: $I_{DRAIN(MinE-CAP)}$, 2 A / div.
CH2: $V_{CLV(MinE-CAP)}$, 50 V / div.
CH3: $V_{CHV(MinE-CAP)}$, 50 V / div.
Time: 5 ms / div.

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14.6.3 Output: 15 V / 3 A

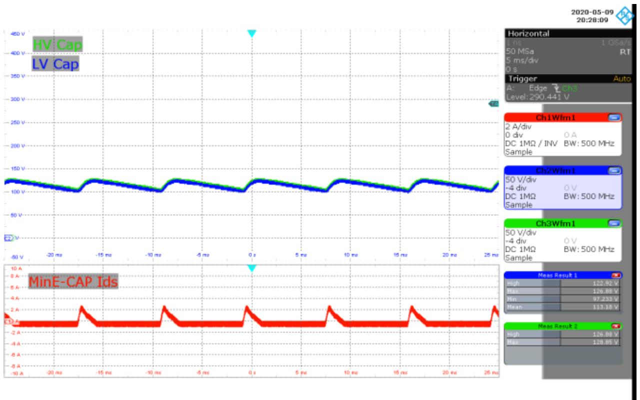

Figure 126 – MinE-CAP Step-Load Response.
90 VAC, 15 V, 3 A Load.
CH1: $I_{DRAIN(MinE-CAP)}$, 2 A / div.
CH2: $V_{CLV(MinE-CAP)}$, 50 V / div.
CH3: $V_{CHV(MinE-CAP)}$, 50 V / div.
Time: 5 ms / div.

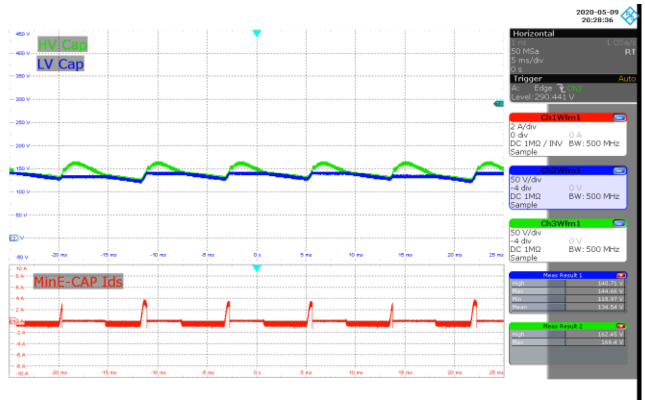

Figure 127 – MinE-CAP Start-up Active Charge.
115 VAC, 15 V, 3 A Load.
CH1: $I_{DRAIN(MinE-CAP)}$, 2 A / div.
CH2: $V_{CLV(MinE-CAP)}$, 50 V / div.
CH3: $V_{CHV(MinE-CAP)}$, 50 V / div.
Time: 5 ms / div.

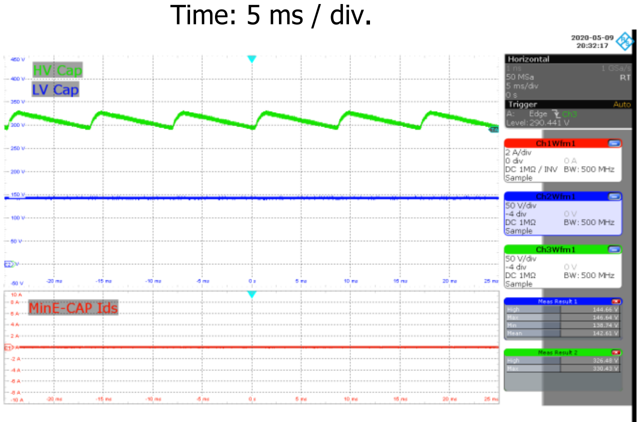

Figure 128 – MinE-CAP Start-up Active Charge.
230 VAC, 15 V, 3 A Load.
CH1: $I_{DRAIN(MinE-CAP)}$, 2 A / div.
CH2: $V_{CLV(MinE-CAP)}$, 50 V / div.
CH3: $V_{CHV(MinE-CAP)}$, 50 V / div.
Time: 5 ms / div.

15 Output Ripple Measurements

15.1 *Ripple Measurement Technique*

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 47 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

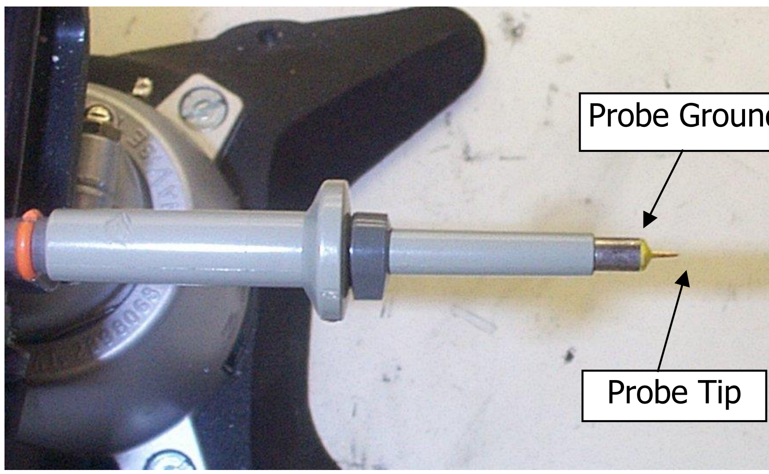

Figure 129 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

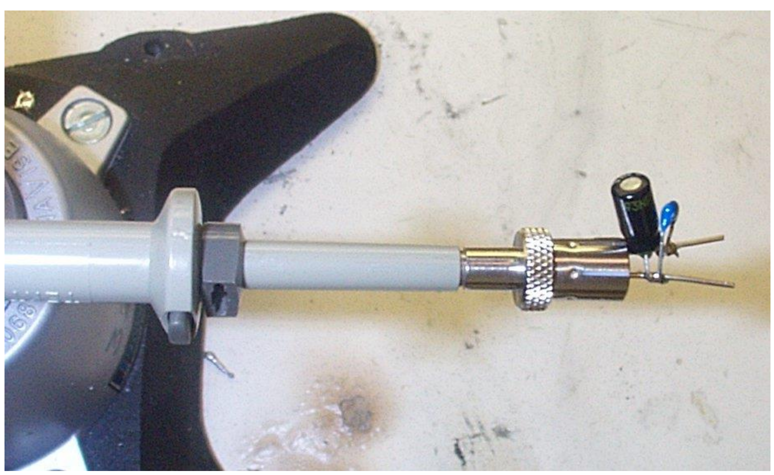

Figure 130 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

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15.2 ***Output Voltage Ripple Waveforms***

Note 1: Output voltages captured at the end of 100 mΩ cable
2: Measurements taken at room temperature (approximately 24 °C)

15.2.1 Output: 5 V / 3 A

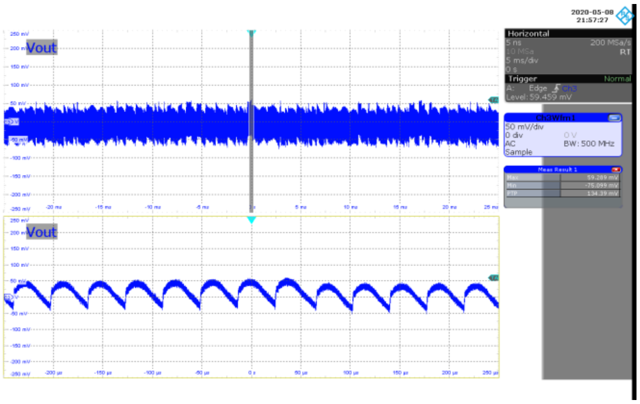

Figure 131 – Output Voltage Ripple.
90 VAC, 5.0 V, 3 A Load (134 mV_{PP}).
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 µs / div. Zoom).

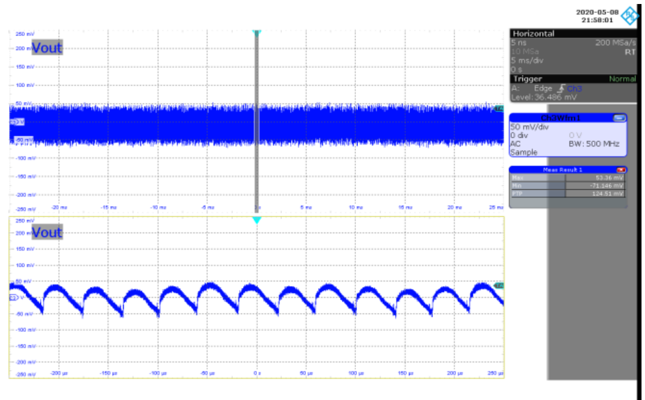

Figure 132 – Output Voltage Ripple.
265 VAC, 5.0 V, 3 A Load (124 mV_{PP}).
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 µs / div. Zoom).

15.2.2 Output: 9 V / 3 A

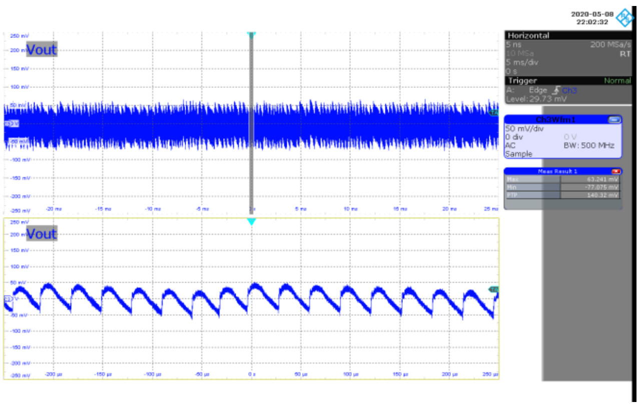

Figure 133 – Output Voltage Ripple.
90 VAC, 9.0 V, 3 A Load (140 mV_{PP}).
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 µs / div. Zoom).

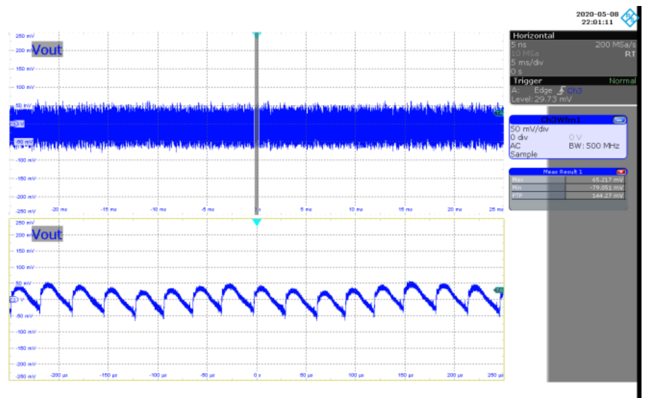

Figure 134 – Output Voltage Ripple.
265 VAC, 9.0 V, 3 A Load (144 mV_{PP}).
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 µs / div. Zoom).

15.2.3 Output: 15 V / 3 A

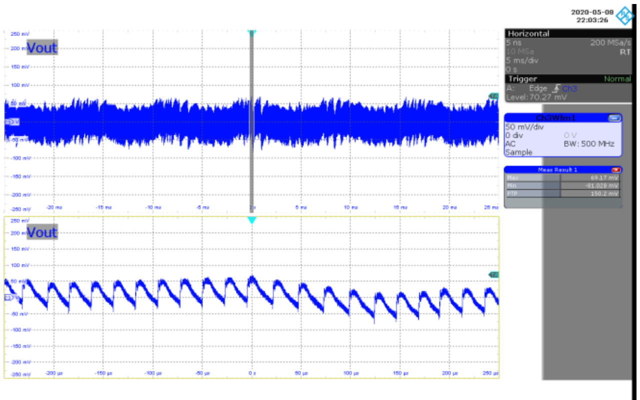

Figure 135 – Output Voltage Ripple.
90 VAC, 15.0 V, 3 A Load (150 mV_{PP}).
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 µs / div. Zoom).

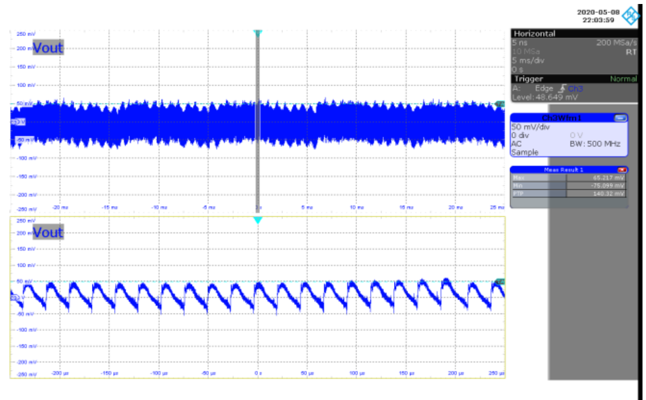

Figure 136 – Output Voltage Ripple.
265 VAC, 5.0 V, 3 A Load (140 mV_{PP}).
CH1: $V_{DRAIN(SR)}$, 50 mV / div.
Time: 10 µs / div.

15.2.4 Output: 20 V / 3.25 A

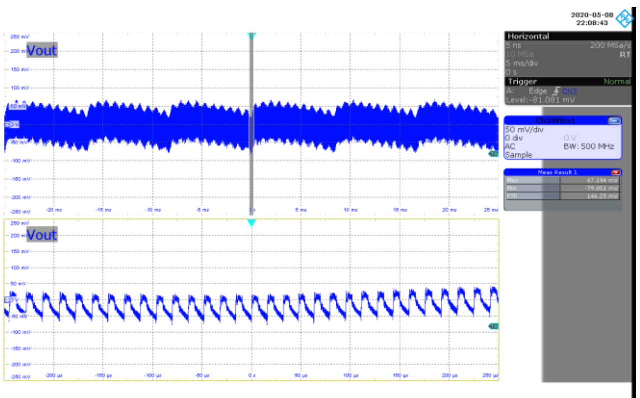

Figure 137 – Output Voltage Ripple.
90 VAC, 20.0 V, 3.25A Load (146 mV_{PP}).
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 µs / div. Zoom).

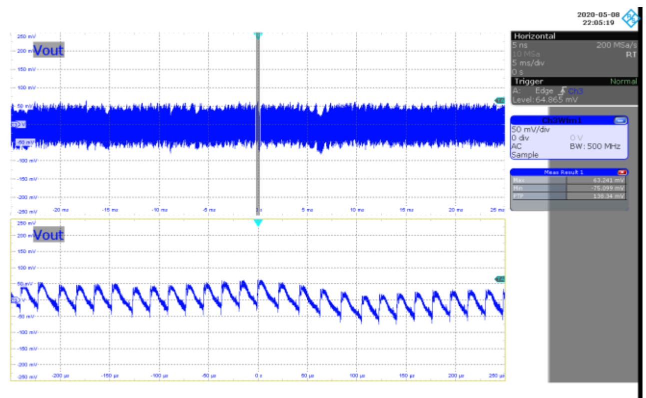

Figure 138 – Output Voltage Ripple.
265 VAC, 20.0 V, 3.25 A Load (138 mV_{PP}).
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 µs / div. Zoom).

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15.3 ***Output Voltage Ripple Amplitude vs. Load***

15.3.1 Output: 5 V / 3 A

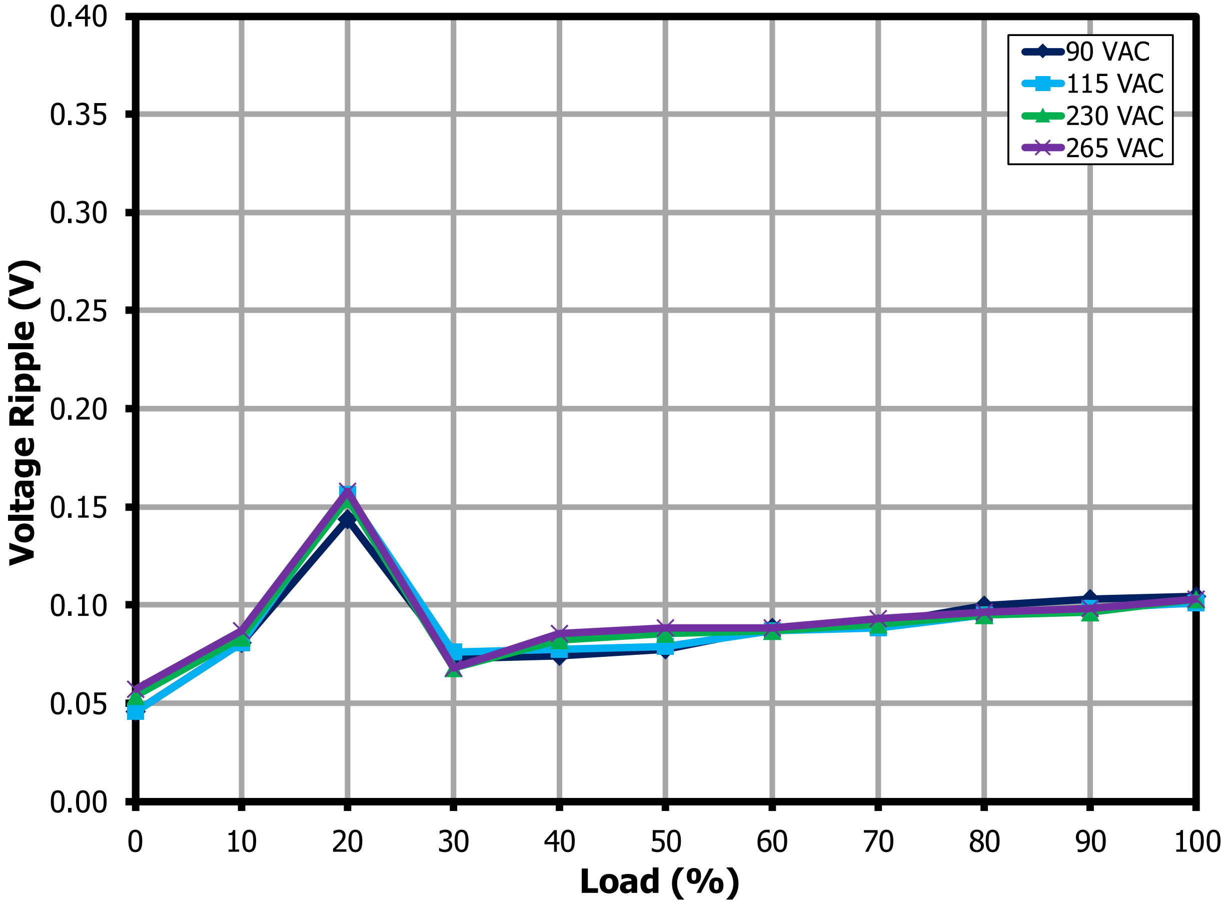

Figure 139 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 5 V Output.

15.3.2 Output: 9 V / 3 A

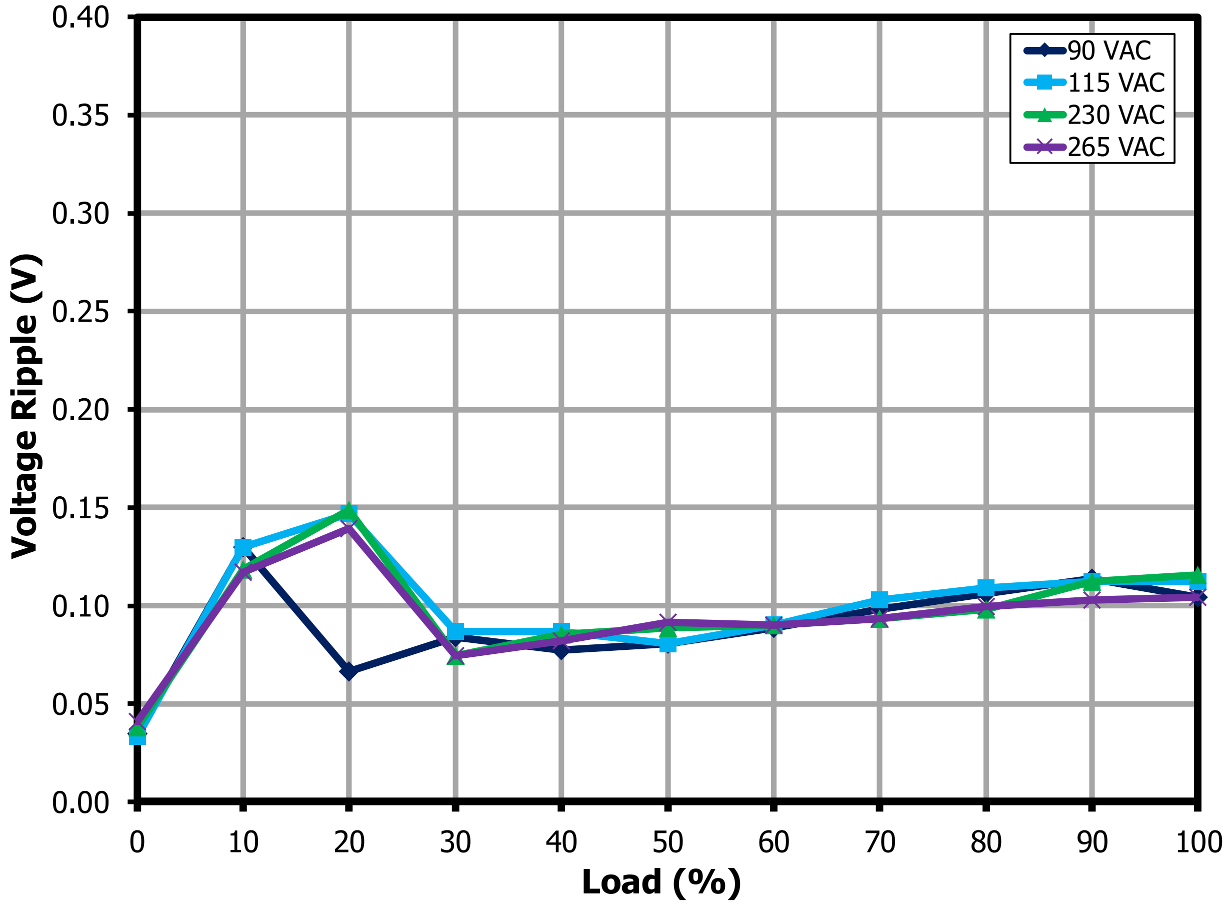

Figure 140 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 9 V Output.

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15.3.3 Output: 15 V / 3 A

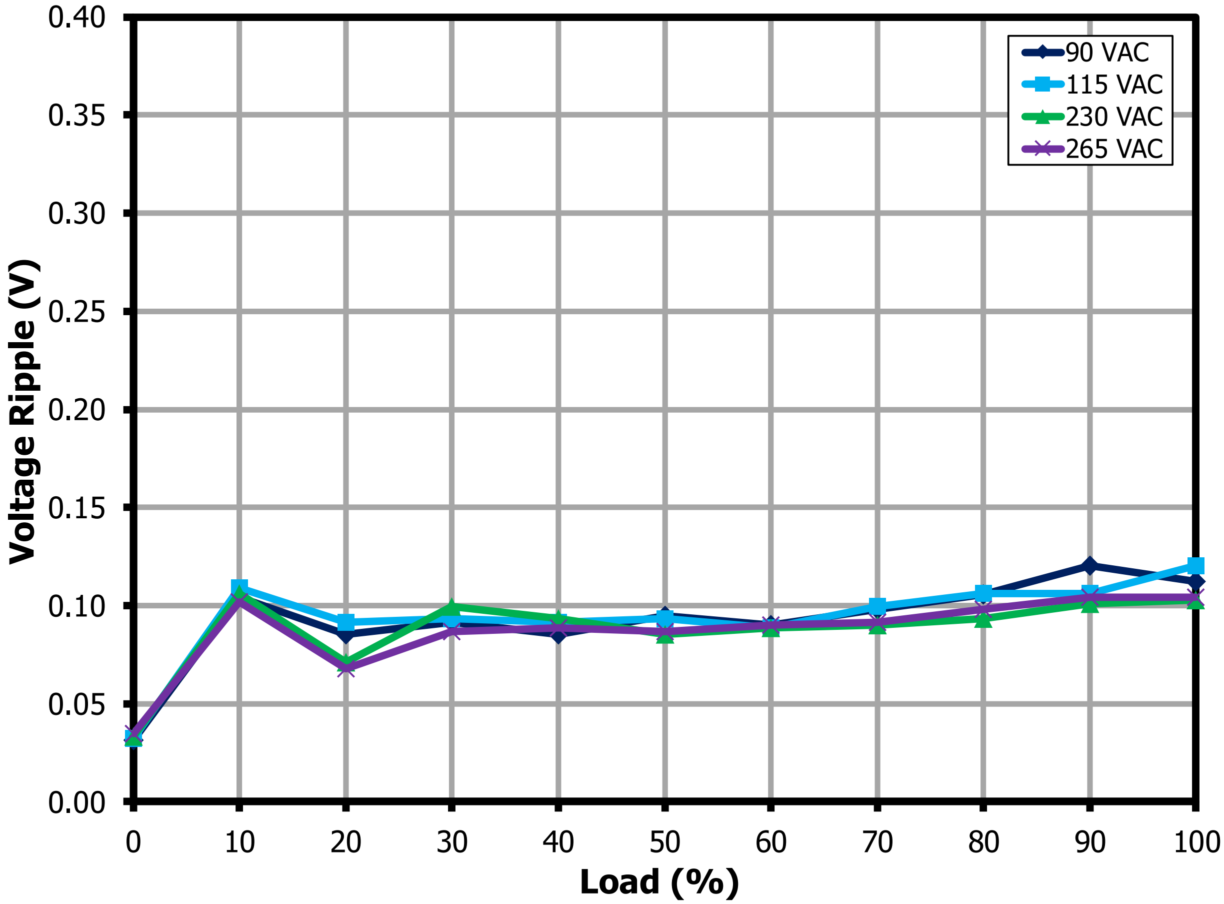

Figure 141 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 15 V Output.

15.3.4 Output: 20 V / 3.25 A

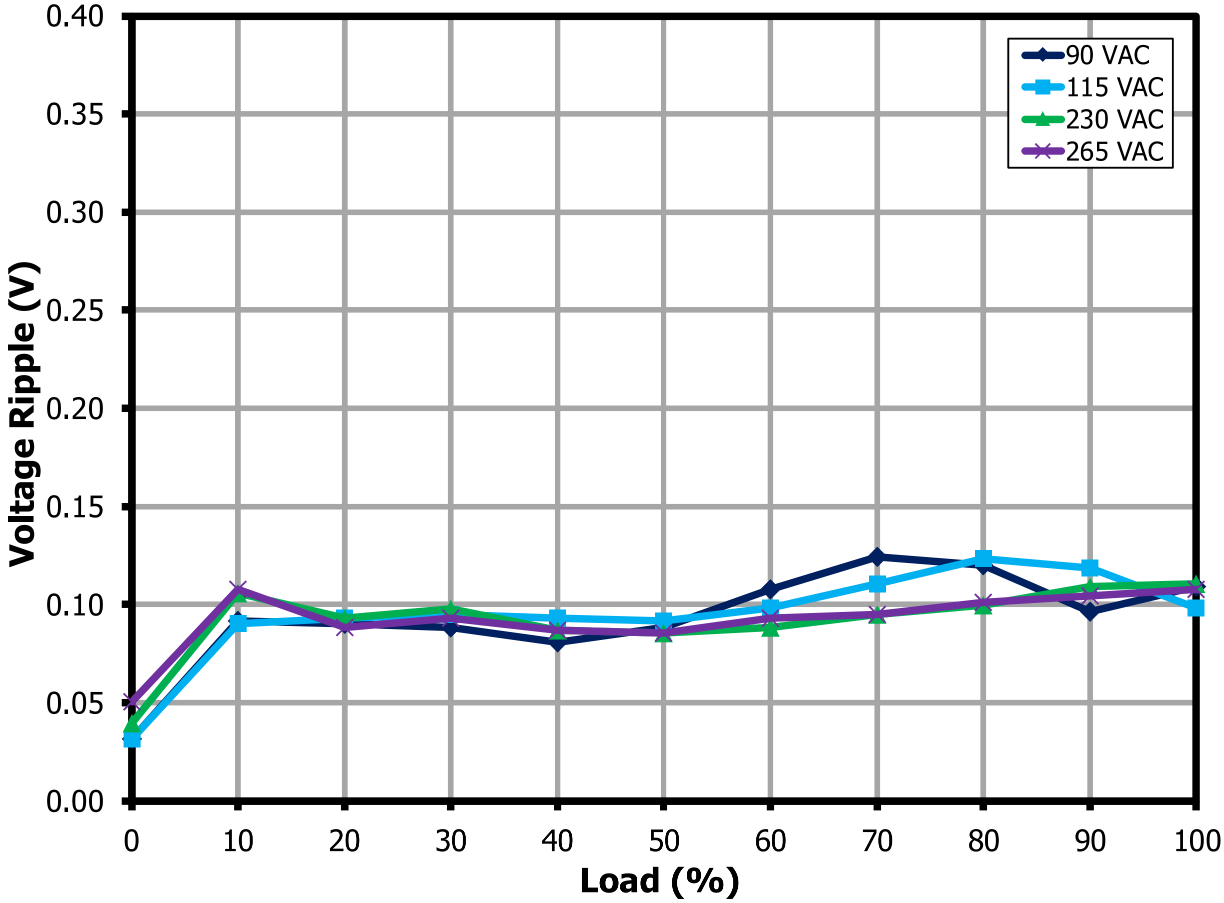

Figure 142 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 20 V Output.

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16 CV/CC Profile

Note: 1. Voltages measured on the PCB end.
2. Positive slope in CC region is per the guidelines of USB PD3.0 PPS specification.

16.1 *Output: 21 V / 3 A*

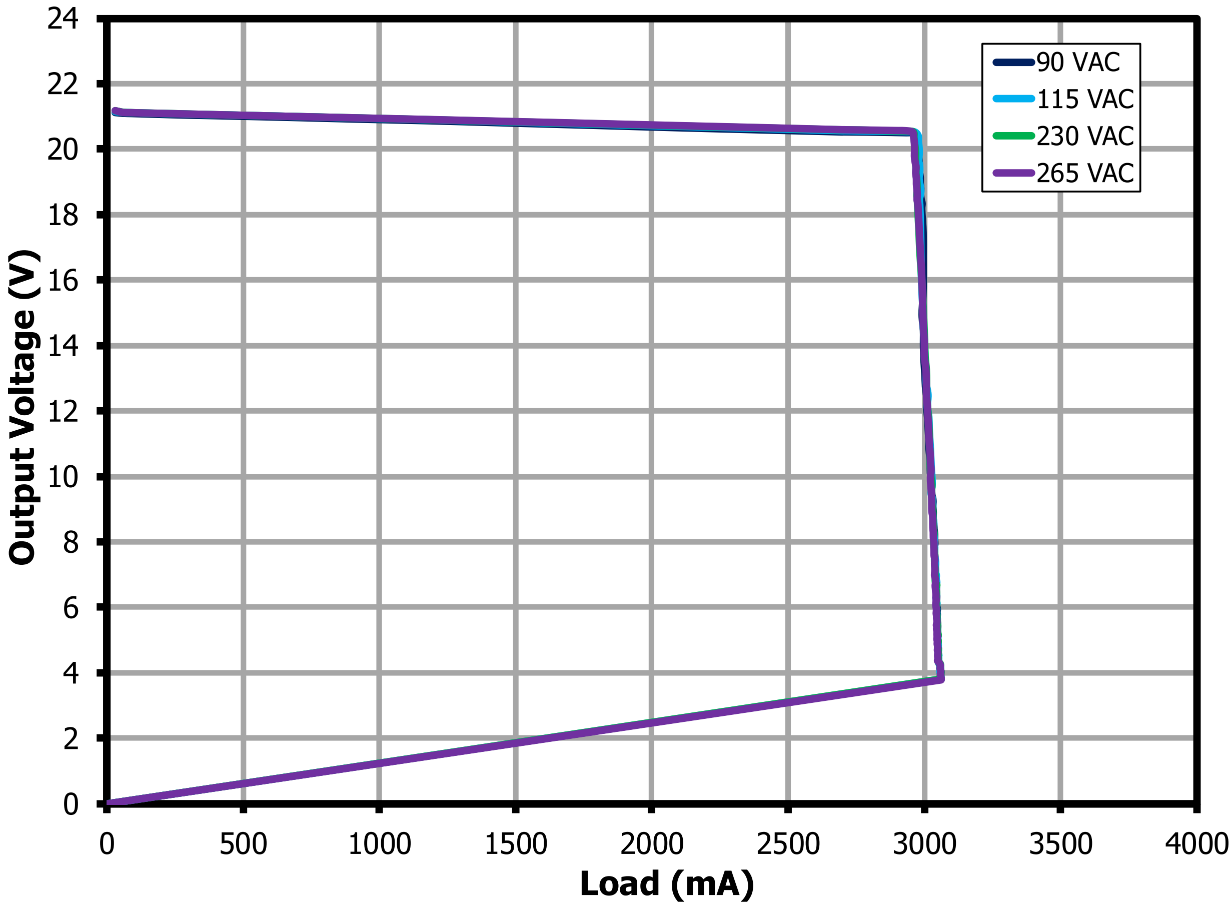
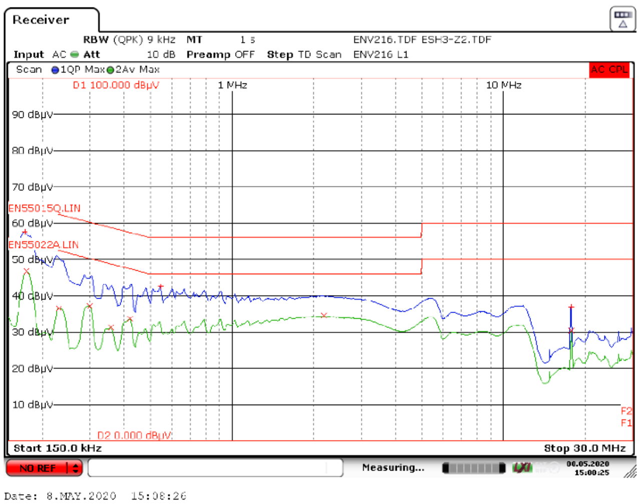


Figure 143 – CV/CC Profile for 20 V, 3.25 A Output.

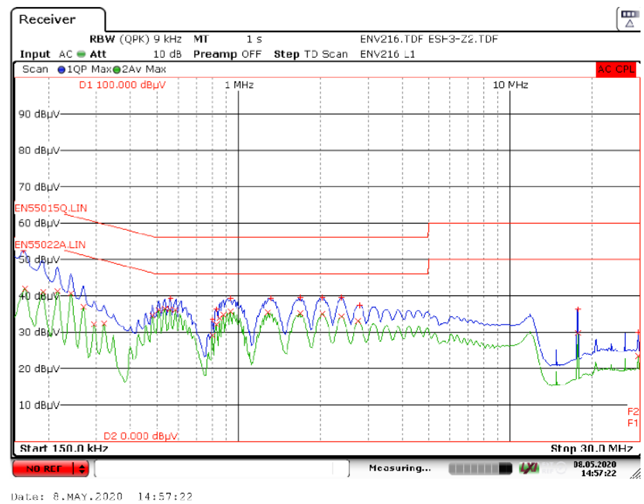
17 Conducted EMI

17.1 *Floating Ground (QPK / AV)*

17.1.1 Output: 5 V / 3 A

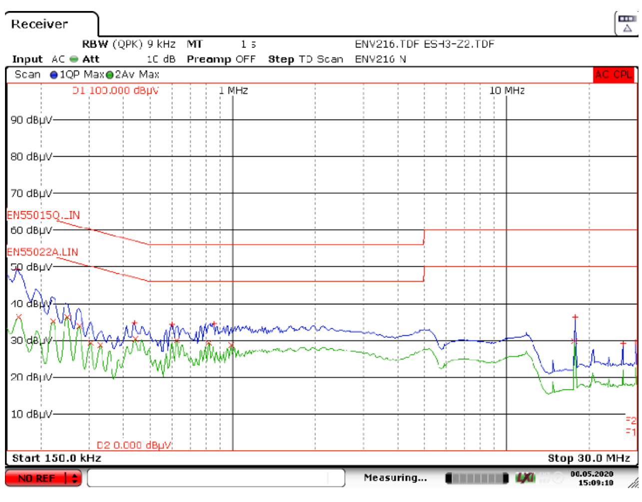


115 VAC.

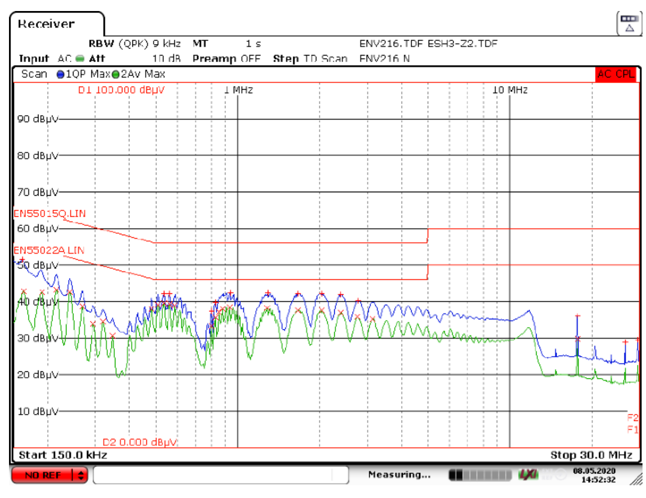


230 VAC.

Figure 144 – Floating Ground EMI, 5 V / 3 A Load [Line Scan].



115 VAC.



230 VAC.

Figure 145 – Floating Ground EMI, 5 V / 3 A Load [Neutral Scan].

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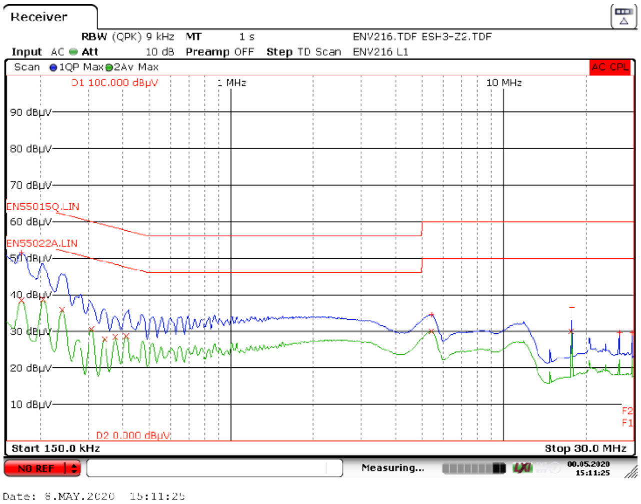
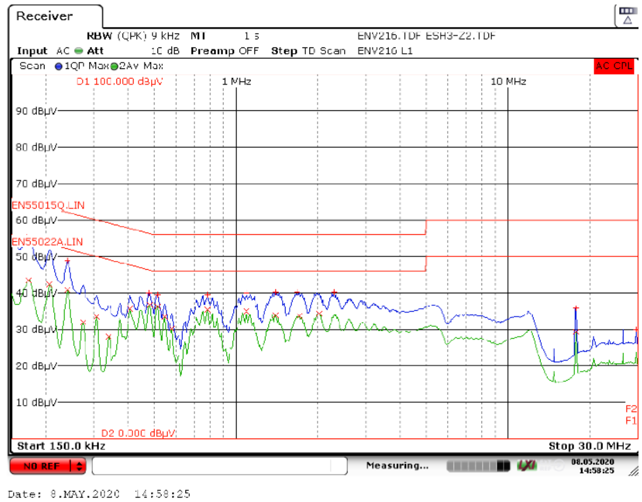
17.1.2 Output: 9 V / 3 A

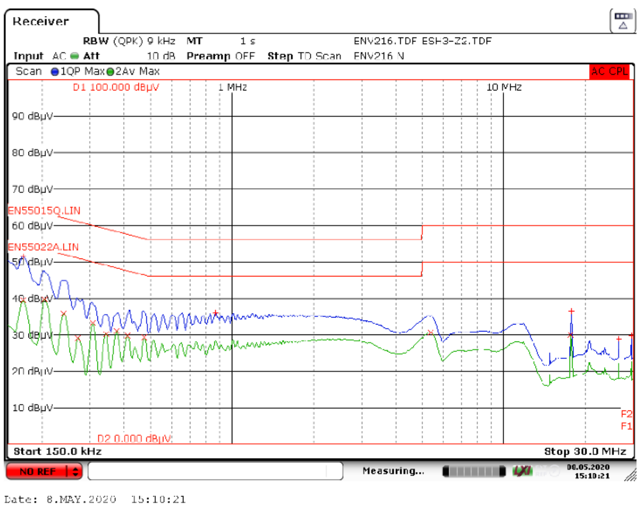


115 VAC.

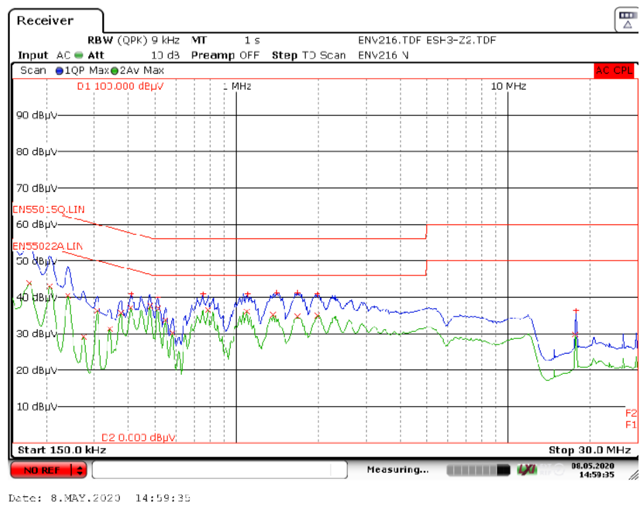


230 VAC.

Figure 146 – Floating Ground EMI, 9 V / 3 A Load [Line Scan].



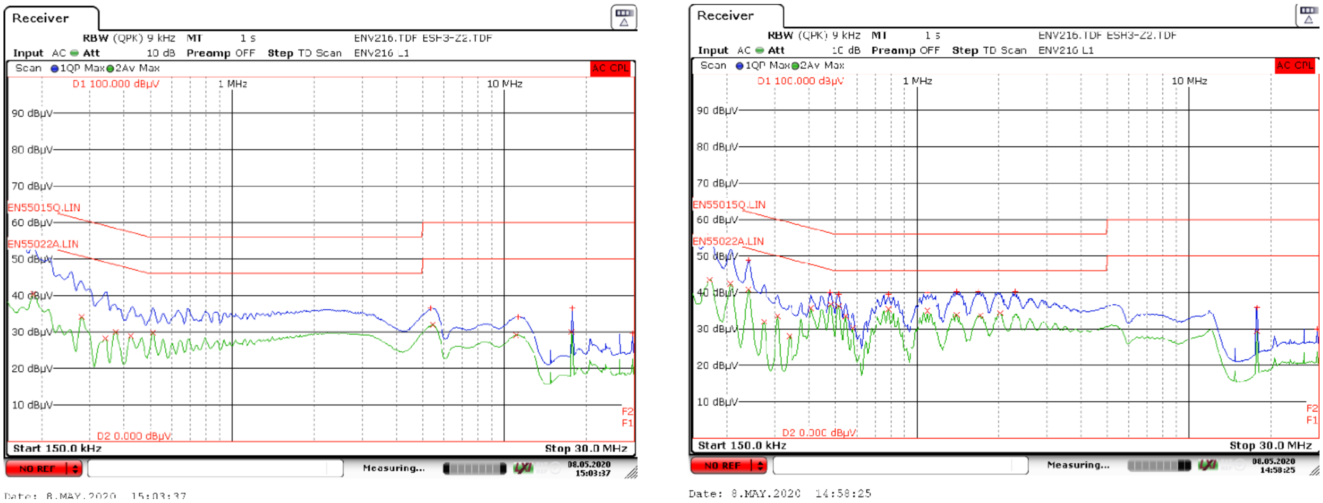
115 VAC.



230 VAC.

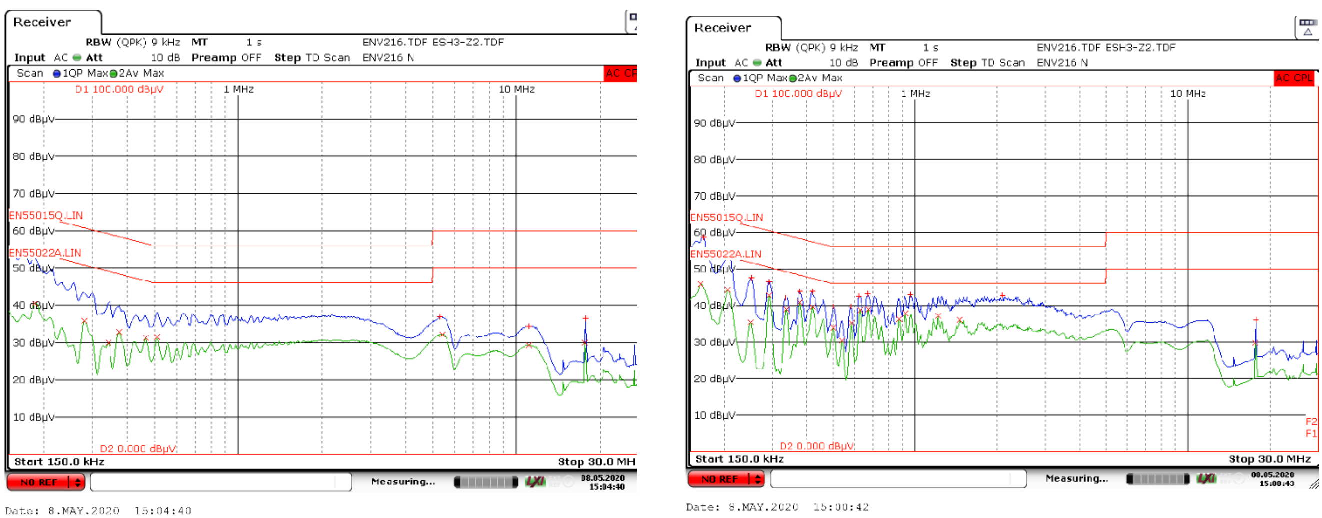
Figure 147 – Floating Ground EMI, 9 V / 3 A Load [Neutral Scan].

17.1.3 Output: 15 V / 3 A



115 VAC. 230 VAC.

Figure 148 – Floating Ground EMI, 15 V / 3 A Load [Line Scan].



115 VAC. 230 VAC.

Figure 149 – Floating Ground EMI, 15 V / 3 A Load [Neutral Scan].

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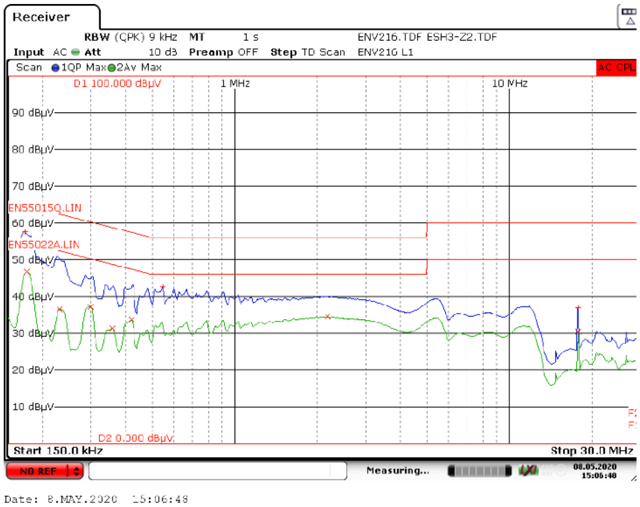
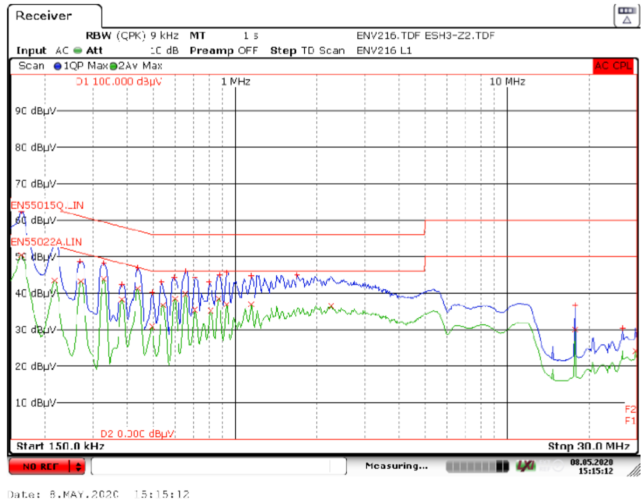
17.1.4 Output: 20 V / 3.25 A

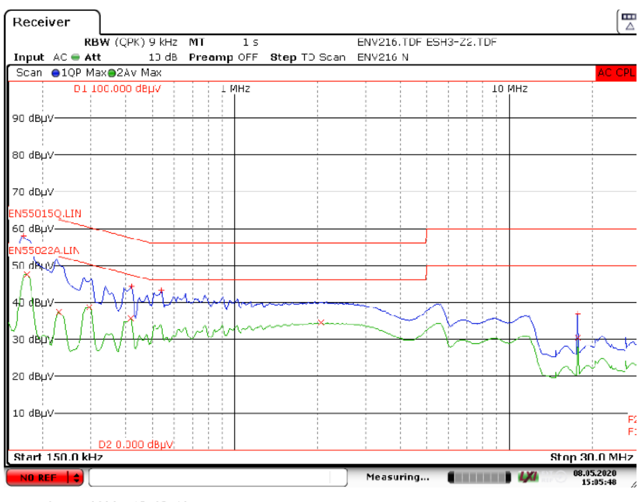


115 VAC.

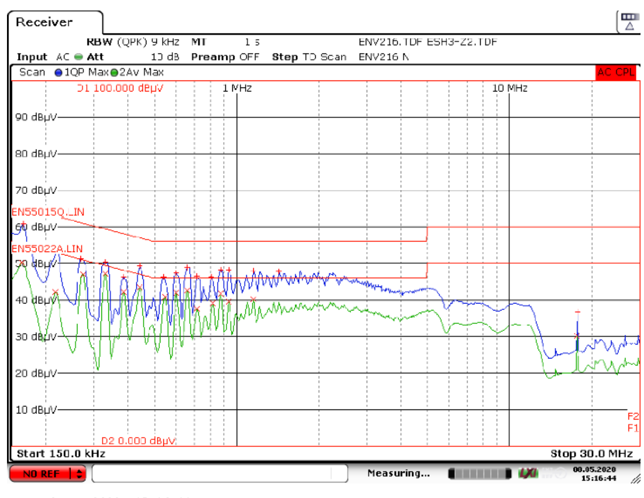


230 VAC.

Figure 150 – Floating Ground EMI, 20 V / 3.25 A Load [Line Scan].



115 VAC.



230 VAC.

Figure 151 – Floating Ground EMI, 20 V / 3.25 A Load [Neutral Scan].

18 Combination Wave Surge

The unit was subjected to ±1000 V differential mode and ±2000 V common mode combination wave surge at several line phase angles with 10 strikes for each condition.

18.1 *Differential Mode Surge (L1 to L2), 230 VAC Input*

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 20 V / 0 A (Pass/Fail)	Test Result 20 V / 3 A (Pass/Fail)
+1000	L1 to L2	0	Pass	Pass
-1000	L1 to L2	0	Pass	Pass
+1000	L1 to L2	90	Pass	Pass
-1000	L1 to L2	90	Pass	Pass
+1000	L1 to L2	180	Pass	Pass
-1000	L1 to L2	180	Pass	Pass
+1000	L1 to L2	270	Pass	Pass
-1000	L1 to L2	270	Pass	Pass

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19 Electrostatic Discharge

The unit was tested with ±8 kV to ±16.5 kV air discharge and ±8.8 kV contact discharge at the positive and negative nodes of the output with 10 strikes for each condition.

A test failure was defined as a temporary interruption of output, even if it is self-recoverable or needs operator intervention to recover or a complete loss of function, which is not recoverable.

19.1 *Contact Discharge, 230 VAC input*

Discharge Voltage (kV)	ESD Strike Location (End of Type-C Cable)	Test Result 20 V / 0 A	Test Result 20 V / 3.25 A
+8.8	+VOUT	Pass	Pass
	GND	Pass	Pass
-8.8	+VOUT	Pass	Pass
	GND	Pass	Pass

19.2 *Air Discharge, 230 VAC input*

Discharge Voltage (kV)	ESD Strike Location (End of Type-C Cable)	Test Result 20 V / 0 A	Test Result 20 V / 3.25 A
+8	+VOUT	Pass	Pass
	GND	Pass	Pass
-8	+VOUT	Pass	Pass
	GND	Pass	Pass
+10	+VOUT	Pass	Pass
	GND	Pass	Pass
-10	+VOUT	Pass	Pass
	GND	Pass	Pass
+12	+VOUT	Pass	Pass
	GND	Pass	Pass
-12	+VOUT	Pass	Pass
	GND	Pass	Pass
+14	+VOUT	Pass	Pass
	GND	Pass	Pass
-14	+VOUT	Pass	Pass
	GND	Pass	Pass
+16.5	+VOUT	Pass	Pass
	GND	Pass	Pass
-16.5	+VOUT	Pass	Pass
	GND	Pass	Pass

20 Audible Noise

20.1 *Audible Noise Test Set-up*

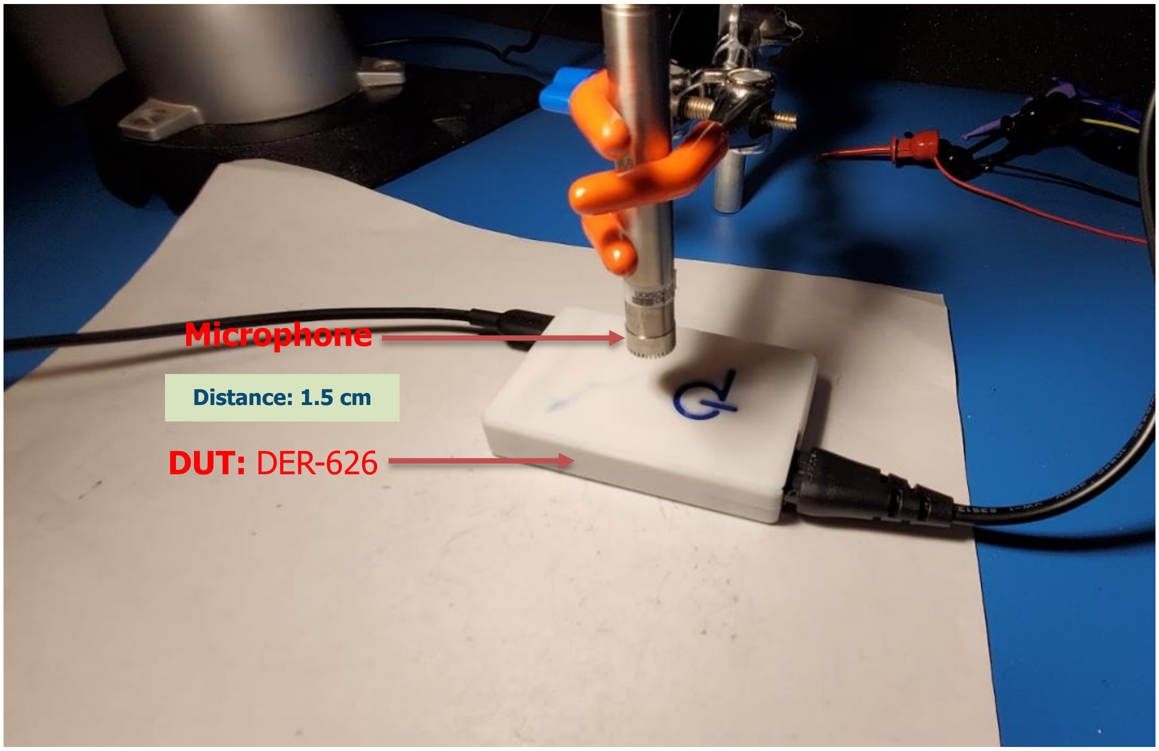

Figure 152 – Audible Noise Test Set-up.

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20.2 ***Summary of Audible Noise Test Results***

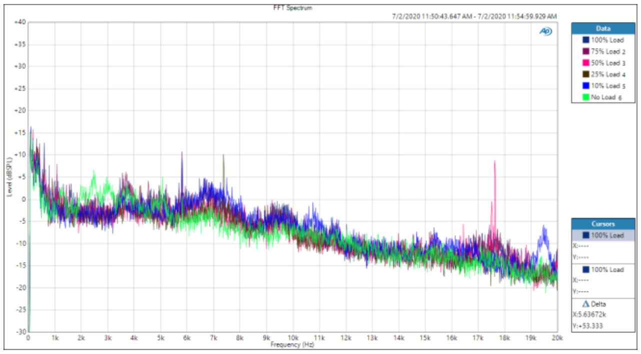
20 V / 3.25 A				
%Load	120 VAC		230 VAC	
	FSW	DBSPL	FSW	DBSPL
100	5.8 kHz	11.0 dB	5.8 kHz	16 dB
75	5.8 kHz	10.5 dB	5.8 kHz	8 dB
50	17.6 kHz	8.0 dB	5.8 kHz	7 dB
25	7.4 kHz	10.0 dB	7.2 kHz	13 dB
10	5.8 kHz	8.0 dB	8.8 kHz	8 dB
0	2.5 kHz	7.0 dB	2.5 kHz	8 dB

15 V / 3 A				
%Load	120 VAC		230 VAC	
	FSW	DBSPL	FSW	DBSPL
100	3.7 kHz	8.0 dB	3.5 kHz	6 dB
75	3.5 kHz	7.0 dB	7.5 kHz	10 dB
50	5.8 kHz	4.0 dB	5.8 kHz	3 dB
25	4.5 kHz	7.0 dB	11.5 kHz	3 dB
10	7.8 kHz	3.0 dB	5.8 kHz	3 dB
0	1.3 kHz	7.0 dB	2.4 kHz	6 dB

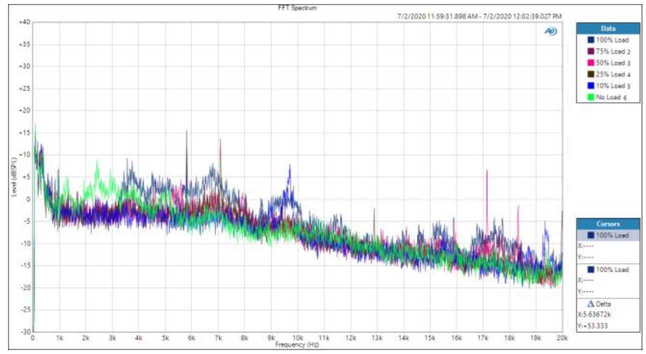
9 V / 3 A				
%Load	120 VAC		230 VAC	
	FSW	DBSPL	FSW	DBSPL
100	6.7 kHz	3.0 dB	15.7 kHz	11 dB
75	6.8 kHz	2.5 dB	13.8 kHz	6 dB
50	6.3 kHz	9.0 dB	12.0 kHz	0 dB
25	5.8 kHz	4.0 dB	9.8 kHz	9 dB
10	13.2 kHz	5.0 dB	4.5 kHz	4 dB
0	1.3 kHz	3.0 dB	2.5 kHz	4 dB

5 V / 3 A				
%Load	120 VAC		230 VAC	
	FSW	DBSPL	FSW	DBSPL
100	6.8 kHz	3.0 dB	6.8 kHz	4 dB
75	6.8 kHz	2.0 dB	6.8 kHz	2 dB
50	4.0 kHz	0.0 dB	19.8 kHz	7 dB
25	15.8 kHz	14.0 dB	4.2 kHz	10 dB
10	3.8 kHz	12.0 dB	6.5 kHz	9 dB
0	3.0 kHz	2.0 dB	2.5 kHz	3 dB

20.3 *Audible Noise Plots 0 to 100% Load*

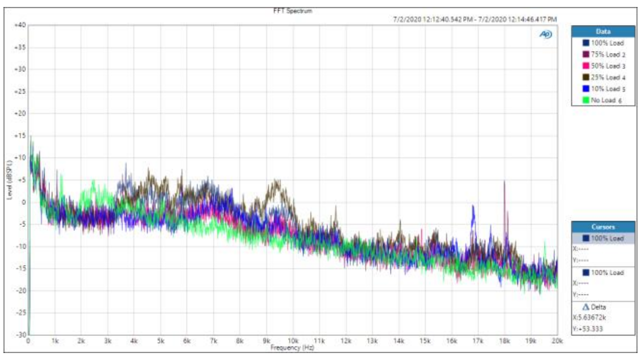


115 VAC.

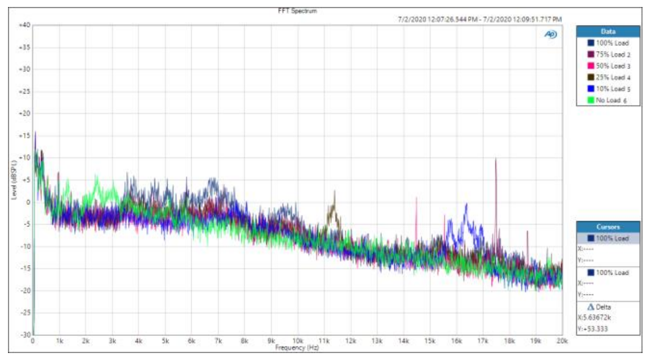


230 VAC.

Figure 153 – Audible Noise Scan 20 V 3.25 A, 0 to 100% Load.

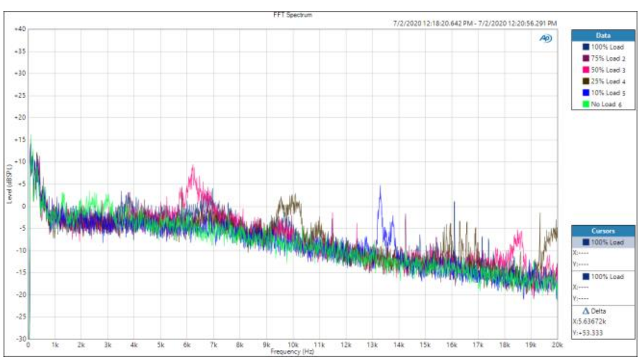


115 VAC.

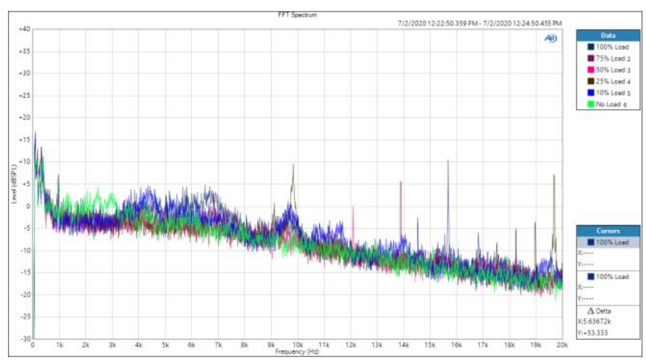


230 VAC.

Figure 154 – Audible Noise Scan 15 V 3 A, 0 to 100% Load.



115 VAC.



230 VAC.

Figure 155 – Audible Noise Scan 9 V 3 A, 0 to 100% Load.

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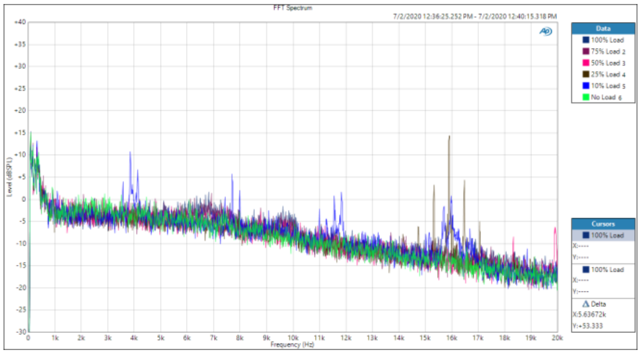
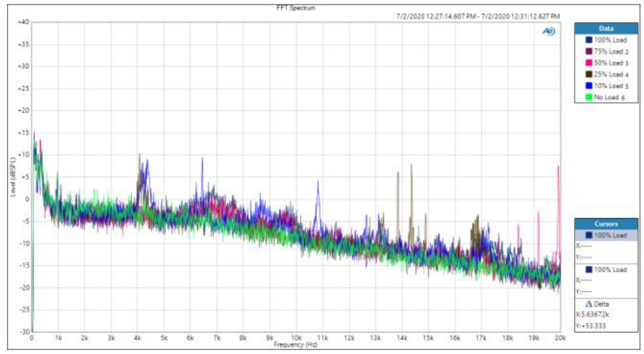


115 VAC.



230 VAC.

Figure 156 – Audible Noise Scan 5 V 3 A, 0 to 100% Load.

21 Revision History

Date	Author	Revision	Description & Changes	Reviewed
29-May-20	GC	1.0	Initial Release.	Apps & Mktg
15-Aug-20	GC	1.1	Updated assembly instructions, BOM and fabrication drawings Added audible noise test results	Apps & Mktg
05-Oct-20	KM	1.2	Finalize for Release	Apps & Mktg

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