Application Note AN-65
LYTSwitch-5 Family

Design Guide and Considerations

Introduction

The LYTSwitch™-5 family is ideal for single-stage power factor corrected constant current LED drivers for tubes, bulbs and recessed lighting up to 25 W. Each device combines a high-voltage power MOSFET, variable frequency and on-time control engine, fast start-up with soft-finish and protection functions including instantaneous line overvoltage shutdown, output short-circuit auto-restart, output overvoltage latch-off and thermal foldback with over-temperature shutdown into a single package, thus greatly reducing component count. Its internal feedback controller is capable of indirect and direct output current sensing that can be set via external programming resistor, thus eliminating the need for optocoupler, especially with isolated design applications.

The integrated 725 V power MOSFET provides a large drain voltage margin in high-line input AC applications, thus increasing reliability. A 625 V power MOSFET option is also offered to reduce cost in applications where the voltage stress on the power MOSFET is low.

Topology neutral LYTSwitch-5 operates in discontinuous conduction mode (DCM) for tight tolerance output current regulation over line input range and operating temperature, high power factor with significantly low harmonic currents via its internal control algorithm. The combination of a low-side switching topology, cooling via electronically quiet SOURCE pins, frequency jitter and DCM operation which inherently eliminates reverse current from the output diode when the power MOSFET is in OFF-state reducing high frequency noise. This allows the use of a simple and small input pi filter yet produces low EMI (note that low input capacitance reduces THD and increases PF).

Output Power Table

Product	Output Power
	90-308 VAC
LYT5225D	9 W
LYT5216D, LYT5226D	16 W
LYT5218D, LYT5228D	25 W

Table 1. LYTSwitch-5 Output Power Table. See LYTSwitch-5 data sheet for more details.

Typical Circuit Configuration

The LYTSwitch-5 device family is topology neutral that it can be used in any switching configuration such as Buck (Tapped-Buck), Buck-Boost (Tapped Buck-Boost), Boost and Flyback (Isolated and Non-Isolated) making it broadly applicable to any design requirement regardless of LED voltage string. The high level integration of LYTSwitch-5 family enables ease of design optimization both in converter and EMI sections resulting to shortened development time.

Circuit in Figures 1 and 2 show a typical low component count universal LED driver using LYTSwitch-5 in Buck and isolated Flyback configurations respectively.

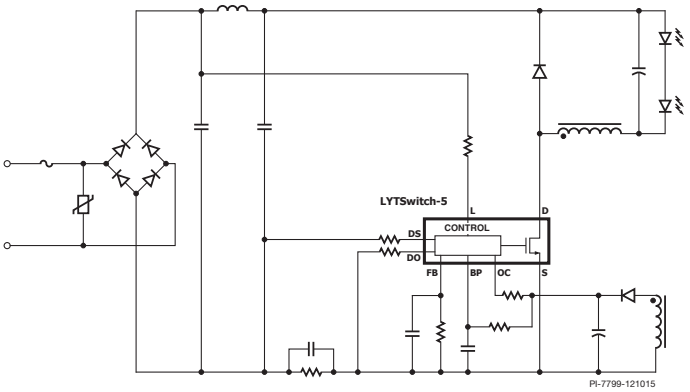


Figure 1. Low Component Count Typical Circuit Buck Topology with LYTSwitch-5 (21 external components).

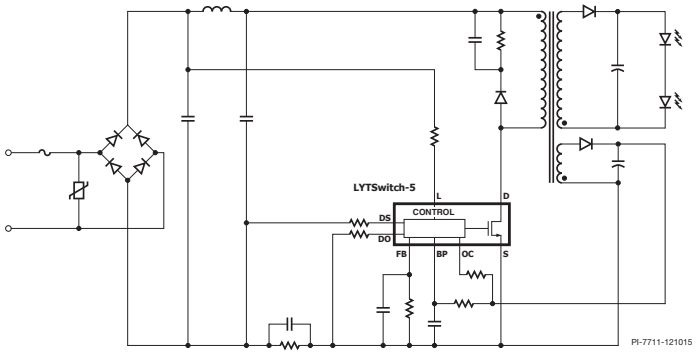


Figure 2. Low Component Count Typical Circuit Isolated Flyback Topology with LYTSwitch-5 (23 external components).

Scope

This application note is intended for users designing an AC-DC LED driver using LYTSwitch-5 family devices. A simplified step by step instruction will guide the user in selecting key components, especially in designing the magnetics necessary to quickly jump start the design process and come up with a sound prototype design. This application note refers directly to the PIXIs design spreadsheet that is a part of the PI Expert™ design software suite (https://piexpertonline.power.com/site/login).

In this application note the user may also find product Reference Design Kits (RDK) and Design Example Reports (DER) useful. These contain a prototype board, a link to an engineering report that contains complete design information including gerber for the printed circuit board (PCB) and test data and product samples. Further details on downloading PI Expert, RDKs and updates to this document can be found at Power Integrations' website www.power.com.

Choosing Switching Topology

The LYTSwitch-5 device family can be used in any switching topology configuration such as Buck (Tapped-Buck), Buck-Boost (Tapped Buck-Boost), Boost and Flyback (Isolated and Non-Isolated) making it broadly applicable to any design requirement regardless of LED voltage string. Choosing the right topology to use can be challenging at times, however using LYTSwitch-5 the designer only needs to know is the output voltage, efficiency and ATHD target in choosing the suitable topology to use. Table 2 shows a topology selection guide.

Output Voltage (V)		Recommended Topology					Remark
Low-Line/ Universal Inputs	**High-Line Inputs**	**Tapped Buck or Buck-Boost**	**Buck**	**Buck-Boost**	**Boost**	**Flyback**	
< 12	< 25	✓					Limited by maximum duty of device at minimum input voltage
13 – 60	27 - 100		✓				Minimum voltage is limited by maximum on-time of device at maximum input
> 24	> 48			✓			Maximum output voltage is limited by transistor breakdown voltage
$V_{OUT} > V_{IN}$					✓		
Any Voltage > 3						✓	
Minimum Efficiency Estimate		>80%	>87%	>85%	>90%	80%	
ATHD%		>15%	>15%	5% < × < 15%	>25%	5% < × < 15%	

Table 2. Recommended Topology Selection Guide.

Design Example

Design a 12 W non-isolated LED driver using LYTSwitch-5 having an output voltage of 75 V, output current of 160 mA, ±5% regulation tolerance with an input voltage range of 90 VAC to 264 VAC, 89% minimum efficiency, and THD <15%.

Step-by-Step Design Procedure

Referring to Table 2, a Buck-Boost topology can be suitable for this particular specification hence the corresponding PIXIs designer spreadsheet will be used. All PIXIs designer spreadsheets are available at Power Integrations website, https://piexpertonline.power.com/site/login

Step 1: Enter Application Variables

Enter: Minimum, Nominal and Maximum Input Voltages; VAC_{MIN} [C3], VAC_{NOM} [C4], VAC_{MAX} [C5], F_L [C6]

2	**ENTER APPLICATION VARIABLES**					Design Title
3	VACMIN	90.0		90.0	Volts RMS	Minimum AC line voltage.
4	VACNOM	230.0		230.0	Volts RMS	Nominal AC line voltage.
5	VACMAX	265.0		265.0	Volts RMS	Maximum AC line voltage.
6	FL			50	Hertz	AC line frequency.
7	VO_MIN			67.5	Volts DC	Guaranteed minimum VO that maintains output regulation.
8	VO	75.0		75.0	Volts DC	Worst case normal operating output voltage.
9	VO_OVP_MIN			85.3	Volts DC	Minimum Voltage at which output voltage protection may be activated.
10	IO	160.0		160.0	m-Amperes	Average output current specification.
11	EFFICIENCY	0.89		0.89	Dimensionless	Total power supply efficiency.
12	Z			0.50	Dimensionless	Loss allocation factor.
13	PO			12.00	Watts	Output power.

Figure 3. Application Variables Section of the PIXIs Design Spreadsheet.

LYTSwitch-5 is intended for wide input voltage applications. It can maintain high efficiency, high power factor, low THD and tight regulations over entire input range.

Use Table 3 as reference for the input range to a particular regional requirement.

Region	Nominal Input (VAC)	Minimum Input (VAC)	Maximum Input (VAC)	Nominal Frequency (Hz)
Japan / USA	100 / 115	85	132	50 / 60
Europe / Rest of World	230 / 240	195	264	50 / 60
Lighting in commercial buildings in USA, (208 VAC phase-to-phase)	208 / 277	177	308	60

Table 3. Standard Worldwide Input Line Voltage Ranges and Line Frequencies.

Enter: Nominal Output Voltage, V_o [C8], Output Current I_o [C10], EFFICIENCY [C11], Loss Allocation Factor, Z [C12]

In a high power factor single stage LED driver, the output will have significantly large low frequency ripple with twice the frequency of the input line, it is recommended to use a power meter when measuring the output power for accuracy. PO [E13] is calculated based on the integral product of VO [C8] and IO [C10], which is used to choose device size.

$$P_O = \int I_{O(t)} \times V_{O(t)} dt$$

LYTSwitch-5 has built-in Latching Output Overvoltage Protection, once the current exceeds the I_{OOV} threshold via the OC pin, the IC will trigger a latch to disable switching thus preventing the output from rising further. Recycling the AC supply is needed to reset this protection mode from latch-off state.

The output overvoltage is detected through the bias supply which is calculated as VO_OVP_MIN by the PIXIs. The accuracy of overvoltage set point will be dependent on the mutual inductance (M) between bias and output winding, that is the better the coupling the more accurate it gets. Therefore it is recommended to wind the bias winding close to the main winding.

For direct output voltage sensing, NS/NB = 1. Or for PIXIs calculation, enter VBIAS [C76] = VO [C8].

The minimum voltage at which output voltage protection may be activated is calculated on cell VO_OVP_MIN [E9].

$$VO_{(OVP)MIN} = (R_{OC} \times I_{OOV} + V_{OC}) \times N/NB$$

Where,

ROC: Feedback resistor connected to OC pin from the rectified bias supply. Typical resistance value is set using 100 µA OC current (IOC) based on the nominal output voltage and output current.

$$R_{OC} = (V_{BIAS} - V_{OC})/I_{OC}$$

I_{OOV}: Latching Overvoltage Current Threshold. Minimum limit at 127 µA.
V_{OC}: OC pin voltage. Typical value at 2.2 V.
N: Output winding turns.
N_B: Bias winding turns.
I_{OC}: 100 µA; default used to set the output current.

Minimum Output Voltage, VO_MIN [E7]

This calculates the minimum output voltage at which tight regulation can be maintained.

Efficiency [C11], η

Use efficiency estimate in Table 2. Once the actual unit is available enter the measured efficiency for fine tuning the output current.

$$\eta = \frac{P_O}{P_{IN}}$$

Loss Allocation Factor, Z [E12]

Allocation factor is the ratio of output and total loss. It is used in the efficiency of the DC-DC section of the converter for calculating the input power and drain current as seen by LYTSwitch-5. Typical value is 0.5.

$$Z = \frac{\text{Secondary Loss}}{\text{Total Losses}}$$

Step 2: LYTSwitch-5 Design Variables

17	**LYTSwitch-5 DESIGN VARIABLES**					
18	BREAKDOWN VOLTAGE	725		725	Volts DC	Choose between 650V and 725V.
19	GENERIC DEVICE	Auto		LYT52X6D		Chosen LYTSwitch-5 generic device.
20	ACTUAL DEVICE			LYT5226D		Chosen LYTSwitch-5 device code.
21	ILIMITMIN			1.767	Amperes	Minimum device current limit.
22	ILIMITTYP			1.900	Amperes	Typical Current Limit.
23	ILIMITMAX			2.033	Amperes	Maximum Current Limit.
24	IP_MOSFET			1.520	Amperes	Worst case peak drain current of the MOSFET.
25	TON_MIN			1.192	u-seconds	Worst case minimum on-time of the MOSFET.
26	TON_MAX			3.138	u-seconds	Worst case maximum on-time of the MOSFET.
27	IAVG_MOSFET			0.141	Amperes	Worst case average drain current of the MOSFET.
28	IRMS_MOSFET			0.301	Amperes	Worst case maximum RMS current of the MOSFET.
29	KDP			1.118	Dimensionless	Ratio between off-time of the MOSFET and on-time of the secondary diode.
30	VDRAIN			490.7	Volts DC	Estimated worst case drain voltage of the MOSFET.

Figure 4. LYTSwitch-5 Design Variables Section of PIXIs Design Spreadsheet.

The ACTUAL DEVICE [E20] will be automatically selected based on the output power calculated and input voltage. In the BREAKDOWN VOLTAGE [E18] cell, a 725 V part is automatically chosen for high-line input, while 650 V for low-line input. However, the user can override the default selection dependent on the requirement and choose a 650 V part, if the actual measured stress voltage on the MOSFET is much less than 650 V and/or choose a device with smaller MOSFET, if temperature margin requirement is not critical.

The corresponding data sheet current limit specifications ($I_{LIMIT(MIN)}$ [E21], $I_{LIMIT(TYP)}$ [E22], and $I_{LIMIT(MAX)}$ [E23]) of the selected device are displayed, which are needed for calculating other design magnetic parameters.

MOSFET Peak Current, IP_MOSFET [E24]
To ensure DCM operation, the theoretical highest operating peak current should not exceed device minimum current limit of device.

Minimum ON-Time, TON_MIN [E25]
The minimum on-time operation is based on the minimum output voltage VO_MIN [E7] to ensure tight output current regulation.

Maximum ON-Time, TON_MAX [E26]
The maximum operating on-time (TON_MAX) is based on the maximum tolerance of output voltage (assumed to be 110%) to ensure tight output current regulation.

Device MOSFET Average and RMS Currents, IAVG_MOSFET [E27], IRMS_MOSFET [E28]
MOSFET average current (IAVG_MOSFET) and RMS current (IRMS_ MOSFET) are given to estimate the conduction loss of device MOSFET.

Ripple to Peak Current Ratio, KDP [E29]
Ratio between off-time of MOSFET and on-time of the secondary diode (Figure 5), KDP greater than 1 is recommended to ensure discontinuous conduction mode of operation.

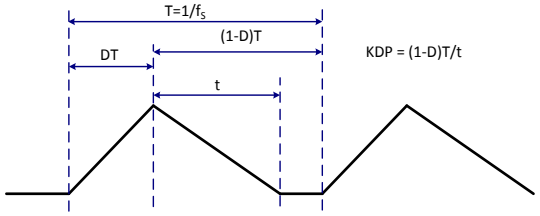


Figure 5. Inductor Current Illustration. KDP of > 1 Ensures Discontinuous Conduction Mode (DCM) of Operation.

MOSFET Drain to Source Voltage Stress, VDRAIN [E30]
Drain to Source voltage stress (V_{DRAIN}) is calculated based on maximum input voltage and 120% of V_O to account for overvoltage condition.

Step 3: Device Programming Parameters

34	**DEVICE PROGRAMMING PARAMETERS**					
35	RDO			6	k-ohms	DO pin resistor.
36	RDS			6	k-ohms	Current sense programming resistor connected to the DS pin for the buck-boost converter.

Figure 6. Device Programming Parameters Input of the Design Spreadsheet.

Data Output Resistor, RDO [E35]
Default value of 6 kΩ.

Topology Selection Resistor RDS [E36]
Resistor RDS is assigned a default value per PIXls design spreadsheet. There are two ways of sensing the output current with LYTSwitch-5 to maintain good regulation, that is Indirect (PSR) and Direct (SSR). These are topology dependent and programmed through RDS resistor value. With topologies where the output ground reference is not common with the input ground reference of the IC controller such as Buck or Isolated Flyback indirect current sensing (PSR) is used, this will eliminate the need for a use of a complex optocoupler or a level shifter circuitry. The sensing is done via the RDC sensing resistor where the signal is fed into the DRIVER CURRENT SENSE (DS) pin of the IC through the RDS resistor. The signal is processed internally and the interpolated value is outputted to the FEEDBACK (FB) pin which is filtered by C_{FB} and R_{FB} (Figure 7).

The latter is used if the ground references are common between the input and output circuitry. With direct sensing (SSR), the R_{DS} resistor is just simply connected to the SOURCE pin and the FEEDBACK pin is used to sense directly the output current via R_{FB2} sense resistor connected in series with the load and a small low pass filter (R_{FB} and C_{FB}) is needed for the feedback signal (Figure 7).

RDS (Ω)	Current Sensing	Topology
6 k	Indirect or Primary Sense Regulation (PSR)	Buck, Buck-Boost, Isolated Flyback
24 k	Direct or Secondary Sense Regulation (SSR)	Non-Isolated Flyback, Boost

Table 4. RDS Resistor Selection for Topology Current Sensing.

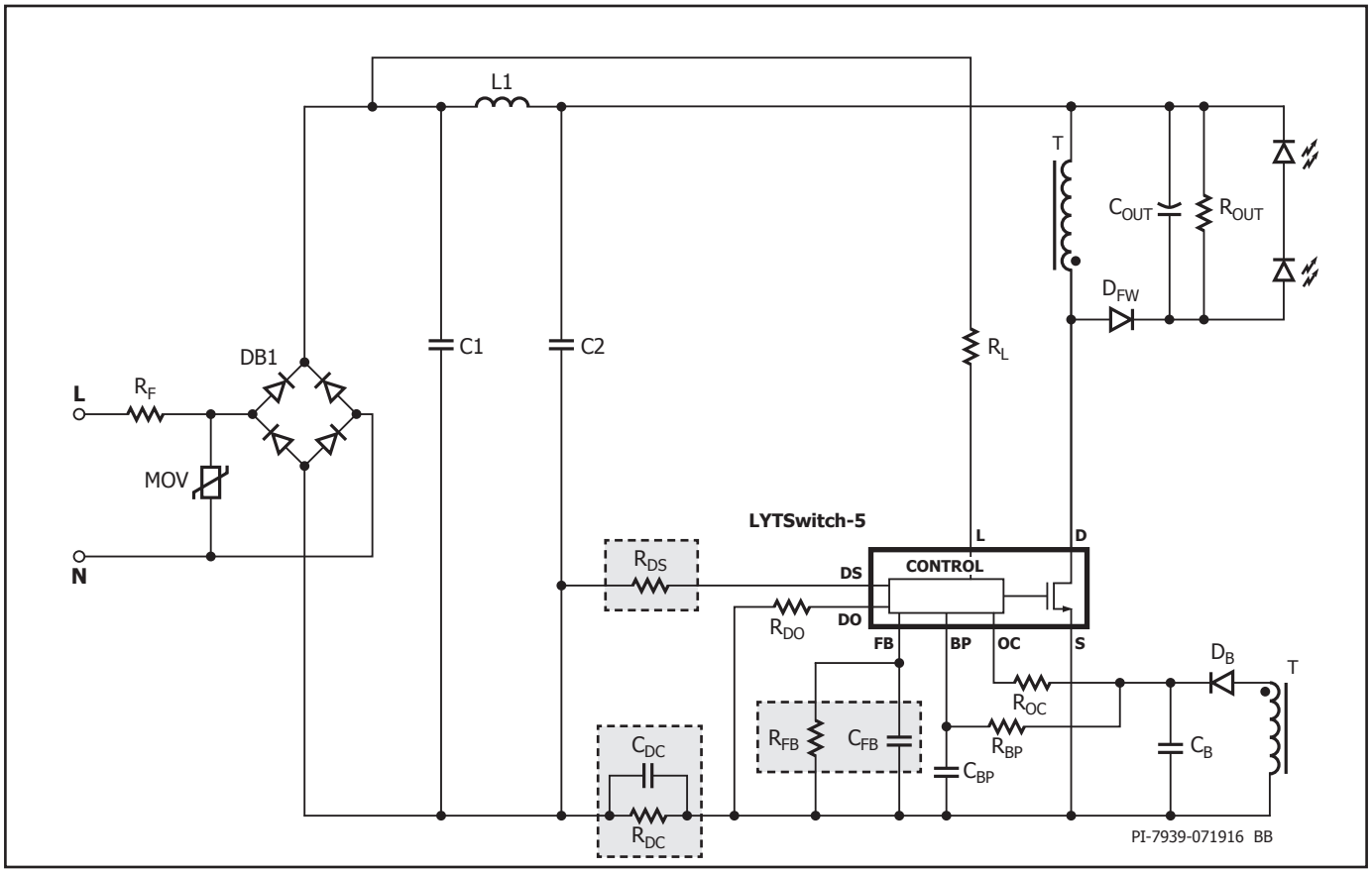


Figure 7. Schematic Shows R_{DS}, R_{DC}, R_{FB} and C_{FB} used for Indirect Sensing of Output Current with Buck-Boost Topology.

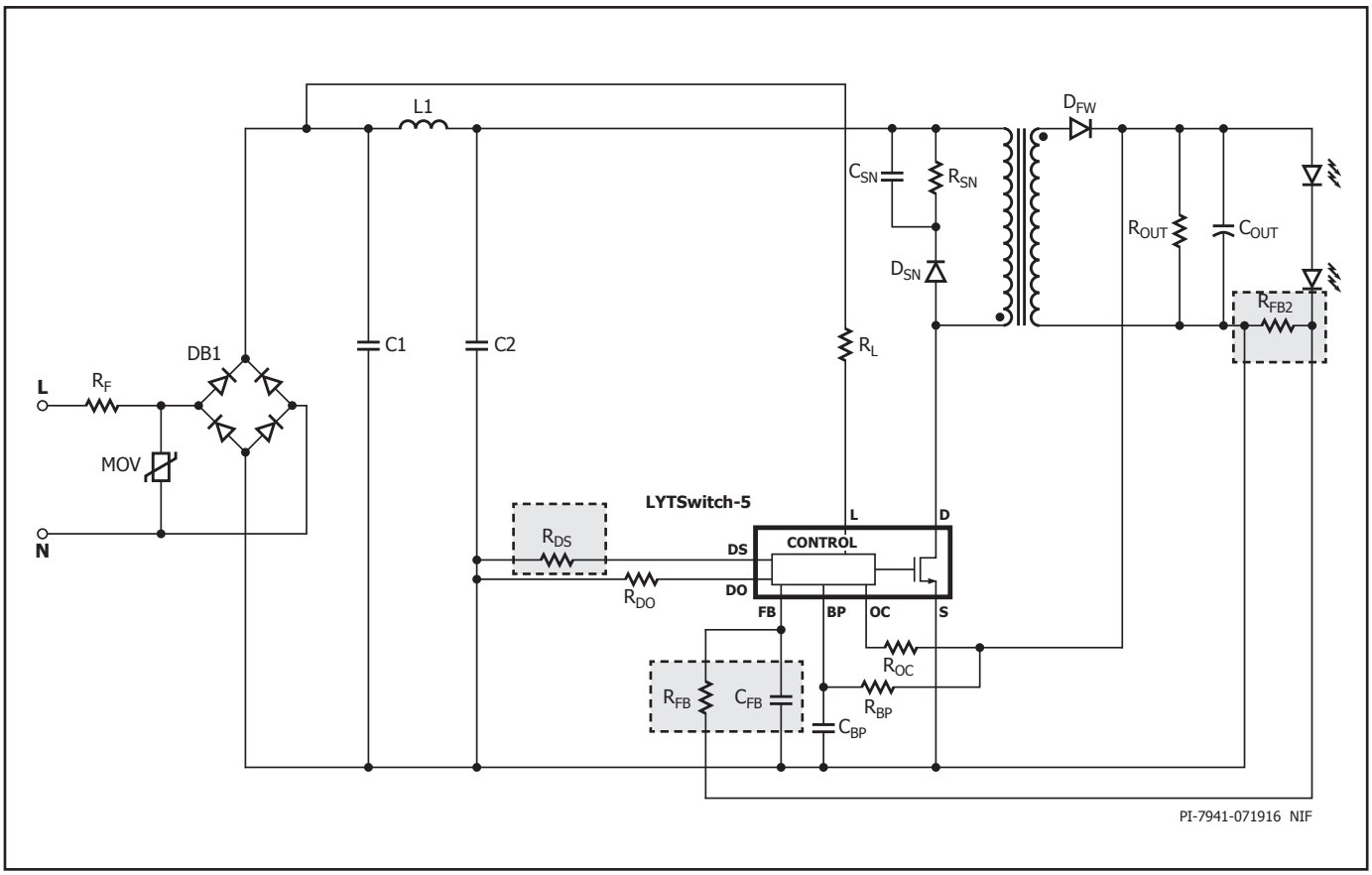


Figure 8. Schematic Shows R_{DS}, R_{FB2}, R_{FB} and C_{FB} used for Direct Sensing of Output Current with Non-Isolated Flyback.

See schematic for other topologies in Appendix A.

Step 4: Enter Inductor Core and Construction Variables CORE TYPE, AE, LE, AL, VE, AW, BW

40	**ENTER INDUCTOR CORE/CONSTRUCTION VARIABLES**					
41	CORE TYPE	EFD15		EFD15		Core type.
42	AE			15.00	mm^2	Core effective cross sectional area.
43	LE			34.00	mm	Core effective path length.
44	AL			700	nH/T^2	Ungapped core effective inductance.
45	VE			510	mm^3	Core volume.
46	AW			19.03	mm^2	Window area of the bobbin.
47	BW			8.85	mm	Bobbin physical winding width.

Figure 9. Inductor Core and Construction Variables Input of the Design Spreadsheet.

Core type selection as a default is set in Auto. The spreadsheet will automatically choose the smallest, but commonly used core suitable for the output power specified. Should the designer prefers a different type of core to use, a list of common cores can be selected from the drop down menu in cell Core Type [C41] of the PIXls spreadsheet or enter manually the parameters for the desired core to use.

Override cells can be used to enter the core and bobbin parameters onto cells AE [C42], LE [C43], AL [C44], VE [C45], AW [C46] and BW [C47]. This is useful if a preferred core is not on the list, or the specified core or bobbin information differs from that referenced by the spreadsheet.

Step 5: Enter Transformer Design Parameters

51	**TRANSFORMER DESIGN PARAMETERS**					
52	Inductance parameters					
53	INDUCTANCE	325		325	u-Henrys	Typical value of inductance.
54	INDUCTOR_TOL	5		5	%	Tolerance of inductance.
55	INDUCTANCE_MIN			309	u-Henrys	Minimum value of inductance.
56	INDUCTANCE_MAX			341	u-Henrys	Maximum value of inductance.
57	N	121		121	Turns	Number of inductor turns.
58	ALG			22.20	nH/T^2	Gapped core effective inductance.
59	BM			2857	Gauss	Maximum flux density.
60	BP			3822	Gauss	Peak flux density.
61	BAC			1429	Gauss	Worst case AC Flux Density for Core Loss Curves (0.5 X Peak to Peak).
62	LG			0.8	mm	Core gap length.
63	LAYERS_DESIRED			5	Dimensionless	Desired number of inductor's winding layers.
64	LAYERS_ACTUAL			4.61	Dimensionless	Actual number of inductor's winding layers.
65	AWG			29	AWG	Inductor's wire gauge.
66	OD_INDUCTOR_INSULATED			0.337	mm	Outer diameter of the inductor winding wire with insulation.
67	OD_INDUCTOR_BARE			0.286	mm	Outer diameter of the inductor winding wire without insulation.
68	IRMS_INDUCTOR			0.452	Amperes	Maximum RMS current flowing through the inductor's winding.
69	CMA_INDUCTOR			280	Cmils/A	Inductor winding CMA.
70	J_INDUCTOR			7.04	A/mm^2	Inductor Winding Current density.
71	PRIMARY WINDING FILL FACTOR			72%	Dimensionless	Percentage of bobbin window filled up by the inductor winding.

Figure 10. Transformer Design Parameters Section: Inductance Parameters of the Design Spreadsheet.

Inductance [E53]
This is the target nominal primary inductance for the main inductor. If left blank, the spreadsheet will calculate the inductance based on the VAC_MIN [E53] to guarantee discontinuous conduction mode over the entire input range. User has the flexibility to override the calculation on cell [C53] and optimized the inductance according to desired operation.

Inductor Tolerance [E54], Inductance_Min [E55] and Inductance_Max [E56]
Expected inductance production tolerance can be assigned in cell [C54]. This tolerance is used in the calculation of the worst-case condition of electrical parameters for primary current and operating duty cycle.

Inductor Turns, N [E57]
This is the number of turns for the main primary-winding. The spreadsheet will automatically optimize the number of turns based on estimated Maximum Flux Density, BM [E59] and worst-case AC Flux Density BAC [E61]. User can assign number of turns on cell [C57] for necessary adjustment.

$$N = INDUCTANCE_{(MAX)} \times IP_{(MOSFET/BM)} \times A_E$$

Gapped Core Effective Inductance, ALG [E58]
ALG (nH/T2) is used in production of core to set the inductance of the transformer. It is used by the transformer vendor to specify the core center leg air gap. This is the value of inductance obtained for the squared number of turns around the core.

Maximum Operating Flux Density, BM [E59]
To avoid core saturation during normal operation at maximum operating temperature, a maximum value of 3300 Gauss is recommended.

Peak Flux Density, BP [E60]
A maximum 4200 Gauss is recommended to avoid core saturation. Peak flux density usually occurs during start-up and/or output short-circuits conditions. The peak flux density is estimated at the maximum device current limit. It is important to verify that core saturation does not occur at maximum ambient temperature under start-up with maximum load.

$$BP = INDUCTANCE_{(MAX)} \times I_{LIMIT(MAX)/N} \times A_E$$

AC Flux Density, BAC [E61]
This is the flux density used in estimating the core loss for a given core material and volume in steady state condition. BAC = 0.5 × BM.

Core Gap Length, LG [E62]
Gap used in the transformer production to set the correct inductance based on core material permeability (AL).

Layers_Desired [E63] and Layers_Actual [E64]
Number of winding layers used to estimate the size of magnetic wire to fit in the transformer bobbin.

Transformer Wire Details, OD_Diameter_Insulated [E66]
Outside wire diameter with insulation is calculated with the maximum diameter that allows the wire to fit given number of primary turns (N), bobbin width (BW) and assigned number of winding layers (L).

Inductor RMS Current, IRMS_Inductor [E68]
The RMS current can be used to estimate winding copper loss of the inductor.

The other useful magnetic parameters given in the spreadsheet are:
OD_Inductor_Bare [E67], diameter of wire without insulation.
CMA_Inductor [E69], inductor winding effective Circular Mils Area.
Current_Density [E70], inductor winding effective current density.
Primary Winding Fill Factor [E71], percentage of bobbin window filled up by the primary winding to estimate if there is sufficient space.

Override cells [C53], [C54], [C57], [C63] and [C65] can be used to enter desired parameters.

Step 6: Transformer Bias Winding and Bias Components

Bias supply necessary to supply current into the BYPASS pin to operate normally even at all input and output conditions and also provides feedback information into the OC pin for regulation. The rectifier diode can be any fast or ultrafast recovery type with a voltage rating above the value given in the design spreadsheet (PIVBS [E77]), typically >200 V, and current rating >200 mA. The 1N4936 and UF4004 are good examples.

Output Rectifier Maximum Peak Inverse Voltage, PIV_{BS} [E77]
This is maximum stress voltage across the bias diode at the maximum input voltage.

$$PIV_{BS} = BIAS_{TURNS/N} \times VAC_{MAX} \times \sqrt{2} + BIAS$$

Override cells [C74] and [C76] can be used to enter desired parameters for VD_{BIAS} and V_{BIAS} respectively.

73	Bias winding parameters					
74	VD_BIAS			0.70	Volts DC	Bias winding diode forward drop voltage.
75	BIAS TURNS			21	Turns	Number of bias winding turns.
76	VBIAS			12.0	Volts DC	Bias Voltage. Check performance at minimum VO and VACMAX.
77	PIVBS			77.0	Volts DC	Output Rectifier Maximum Peak Inverse Voltage (calculated at VACMAX)
78	CBIAS			22.0	u-Farads	Bias winding rectification capacitor.
79	RBP			6.36	k-Ohms	Bias supply resistor assuming 1mA current necessary to supply the BP pin.
80	CBP			2.2	u-Farads	Minimum BP pin capacitance.

Figure 11. Transformer Bias Winding Parameters of the Design Spreadsheet.

Bias Diode Forward Voltage Drop, VD_BIAS [E74]
Default value of typical forward voltage drop of 0.7 V for the bias rectifier diode.

Bias Winding Turns, $BIAS_{TURNS}$ [E75]
This is the number of turns of the bias winding calculated based on bias voltage chosen and output voltage.

$$BIAS_{TURNS} = (V_{BIAS} + VD_{BIAS})/(V_O + VF_{DIODE}) \times N$$

Bias Voltage, V_{BIAS} [E76]
Default value is 12 V the minimum value to ensure voltage supply for the bias to support the IC. Excessive voltage ripple is not recommended, at least 10 µF electrolytic capacitor filter must be used and if ceramic type capacitor is used, 22 µF value is recommended to account for huge tolerance for type of capacitor.

For designs which require a wider LED voltage operation, increasing the bias voltage to 20 V is recommended to maintain tight regulation with lower LED voltage.

Step: 7 Secondary Output Diode Parameters

Use ultrafast diode for output rectification and the recommended diode rating should 2 times of the output current, i.e. $2x\ I_O < I_{AVG(DIODE)}$, for higher efficiency.

Output Diode Voltage Drop, VF_DIODE [E85]
Enter the average forward voltage drop for the output diode. Use 0.7 V for a PN diode. Estimated forward power loss to this diode estimated by taking the product of $I_O \times V_F$.

Output Diode RMS Current, IRMS_DIODE [E86]
The RMS current through the diode is calculated that can be used to calculate the copper loss of the inductor.

Output Diode Peak Current, IP_DIODE [E87]
Peak current in the output diode is calculated in a worst-case condition to guide the user to select the diode current rating and package size.

Peak Inverse Diode Voltage, PIV_DIODE [88]
Use this parameter in selecting the voltage rating of the output diode. The worst-case reverse peak voltage is calculated in open load condition which is the worst-case condition.

For Buck-Boost;

$$PIV_{DIODE} = VAC_{MAX} \times \sqrt{2} + VO_{MAX}$$

84	**SECONDARY DIODE PARAMETERS**					
85	VF_DIODE			0.7	Volts DC	Output diode forward voltage drop.
86	IRMS_DIODE			0.375	Amperes	Diode RMS current at LP_MIN, VACMIN and PO_MAX.
87	IP_DIODE			1.520	Amperes	Diode peak current at LP_MIN ,VACMAX and PO_MAX.
88	PIV_DIODE			506.0	Volts DC	Peak Inverse Voltage at VO_MAX on output diode.

Figure 12. Secondary Diode Parameters of the Design Spreadsheet.

Step 8: Feedback and Protection Parameters with Fine Tuning

This section will guide the user in selecting the external parts to be used in the design for achieving the target output current. Leaving the section blank will recommend the initial value to be used in the prototype. Once the prototype has been built, the output current can be fined tuned using the override cells [C93], [C96], [C98], [C99] and [C101].

92	**FEEDBACK AND PROTECTION PARAMETERS WITH FINE TUNING**					
93	RL			3.74	M-Ohms	Standard (E96 / 1%) L pin resistor.
94	OVP_LINE			317.3	Volts RMS	Line overvoltage based on the actual L pin resistor used.
95	RDC_THEORETICAL			2.84	Ohms	Theoretical DS pin sense resistor.
96	RDC			2.87	Ohms	Standard (E96 / 1%) DS pin sense resistor.
97	CDC			10.0	u-Farads	Standard capacitor connected in parallel with the DS pin sense resistor.
98	VBIAS_MEASURED			12.0	Volts DC	Actual bias voltage (across the bias capacitor) measured on the bench.
99	VO_MEASURED			75.0	Volts DC	Actual load voltage measured on the bench.
100	ROC			100.0	k-Ohms	Standard (E96 / 1%) OC pin resistor.
101	IO_ACTUAL			160.0	m-Amperes	Actual output current seen on the bench.
102	RFB_THEORETICAL			41.8	k-Ohms	Calculated value of RFB, using standard values for RDS, ROVP, and RL
103	RFB			42.2	k-Ohms	Standard (E96 / 1%) F pin resistor.
104	CFB			150.0	n-Farads	Standard capacitor connected to the F pin.

Figure 13. Feedback and Protection Parameters with Fine Tuning of the Design Spreadsheet.

Line-Sense Resistor, RL [E93]
Line-sense resistor is used for line compensation for regulation, phase angle measurement in dimming, line input overvoltage detection. To achieve accurate output current regulation and accurate line measurement a resistor with 1% tolerance is recommended. It is also recommended to use 2-1206 or 2-1/4 W package resistor for high-line application and 1-1206 or 1-1/4 W for low-line application.

$$R_L = VAC_{MAX} \times \sqrt{2} / I_{LOV}$$

Line Overvoltage, OVP_LINE [E94]
This protection is against line surge or swell. The unit will enter to auto restart when the threshold is reached. The spreadsheet will calculate the equivalent RMS input voltage for OVP.

$$OVP_{LINE} = R_L \times I_{LOV+} \times \sqrt{2}$$

Where;
I_{LOV+}: Current threshold for input overvoltage at typical value of 120 µA in the data sheet.

Theoretical Drain Current Sense Resistor, RDC_THEORETICAL [E95]
The ideal resistor value to be used in the drain current sensing is calculated. The voltage drop across the resistor is sensed through DS pin and the recommended average voltage drop across this sense resistor is 200 mV.

Standard Drain Current Sense Resistor, RDC [E96]
This identifies standard 1% resistor value nearest to the RDC_THEORETICAL to lessen the need of paralleling another resistor for centering the output, also saves cost and space (Figure 8).

Capacitance Across Drain Current Sense Resistor, CDC [E97]
This is the capacitor (CDC) across the drain current sense resistor (RDC) that filters the switching drain current to reduce the IRMS power dissipation across the sense resistor.
Low ESR ceramic type capacitor is recommended to use. Aluminum electrolytic capacitor due to its size, cost, relative high ESR and high capacitance tolerance is not recommended.

Actual Bias Voltage, VBIAS_MEASURED [E98]
Enter the actual bias voltage for fine tuning the output current. The actual may differ significantly from calculated due to leakage inductance of the transformer.

Actual Output Voltage, VO_MEASURED [E99]
Enter the actual output voltage with LED load for fine tuning the output current.

Output Current Compensation Resistor, ROC [E100]
Load variation, output overvoltage protection and output short-circuit is monitored through bias voltage via compensating resistor (ROC). Spreadsheet will calculate this resistance based from the actual bias voltage (VBIAS_MEASURED). A 1% tolerance resistor is recommended in this location for tight output current tolerance.

Actual Output Current, IO_ACTUAL [E101]
Enter the actual current as measured from the bench for the fine tuning of external components to center the output to a desired level.

Theoretical Feedback Resistor, RFB_THEORETICAL [E102]
Spreadsheet calculates the exact feedback resistor resistance to set the output current based from the actual output current measured.

Feedback Resistor, RFB [E103]
The spreadsheet will determine the nearest single resistance to use for RFB to avoid paralleling of components to get the desired current. But if the application requires tight output current tolerance then use the resistance calculated by RFB_THEORETICAL.

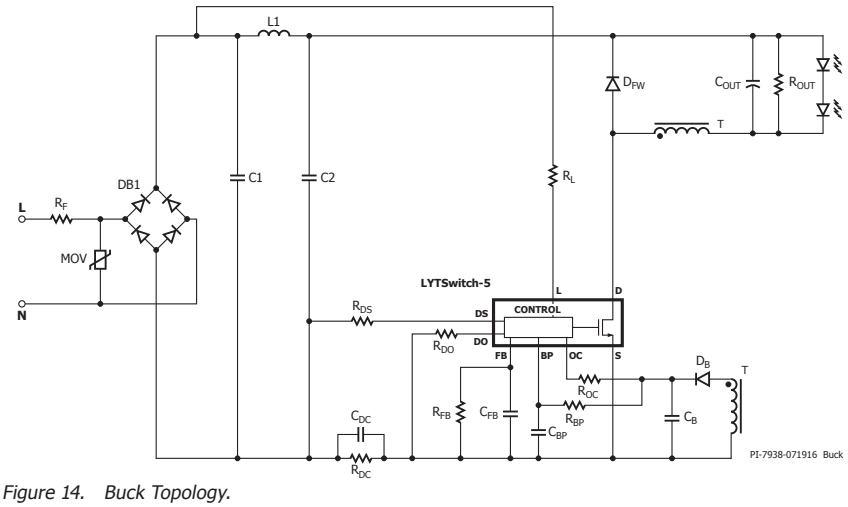
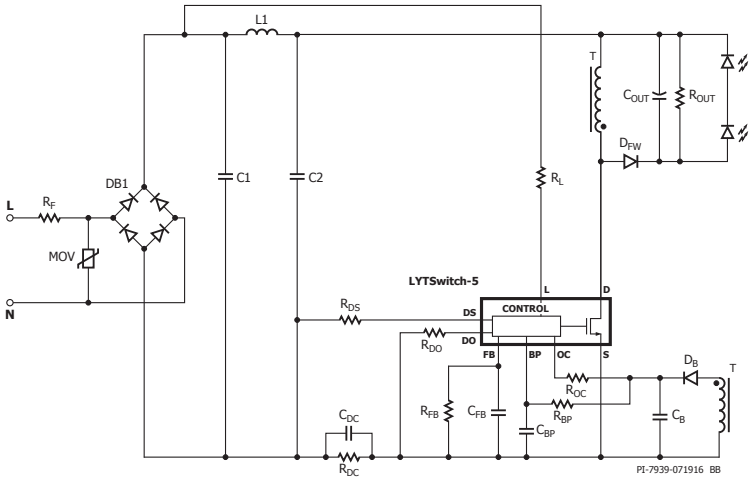
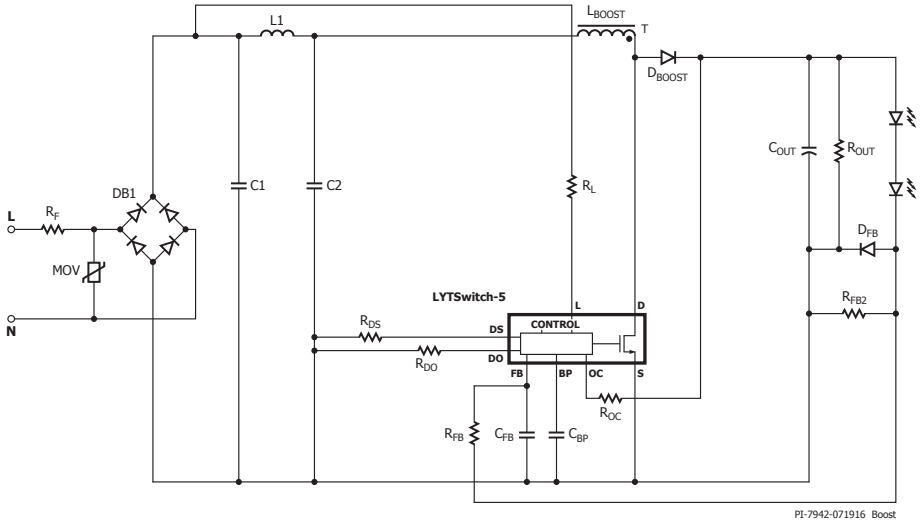
Feedback Filter Capacitance, CFB [E104]
Filter capacitance for the feedback current to average the signal to a desired voltage mean level of the FEEDBACK pin. The desired time constant is in the range of 3 ms to 6 ms to maintain stable operation with tight current regulation.

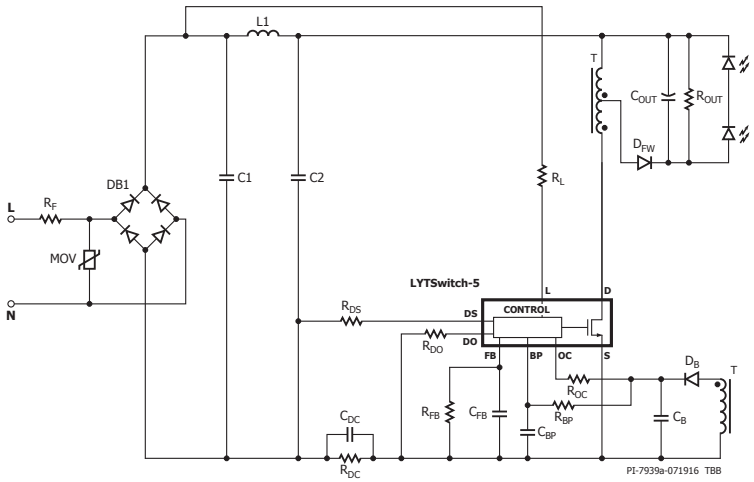
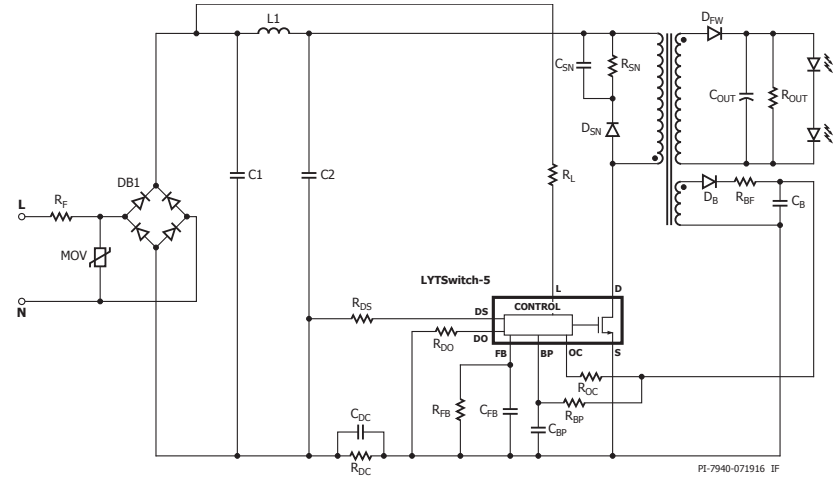
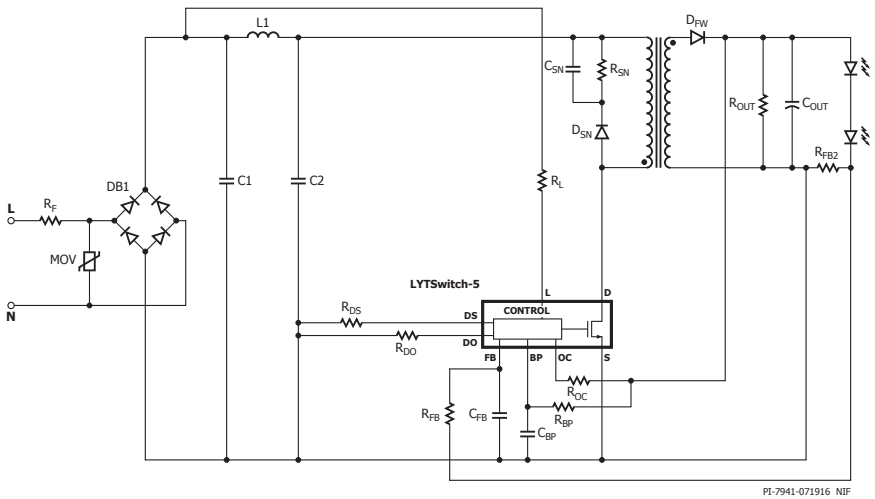
$$t_C = C_{FB} \times R_{FB}$$

PIXls Design Spreadsheet for other topologies is available in PI public website (https://piexpertonline.power.com/site/login)

Appendix A:

LYTSwitch-5 Topology Configurations

Basic Circuit Schematic	Key Features
	Buck Benefits • Highest efficiency • Lowest component count – small size • Simple low-cost power inductor • Low drain source voltage stress • Best EMI/lowest component count for filter Limitations • Non-Isolated
Figure 14. Buck Topology.	
	Buck-Boost Benefits • Ideal for non-isolated high output voltage designs • High efficiency • Low component count • Simple common low-cost power inductor can be used • Lowest THD Limitations • Maximum VOUT is limited by MOSFET breakdown voltage • Non-isolated
Figure 15. Buck-Boost Topology.	
	Boost Benefits • Ideal for non-isolated high output voltage designs; Vo > Vin • Highest efficiency • Lowest component count • Simple common low-cost power inductor Limitations • Maximum VOUT is limited by MOSFET breakdown voltage • Single input line voltage range • Non-isolated • High THD
Figure 16. Boost Topology.	

Basic Circuit Schematic	Key Features
 *Figure 17. Tapped Buck-Boost Topology.*	Tapped Buck-Boost Benefits • Ideal for low output voltage designs (<25 V) • Simple common low-cost tapped inductor • Low THD Limitations • Maximum VOUT is limited by MOSFET breakdown voltage
 *Figure 18. Isolated Flyback Topology.*	Isolated Flyback Benefits • Provides isolated output • Supports widest range of output voltages • Lowest THD Limitations • Flyback transformer • Overall efficiency reduced by parasitic capacitance and inductance in the transformer • Larger PCB area to meet isolation requirements • Requires additional components (primary clamp and bias) • Higher RMS switch and winding currents increases losses and lowers efficiency
 *Figure 19. Non-Isolated Flyback Topology.*	Non-Isolated Flyback Benefits • Direct sensing of output current • Supports widest range of output voltages • Low THD Limitations • Flyback transformer • Overall efficiency reduced by parasitic capacitance and inductance in the transformer • Larger PCB area to meet isolation requirements • Requires additional components (primary clamp and bias) • Higher RMS switch and winding currents increases losses and lowers efficiency

Revision	Notes	Date
A	Initial Release.	07/16

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