Application Note AN-86
LinkSwitch-XT2 Family

Design Guide

Product Highlights

The LinkSwitch™-XT2 IC family combines a high-voltage (725 V or 900 V) power MOSFET switch and an ON/OFF controller into a monolithic IC which is fully fault protected. Auto-restart limits device and circuit dissipation during overload and output short-circuit, over-temperature protection disables switching during thermal faults. Large hysteresis in the thermal protection circuit protects the PCB and surrounding components from experiencing high average temperature during fault conditions. Frequency-jitter reduces EMI by modulating switching frequency. The LinkSwitch-XT2 family is ideal for low-power adapters and chargers as well as auxiliary power for appliances, and to provide power for industrial systems, and metering power. LinkSwitch-XT2-based circuits are extremely cost-effective and offer an ideal replacement for linear charger replacement circuits, meeting worldwide standby and efficiency standards such as those described by the California Energy Commission (CEC).

LinkSwitch-XT2 ICs can operate without a primary-side clamp circuit (Clampless™) for output powers below 2 W (up to 2.5 W with a bias winding) significantly reducing component count. As a replacement for conventional linear and RCC topologies, LinkSwitch-XT2-based designs offer multiple functional benefits.

- Output overvoltage protection (OVP)
- Input overvoltage line protection (OVL)
- Hysteretic over-temperature protection (OTP)
- Extended creepage between DRAIN pin and all other pins to improve field reliability
- 725 V MOSFET rating for excellent surge withstand
- 900 V MOSFET rating series for increased industrial input voltage ranges or extra safety margin
- Extremely low component count
- Single-sided PCB and full SMD manufacturability

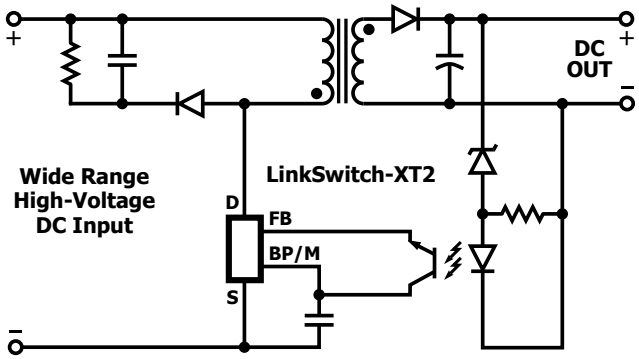


Figure 1. Basic Configuration Using LinkSwitch-XT2 in a Flyback Converter.

Scope

This application note describes the process of designing an isolated power supply using the LinkSwitch-XT2 family of devices. The objective is to provide power supply engineers with and to enable them to build quickly an efficient, cost-effective flyback converter. Design equations are provided for the selection of key components. To simplify terminology, the application note refers directly to the PIXls design spreadsheet that is part of the PI Expert™ design software suite. The basic circuit for LinkSwitch-XT2 power supplies is shown in Figure 1, which also serves as the reference for component identification and is used throughout this application note.

In addition to this application note, the reader may also find the LinkSwitch-XT2 Reference Design Kit (RDK) – containing an engineering prototype board, useful as an example of a complete and fully functional power supply. Further details can be found at www.power.com.

Quick Start

Readers familiar with power supply design and Power Integrations design software may elect to skip the step-by-step design approach described later, and can use the following information to quickly design the transformer and select the components for a first prototype. For this approach, only the information described below needs to be entered into the PIXls spreadsheet, other parameters will be automatically selected based on a typical design. The spreadsheet below is for LNK3604 XT2 Variant.

- Enter AC input voltage range VACMIN, VACMAX and minimum line frequency fL
- Enter Time_Bridge_Conduction estimate
  - The conduction time, is usually set at 2.66 ms and can be verified by direct measurement.
- Enter nominal output voltage VOUT
- Enter continuous output current IOUT
- Enter estimated efficiency, η
  - 0.8 for universal input voltage (85-265 VAC) or single 100/115 VAC (85-132 VAC) and 0.85 for a single 230 VAC (185-265 VAC) design. Adjust the number accordingly after measuring the efficiency of the first prototype board at peak load and VACMIN.
- Enter loss allocation factor
  - 0.5 for typical application. Adjust the number accordingly after the first prototype-board evaluation.
- Enter input capacitance
  - 2-3 μF/W for universal (85-265 VAC) or single 100/115 VAC (85-132 VAC) line input.
  - 1 μF/W for single 230 VAC (185-265 VAC) line input
- Select the type of Feedback configuration
  - Choose between Opto for isolated converter or Bias winding for non-isolated converter.
- Select Yes if a bias winding is required
- Select configuration for current limit mode
  - Two current limit configurations are available, REDUCED, STANDARD.
- Enter the desired reflected output voltage, VOR
  - A good starting value for VOR is to set within the range of 90 V – 110 V.
- Enter the on-state Drain to Source Voltage, VDSON
  - The default value given is 10 V. If no available value given in MOSFET datasheet, typical setting of VDSON during on-state is 10 V.
- Enter Primary Inductance Tolerance, LPRIMARY_TOL
  - The default value given is 10%. If no available data from the supplier, typical setting is 10% to ensure manufacturability of the transformer.
- Enter the Output Winding Diode Forward Voltage Drop, VF_SECONDARY
  - VF_SECONDARY is typically set at 0.7 V.
- Enter core type (if desired),.
  - Suggested core size will be selected automatically if none is entered
  - AE, LE, AL, BW are automatically reflected based on the selected core type.
  - For custom core, enter the core parameters
- Enter the desired safety margin, MARGIN
  - The default margin in the spreadsheet is 0 mm, assuming that a triple insulated wire will be used for secondary windings.
  - If triple insulated wire is not used at the secondary winding, the value that should be entered for safety margin M is 3.1 mm. This is the typical margin for universal input (85 – 265 VAC).
- Enter number of primary layers (if desired), LAYERS_PRIMARY
  - The default number of primary layers reflected in the spreadsheet is 3.
- Enter the Primary winding wire AWG, AWG_PRIMARY
  - The value recommended is based on the given/calculated primary current. If desired to alter the value other parameters and ensure that no warnings are generated.
- Enter secondary number of turns, NSECONDARY
  - If the grey override cell is left blank, the spreadsheet will automatically calculate the secondary number of turns.
- Enter the desired Bias Turns , NBIAS
  - Typically, the default value in the spreadsheet will give a 22 V Bias winding voltage as this gives the optimized performance on OVP setting.
- Enter Bias Winding Diode Forward Voltage Drop, VF_BIAS
  - Typically set at 0.7 V.

For multiple outputs design enter the following requirements under Transformer Secondary Design Parameters (Multiple Outputs):

1st Output
(If unused, the defaults are from the single output design)
- Enter the Main Output Voltage, VOUT1

2nd Output
(If unused, leaved the section blank)
- Enter the 2nd Output Voltage, VOUT2
- Enter the 2nd Output DC Current, IOUT2
- Enter the output diode voltage drop for the 2nd output, VD2

A 3rd output may be added if desired.

If any warnings are generated, make changes to the design by following instructions in spreadsheet.
- Build transformer as suggested in "Transformer Construction" tab
- Select key components
- Build prototype and iterate design as necessary, entering measured values into spreadsheet where estimates were used (e.g. efficiency, VMIN). Note that the initial efficiency estimate is very conservative.

Output Power Table

Poducts[3]	Peak or Open Frame[1,2]	
	725 V MOSFET	
	230 VAC ±15%	85-265 VAC
LNK3604P/G/D	9.2 W	6.1 W
Products[3]	900 V MOSFET	
	230 VAC ±15%	85-265 VAC
LNK3694P/G/D	6 W	4 W
LNK3696P/G/D	11 W	8 W

Table 1. Output Power Table.

Notes:
1. Maximum continuous power in a typical non-ventilated enclosed adapter measured at 50 °C ambient.
2. Maximum practical continuous power in an open frame design with adequate heat sinking, measured at 50 °C ambient.
3. Packages: P: DIP-8C, G: SMD-8C, D: SO-8C.

Step-by-Step Design Procedure

Step 1 – Enter Application Variables VAC_{MIN}, VAC_{MAX}, f_L, V_O, I_O, η, C_{IN}

ENTER APPLICATION VARIABLES					
LINE VOLTAGE RANGE			UNIVERSAL		AC line voltage range
VACMIN	85.00		85.00	Volts	Minimum AC line voltage
VACTYP			115.00	Volts	Typical AC line voltage
VACMAX	265.00		265.00	Volts	Maximum AC line voltage
fL	50		50	Hertz	AC mains frequency
TIME_BRIDGE_CONDUCTION	2.90		2.90	mseconds	Input bridge rectifier diode conduction time
LINE RECTIFICATION	F		F		Select 'F'ull wave rectification or 'H'alf wave rectification
VOUT	5		5	Volts	Output voltage
IOUT	0.5		0.5	Amperes	Average output current specification
CC THRESHOLD VOLTAGE	0.00		0.00	Volts	Voltage drop across the sense resistor
OUTPUT CABLE RESISTANCE	0.00		0.00	Ohms	Enter the resistance of the output cable (if used)
EFFICIENCY	0.70		0.70		Efficiency Estimate at output terminals. Under 0.8 if no better data available
LOSS ALLOCATION FACTOR	0.50		0.50		The ratio of power losses during the MOSFET off-state to the total system losses
POUT			2	Watts	Continuous Output Power
CIN	6.60		6.60	uFarads	Input capacitor
VMIN			91.16	Volts	Valley of the rectified VACMIN
VMAX			374.77	Volts	Peak of the VACMAX
FEEDBACK	OPTO		OPTO		Select the type of feedback required
BIAS WINDING	YES		YES		Select whether a bias winding is required

Table 2. Application Variable Section of LinkSwitch-XT2 Design Spreadsheet.

Input Voltage
Determine the input voltage range from Table 3.

Nominal Input Voltage (VAC)	VAC_{MIN}	VAC_{MAX}
100/115	85	132
230	195	265
Universal	85	265

Table 3. Standard Worldwide Input Line Voltage Ranges.

Line Frequency, f_L
Select 50 Hz for universal or single line 100 VAC, 60 Hz for single line 115 VAC input. 50 Hz for single 230 VAC input. These values represent typical line frequencies which most applications this gives adequate overall design margin. For absolute worst-case conditions, assume a line frequency tolerance of ±6%.

Output Voltage, V_{OUT} (V)
Enter the nominal output voltage of the main output during the continuous load condition. Generally, the main output is the output from which feedback is derived. For CV/CC designs this should be the typical output voltage at the nominal peak power point in the output characteristic. For CV only outputs, this should be the specified output voltage. For designs with an output cable, enter the voltages at the load.

Output Current, I_{OUT} (A)
Enter the output current from the power supply. For CV/CC designs this should be the maximum output current at the maximum peak-power point in the output characteristic (see Figure 2). For CV only outputs, this should be the maximum output current. In multiple output designs the output power of the main output (typically the output from which feedback is taken) should be increased such that the maximum continuous output power from the main output matches the combined output power from all the outputs. The individual output voltages and currents should then be entered at the bottom of the spreadsheet.

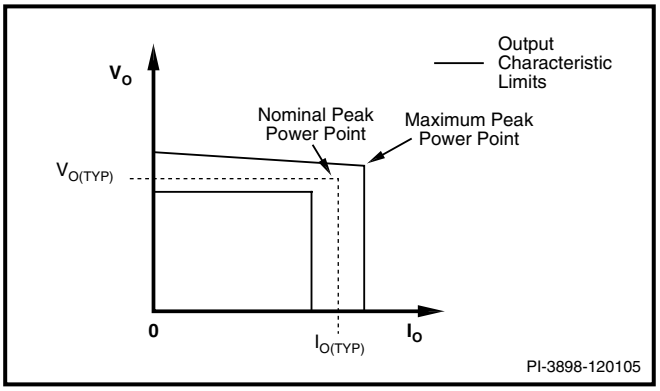


Figure 2. Diagram Showing Correct Values of IO and VO to Enter for CV/CC Designs.

CC Threshold Voltage (V)
For CV only designs, this is not applicable; enter 0. For CV/CC designs, this is the expected voltage developed across the current sense resistor at the nominal CC point. Typically, this value is in the range of 0.3 V to 1.3 V, depending on the specific circuit used. For designs using the V_BE of a bipolar transistor (~ 0.65 V) as the CC reference voltage, to maintain CC control, the optocoupler LED has to stay forward biased. This may require an additional resistor to be added in series with the CC sense resistor to increase the overall voltage drop (> ~1.1 V). It is this overall voltage drop that should be entered as the CC threshold. For the exact forward drop of the optocoupler LED, consult the manufacturer's data sheet.

Output Cable Resistance (Ω)
Enter the output cable resistance. If there is no output cable enter 0. This parameter is used as part of the total output power calculation.

Power Supply Efficiency, η
This is the complete power supply efficiency measured at the point of load, therefore including any CC sense and cable losses. For a CV/CC design with a nominal peak power point at a voltage of 5.5 V and current of 0.5 A, use a value of 0.57. Use a value of 0.64 for a 5.5 V CV only design if no better data is available, or until measurements can be made on a prototype.

Bridge Diode Conduction Time, t_c (ms)
Enter the bridge diode conduction time. Use 2.66 ms if no other data is available or until a measurement can be made on a prototype.

Power Supply Loss Allocation Factor
This factor represents the proportion of losses between the primary and the secondary of the power supply.
If no better data is available then the following values are recommended:

$$Z = \frac{\text{Secondary Losses}}{\text{Total Losses}}$$

- Bias winding feedback designs (CV): 0.5
- Optocoupler CV feedback: 0.5
- Optocoupler CV and CC feedback: 0.75

Total Input Capacitance, C_{IN} (μF)
Enter total input capacitance using Table 4 for guidance. The capacitance is used to calculate the minimum and maximum DC voltage across the bulk capacitor and should be selected to keep the minimum DC input voltage, V_{MIN} > 50 V, and ideally V_{MIN} > 70 V.

	Total Input Capacitance per Watt Output Power μF/W	
AC Input Voltage (VAC)	**Full-Wave Rectification**	**Half-Wave Rectification**
100/115	2	4-5
230	1	1-2
86-265	2	4-5

Table 4. Suggested Total Input Capacitance for Different Input Voltage Ranges

Enter Feedback, Bias type and Clamp information
Select between either bias winding feedback (primary-side feedback), Figure 3, or optocoupler feedback (secondary-side feedback), Figure 4. Bias winding makes use of a primary- side auxiliary winding to set the output voltage. Optocoupler feedback directly senses the output voltage and can provide any level of accuracy depending on the voltage reference selected. Secondary-side feedback also allows for a CV/CC output characteristic. See Table 5 for a summary of feedback types.

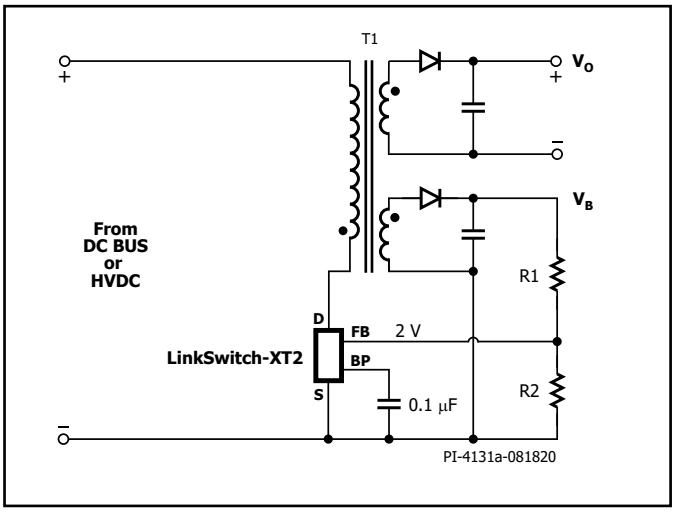


Figure 3. Primary-Side Feedback (Bias Winding Feedback) Scheme Used in a CV Only Output

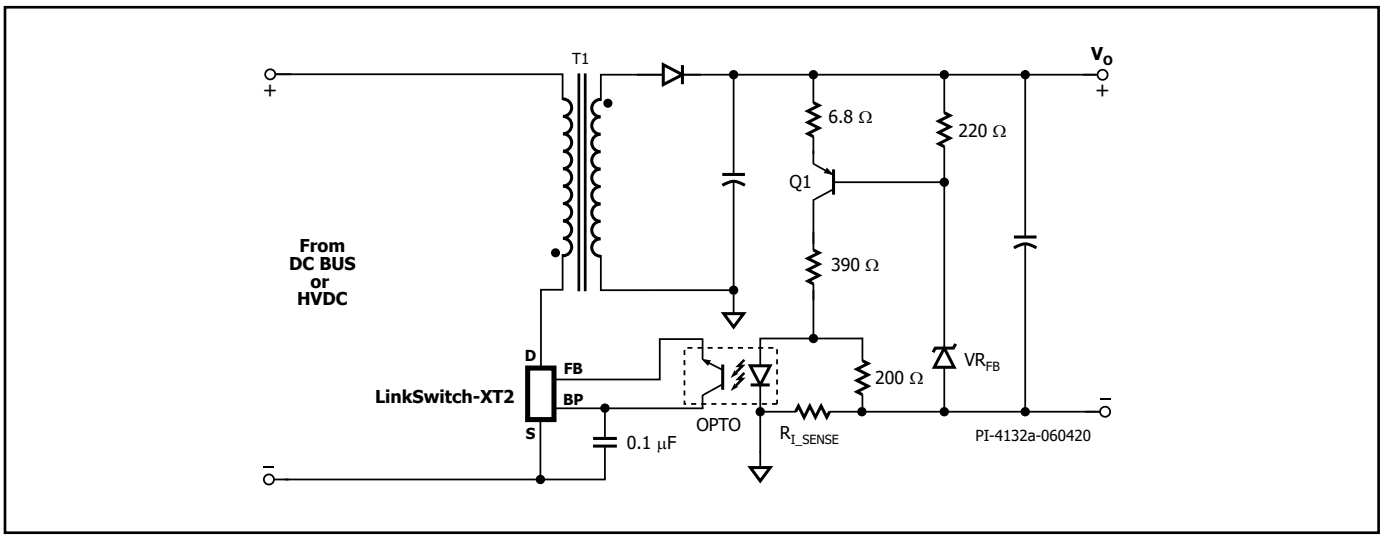


Figure 4. Secondary-Side Feedback Scheme used for a CV/CC Output Characteristic Design.

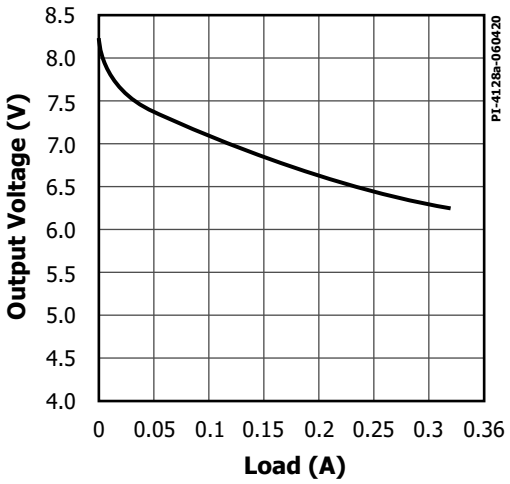
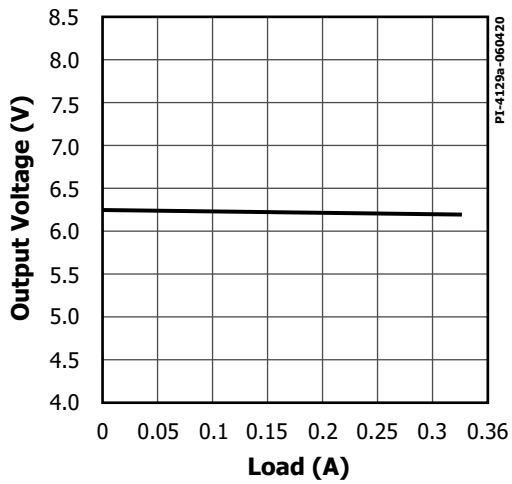
	Bias Winding Feedback	Optocoupler Feedback
Typical Output Characteristics		
Cost	Lower cost	Higher cost
Component Count	Lower component count	Higher component count
CV/CC Characteristic Possible	No	Yes

Table 5. Summary of Comparison Between Bias Winding Feedback and Optocoupler Feedback.

Figure 1 shows a CV only optocoupler design, Table 6 provides guidance for component selection for both CV and CV/CC configurations. Figure 3 shows a CV only bias winding configuration.

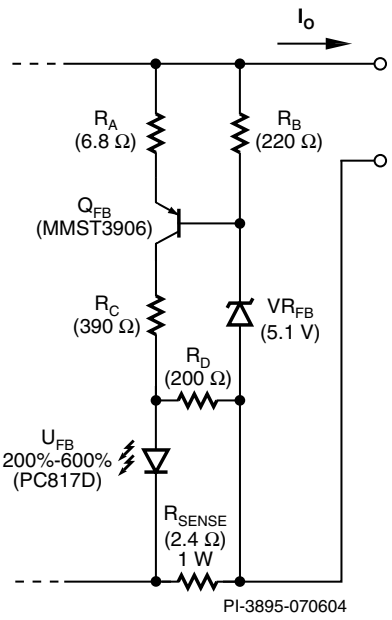
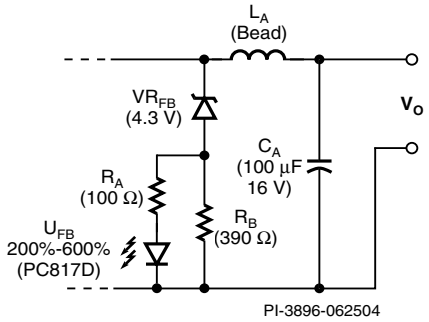
Output Type	CV/CC	CV Only
Suggested Feedback		
Notes	R_{SENSE}: $V_{F(UFB)}/I_O$ VR_{FB}: $V_{O-VBE(QFB)}$ (Use a Zener with a low I_{ZT} such as the BZX79 series) R_S: $V_{BE(QFB)}/I_{ZT(VRFB)}$ R_A: Limits base-emitter current of Q_{FB}, R_C and R_D: Limits U_{FB} current U_{FB}: Use high CTR device (200% – 600%) Q_{FB}: Any samll signal PNP transistor (Values shown for a 5.5 V, 500 mA output)	VR_{FB}: V_O-$V_{F(UFB)}$ (Use a Zener with a low I_{ZT} such as the BZX79 series) R_B: $V_{F(UFB)}/I_{ZT(VRFB)}$ R_A: Limits U_{FB} current during transients and allows small output voltage adjustments U_{FB}: Use high CTR device (200% – 600%) L_A: Optional for lower output switching noise (Use ferrite bead or low value (1-3 µH) inductor rated for I_O) C_A: Optional for lower output switching noise (Use low ESR, 100 µF with voltage rating >1.25 × V_O) (Values shown are for a 5 V output)

Table 6. Example of Feedback Configurations.

If optocoupler feedback is selected, the user still has the option to use a bias winding. It may be used to externally power the LinkSwitch-XT2 device for lower no-load consumption. In addition, the bias winding can be configured as a shield for reduced EMI.

Designs below 2.5 W output power may be able to eliminate the primary-side clamp circuit. Clampless circuits offer the benefit of low cost and component count, but these circuits rely on specific transformer construction techniques. See the section on transformer construction for details.

For designs greater than 2.5 W, a Clampless solution is not recommended. See the section on clamp design for details.

All the variables described above can be entered in the "Enter Application variables" section of the LinkSwitch-XT2 design spreadsheet in PI Xls design software (see Table 2).

Step 2 – Enter LinkSwitch-XT2 Variables

To select the correct LinkSwitch-XT2 device, refer to the LinkSwitch-XT2 data sheet power table and select based on the input voltage, enclosure type and output power of the design.

LINKSWITCH-XT2 VARIABLES					
CURRENT LIMIT MODE	RED		RED		Pick between RED(Reduced) or STD(Standard) current limit mode of operation
PACKAGE	SO-8C		SO-8C		Device package
ENCLOSURE	Adapter		Adapter		Pick the device enclosure
GENERIC DEVICE			LNK3604		Device series
DEVICE CODE			LNK3604D		Device code
PMAX			3.60	Watts	Device maximum power capability
VOR	77		77	Volts	Voltage reflected to the primary winding when the MOSFET is off
VDSON			10.0	Volts	MOSFET on-time drain to source voltage
VDSOFF			556.5	Volts	Estimated MOSFET off-time drain to source voltage
ILIMITMIN			0.180	Amperes	Minimum current limit
ILIMITTYP			0.205	Amperes	Typical current limit
ILIMITMAX			0.230	Amperes	Maximum current limit
FSMIN			124000	Hertz	Minimum switching frequency
FSTYP			132000	Hertz	Typical switching frequency
FSMAX			140000	Hertz	Maximum switching frequency
RDSON			44.20	Ohms	MOSFET drain to source resistance

Table 7. Linkswitch-XT2 Variables

Current Limit

The value of the BYPASS/MULTI-FUNCTION pin capacitor determines the device current limit setting. LinkSwitch-XT2 allows the internal current limit to be selected between two levels, Standard Current Limit and Reduced Current Limit. The choice can be selected in the spreadsheet by entering RED or STD.

Selecting the correct current limit level depends on the thermal environment, the amount of board area or use of an external heatsink, and the average output power.

Selecting RED gives the lowest current limit and results in lowest device dissipation. This minimizes heatsinking needed even in high ambient conditions. An example where RED would be selected is in a sealed adapter with minimal heat sinking.

Selecting STD gives the highest current limit and therefore maximum power from a given device. This is ideal for open frame designs, adapters where an external heatsink is attached to the SOURCE pins of the device.

Selecting STD is optimum for most applications, balancing heat dissipation and system efficiency.

PRIMARY WAVEFORM PARAMETERS					
MODE OF OPERATION			CCM		Mode of operation
KRP/KDP			0.935		Measure of continuous/discontinuous mode of operation
KP_TRANSIENT			0.536		KP under conditions of a transient
DMAX			0.516		Maximum duty cycle
TIME_ON			4.161	useconds	MOSFET conduction time at the minimum line voltage
TIME_ON_MIN			0.828	useconds	MOSFET conduction time at the maximum line voltage
IAVG_PRIMARY			0.049	Amperes	Average input current
IRMS_PRIMARY			0.077	Amperes	Root mean squared value of the primary current
LPRIMARY_MIN			1518	uH	Minimum primary inductance
LPRIMARY_TYP			1632	uH	Typical primary inductance
LPRIMARY_MAX			1476	uH	Maximum primary inductance
LPRIMARY_TOL	7		7		Primary inductance tolerance

Table 8. Primary Waveform Parameters

SECONDARY WAVEFORM PARAMETERS					
IPEAK_SECONDARY			3.118	Amperes	Peak secondary current
IRMS_SECONDARY			1.295	Amperes	Root mean squared value of the secondary current
PIV_SECONDARY			32.65	Volts	Peak inverse voltage on the secondary diode, not including the leakage spike
VF_SECONDARY			0.7	Volts	Secondary diode forward voltage drop

Table 9. Secondary Waveform Parameters

Reflected Output Voltage, V_{OR} (V)
This parameter is the secondary winding voltage reflected back to the primary through the turns ratio of the transformer (during the conduction time of the output diode). The default value is 100 V, however this can be increased up to 185 V to achieve the maximum power capability from the selected LinkSwitch-XT2 device. In general, start with the default value of 100 V, increasing the value when necessary to maintain KP above its lower limit of 0.6. For Clampless designs, there is less flexibility in selecting the value of VOR. Increasing VOR directly increases the peak Drain voltage. Therefore, for Clampless designs, a value of ≤90 V should be used and only increased once the peak Drain voltage has been measured and adequate margin (< = 90%) to BVDSS determined.

LinkSwitch-XT2 On-State DRAIN to SOURCE Voltage, V_{DSON} (V)
This parameter is the average on-state voltage developed across the DRAIN and SOURCE pins of LinkSwitch-XT2. By default, if the gray override cell is left empty, a value of 10 V is assumed. Use the default value if no better data is available.

Secondary Diode Forward Voltage Drop, $V_{F(SECONDARY)}$ (V)
Enter the average forward voltage drop of the (main) output diode. Use 0.5 V for a Schottky diode or 1 V for a ultrafast diode if no better data is available. By default, a value of 0.7 V is assumed.

Calculated Ripple to Peak Current Ratio, K_P
Below a value of 1, indicating continuous conduction mode, K_P is the ratio of ripple to peak primary current (K_{RP}). Above a value of 1, indicating discontinuous conduction mode, KP is the ratio of primary MOSFET off-time to the secondary diode conduction time (K_{DP}). The value of K_P should be in the range of $0.6 < K_P < 6$ and guidance is given in the comments cell if the value is outside this range. A value above 1 will typically result in lower noise, discontinuous conduction mode at 115 VAC, where EMI measurements are made.

Variables referenced in Step 2 are found in the "LinkSwitch-XT2 Variables, Primary Waveform Parameters and Secondary Waveform Parameters" section of the spreadsheet (see Table 7 to Table 9).

Step 3 – Transformer Construction Parameters

Core Effective Cross-Sectional Area, Ae (mm²)

Core Effective Path Length, Le (mm), Core Ungapped

Effective Inductance, AL (nH/turns²)

Volume of the Core, Ve (mm³)

Window area of the Bobbin, AW (mm)

Width of the Bobbin, BW (mm)

Mean Length per turn of the Bobbin, MLT (mm)

TRANSFORMER CONSTRUCTION PARAMETERS					
Core selection					
CORE	EE13		EE13		Select the transformer core
BOBBIN			B-EE13-H		Bobbin name
AE	17		17	mm^2	Cross sectional area of the core
LE			30.2	mm	Effective magnetic path length of the core
AL			1130.0	nH/(turns^2)	Ungapped effective inductance of the core
VE			517.0	mm^3	Volume of the core
AW			21.90	mm^2	Window area of the bobbin
BW	7.9		7.9	mm	Width of the bobbin
MLT			0.00	mm	Mean length per turn of the bobbin
MARGIN	0.00		0.00	mm	Safety margin

Table 10. Transformer Construction Parameters

By default, if the Core Type cell is left empty, the spreadsheet will select the EE13 core. The user can change this selection and choose an alternate core from a list of commonly available cores suitable for the output power (see Table 10). Changes to these values will change the power capability of a given core size, therefore Table 11 should be used for guidance only.

The gray override cells can be used to enter the core and bobbin parameters directly. This is useful if a core is selected that is not on the list or the specific core or bobbin information differs from that recalled by the spreadsheet.

Safety Margin, MARGIN (mm)
For designs that require isolation but are not using triple insulated wire for the secondary winding, the width of the safety margin to be used on each side of the bobbin should be entered here. Typically, for universal input designs, a total margin of 6.2 mm would be required; therefore a value of 3.1 mm would be entered into the spreadsheet. For vertical bobbins, the margin may not be symmetrical however, the total margin divided by 2 should still be entered.

As the margin reduces the available area for the windings, margin construction may not be suitable for small core sizes. If after entering the margin, more than 4 primary layers (L) are required, it is suggested that either a larger core be selected or switch to a zero margin design using triple insulated wire for the secondary winding.

Core Size	*Suggested Power Range*	
	100/115 or 85-265 VAC	*230 VAC Only*
EE8	*<1W*	*<1W*
EE10	*<2W*	*<2W*
EE13	*<4W*	*<4W*
EE16	*<5W*	*<6W*
EE19	*<5.6W*	*<7.1W*
EE22	*<6W*	*<8W*
EE25	*<6W*	*<9W*

Table 11. Commonly Available Cores and Power Levels at Which Cores Can be used for Typical Designs.

PRIMARY WINDING					
NPRIMARY			122		PrImary number of turns
BMAX_TARGET			1500	Gauss	Target value of the magnetic flux density
BMAX_ACTUAL			1810	Gauss	Actual value of the magnetic flux density
BAC			846	Gauss	AC flux density
ALG			110	nH/T^2	Gapped core effective inductance
LG			0.176	mm	Core gap length
LAYERS_PRIMARY	2		2		Number of primary layers
AWG_PRIMARY			38		Primary winding wire AWG
OD_PRIMARY_INSULATED			0.125	mm	Primary winding wire outer diameter with insulation
OD_PRIMARY_BARE			0.101	mm	Primary winding wire outer diameter without insulation
CMA_PRIMARY			204	mil^2/Amperes	Primary winding wire CMA

Table 12. Primary Winding Parameters.

Actual Maximum Operating Flux Density, BMAX_ACTUAL (Gauss)

The cycle skipping mode of operation used in LinkSwitch-XT2 can generate audio frequency components in the transformer. To limit this audible noise generation the transformer should be designed such that the peak core flux density is below 1500 Gauss (150 mT). Following this guideline, and using the standard transformer production technique of dip varnishing, practically eliminates audible noise. Vacuum impregnation of the transformer should not be used due to the high primary capacitance and increased losses that result

Higher flux densities are possible, however careful evaluation of the audible noise performance should be made using production transformer samples before approving the design. Audible noise may also be created by ceramic capacitors that use dielectrics such as Z5U, when used in clamp circuits may also generate audio noise. If this is the case, try replacing them with a capacitor having a different dielectric, for example a film type. Flux densities above 3000 Gauss (300 mT) are not recommended

Primary Layers, Layers_Primary

By default, if the override cell is empty, a value of 3 is assumed. Primary layers should be in the range of 1 < L < 4, and in general it should be the lowest number that meets the primary current density limit (CMA) of 200 Cmils/Amp. Values above 4 layers are possible, but the increased leakage inductance and physical fit of the windings should be considered.

For Clampless designs without a bias winding, 2 primary layers must be used. This is to ensure sufficient primary capacitance to limit the peak Drain voltage below the BVDSS rating of the internal MOSFET.

SECONDARY WINDING					
NSECONDARY	9		9		Secondary turns
AWG_SECONDARY			26		Secondary winding wire AWG
OD_SECONDARY_INSULATED			0.76	mm	Secondary winding wire outer diameter with insulation
OD_SECONDARY_BARE			0.455	mm	Secondary winding wire outer diameter without insulation
CMA_SECONDARY			247	mil^2/Amperes	Secondary winding CMA

Table 13. Secondary Winding Parameters.

Secondary Turns, $N_{SECONDARY}$

By default, if the grey override cell is left blank, the minimum number of secondary turns is calculated such that the maximum operating flux density, BM, is kept below the recommended maximum. In general, it is not necessary to enter a number in the override cell except in designs where a higher operating flux density is acceptable (see Minimizing Audible Nose section for an explanation of BM limits).

BIAS WINDING					
NBIAS	20		20		Bias turns
VF_BIAS	0.50		0.50	Volts	Bias diode forward voltage drop
VBIAS			12.67	Volts	Bias winding voltage
PIVB			74.10	Volts	Peak inverse voltage on the bias diode
CBP			1.0	uF	BP pin capacitor

Table 14. Bias Winding Parameters.

Calculated Bias Winding Turns and Voltage N_{BIAS}, V_{F_BIAS}
Where a bias winding is used, the number of turns and voltage developed are displayed. The relatively large default number of turns allows the bias to be used as a shield winding for reduced EMI. If desired, the number of turns can be adjusted by entering a value into the gray override cell.

The variables described in Step 3 are found in the "Transformer Construction Parameters, Primary Winding, Secondary Winding, and Bias Winding" section of the spreadsheet (see Table 10, Table 12, Table 13, and Table 14).

Other transformer parameters calculated in the spreadsheet are:

NPRIMARY - Primary Winding Number of Turns
ALG (nH/T^2) - Gapped Core Effective Inductance
BAC (Gauss) - AC Flux Density for Core Loss Curves (0.5 xPeak to Peak)
AWG - Primary Wire Gauge (Rounded to next smaller standard AWG value)
OD PRIMARY INSULATED (mm) - Primary winding wire outer diameter with insulation
OD PRIMARY BARE (mm) - Primary winding wire outer diameter without insulation
CMA PRIMARY (mils^2/Amp) - Primary Winding Current Capacity

Step 4 – Iterate Transformer Design and Generate Transformer Design Output

Iterate the design making sure that no warnings are displayed. Any parameters outside the recommended range of values can be corrected by following the guidance given in the right hand column.

Once all warnings have been cleared, the output transformer design parameters can be used to either wind a prototype transformer or send to a vendor for samples.

The key transformer electrical parameters are:

Primary Inductance, $L_{PRIMARY\_TYP}$ (µH)
This is the target nominal primary inductance of the transformer.

Primary Inductance Tolerance, $L_{PRIMARY\_TOL}$ (%)
This is the assumed primary inductance tolerance. A value of ±10% is used by default, however if specific information is known from the transformer vendor, then this may be overridden by entering a new value in the gray override cell.

Step 5 – Selection of Input Stage

The input stage comprises fusible resistor(s), input rectification diodes and line filter network. Flameproof fusible resistors are recommended to be chosen and depending on the differential line input surge requirements, a wire-wound type may be required. The fusible resistor(s) provides fuse safety, inrush current limiting and differential mode noise attenuation. The EMI performance of half-wave rectified designs is improved by adding a second diode in the lower return rail.

The EMI performance of half-wave rectified designs is improved by adding a second diode in the lower return rail. This provides EMI gating (EMI currents only flow when the diode is conducting) and also doubles the differential surge-withstand as the surge voltage is shared across two diodes. In designs using a single input capacitor at least one of the input diodes should be a fast type (trr < 200 ns), This reduces ringing and associated increase in EMI. Table 15 shows the recommended input stage based on output power for a universal input design while Table 4 shows how to adjust the input capacitance for other input voltage ranges.

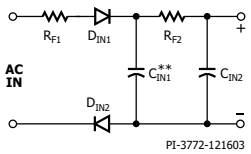
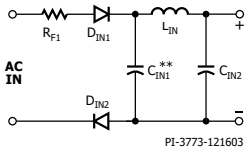
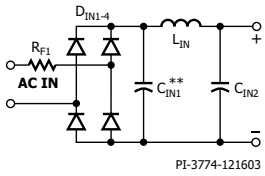
P_{OUT}	≤1 W	≤3 W	
Suggested 85 – 265 VAC Input Stage			
Component Selection Guide	R_{F1}: 8.2 Ω, 1 W Fusible R_{F2}: 100 Ω, 0.5 W, Flameproof C_{IN1}, C_{IN2}: ≥3.3 µF, 400 V each D_{IN1}, D_{IN2}: 1N4007, 1 A, 1000 V	R_{F1}: 8.2 W, 1 W Fusible L_{IN}: 470 mH – 22 mH, (0.05 A - 0.3A) C_{IN1}, C_{IN2}: ≥4 µF/W_{OUT}, 400 V each D_{IN1}, D_{IN2}: 1N4007, 1 A, 1000 V	R_{F1}: 8.2 W, 1 W Fusible L_{IN}: 470 µH - 2.2 mH, (0.05 A – 0.3 A) C_{IN1}, C_{IN2}: ≥2 µF/W_{OUT}, 400 V each D_{IN1}, D_{IN2}, D_{IN3}, D_{IN4}: 1N4007, 1 A, 1000 V
Comments	**Increase value to meet required differential line surge	**Increase value to meet required differential line surge	**Increase value to meet required differential line surge

Table 15. Input Filter Recommended Based on Total Output Power.

Step 6 – Selection of LinkSwitch-XT2 External Components

LinkSwitch-XT2 current limit can be selected using the 0805 size BYPASS pin capacitor for more stability (0.1 μF for normal current limit / 1 μF for reduce current limit). LinkSwitch-XT2 ICs select between normal and reduced current limit at power-up prior

Step 7 – Selection of Primary Clamp Circuit

For output powers of 2.5 W or below and using the LNK3604, it is possible to eliminate external clamp components by careful design of the transformer and bias winding. For Clampless designs, a 2-layer primary should be used. The resultant increase in the intra-winding capacitance limits the peak drain voltage at turn off. For output powers greater than 2 W, the winding capacitance is not sufficient to limit peak drain voltage. Therefore a bias winding should be added to the transformer and rectified with a standard recovery (rectifier) diode. Suitable diodes for the bias winding include 1N4003-1N4007. The addition of a bias winding acts as a clamp and also reduces the leakage inductance ringing and improves EMI. Table 16 summarizes the requirements between Clampless designs and designs using an external clamp.

For output powers >2.5 W, either an RCD or Zener clamp is suggested. Select the initial clamp components using the table as guide. If an RCD clamp is selected, then some empirical adjustment of the values is normally required to take account of the actual VOR and transformer leakage inductance of the design. As a general rule, minimize the value of the capacitor and maximize the value of the resistor. For both RCD and Zener clamps, verify that the peak drain voltage does not exceed 725 V at the highest input voltage and peak (overload) output power.

	Clampless		**External Clamp**
	≤2 W	2 W < P_O <2.5 W	
Bias Winding Required	N	Y	N
Device	LNK3604 only		Any
Primary layers	= 2 (no bias winding) ≤4 (with bias winding)	≤4	≤4
Recommended Transformer Parameters	Leakage inductance <90 μH Primary capacitance ≥50 pF	No Restriction	
Leakage Ring Effect on EMI	High	Medium	Low

Table 16. Factors to be Considered While Deciding Between a Clampless or External Clamp Design.

Step 8 – Selection of Output Diode and Pre-Load Resistor

MULTIPLE OUTPUT PARAMETERS					
Output 1					
VOUT1			5	Volts	Output Voltage 1
IOUT1			0.500	Amperes	Output Current 1
POUT1			2.50	Watts	Output Power 1
VD1			0.70	Volts	Secondary diode forward voltage drop for output 1
NS1			9		Number or turns for output 1
ISRMS1			1.295	Amperes	Root mean squared value of the secondary current for output 1
IRIPPLE1			1.194	Amperes	Current ripple on the secondary waveform for output 1
PIV1			32.65	Volts	Peak inverse voltage on the secondary diode for output 1
DIODE1_RECOMMENDED			SB350		Recommended diode for output 1
PRELOAD			N/A	kohms	Preload resistor to ensure a load of at leat 3mA on t he first output
CMS1			259.0	Cmils	Bare conductor effective area in circular mils for output 1
AWGS1			25	AWG	Wire size for output 1

Table 17. Multiple Output Parameters.

$V_R \geq 1.25 \times$ PIVS, where PIVS is taken from the Voltage Stress Parameters section of the spreadsheet and Transformer Secondary Design Parameters.

$I_D \geq 2 \times I_O$, where I_D the diode rated DC current and I_O is the output current.

Additionally, Table 18 lists some of the suitable Schottky and ultrafast diodes that may be used with LinkSwitch-XT2 circuits. The LinkSwitch-XT2 spreadsheet also recommends a diode based on the above guidelines (see Table 17).

Series Number	Type	VR Range	I_F	Package	Manufacturer
		V	A		
1N5817 to 1N5819	Schottky	20 - 40	1	Leaded	Vishay
SB120 to SB1100	Schottky	20 - 100	1	Leaded	Vishay
1N5820 to 1N5822	Schottky	20 - 40	3	Leaded	Vishay
SS12 to SS16	Schottky	20 - 60	1	SMD	Vishay
SS32 to SS36	Schottky	20 - 60	3	SMD	Vishay
UF4002 to UF4006	Ultrafast	100 - 600	1	Leaded	Vishay
MUR110 to MUR160	Ultrafast	100 - 600	1	Leaded	On Semi
UF5401 to UF5408	Ultrafast	100 - 800	3	Leaded	Vishay
ES1A to ES1D	Ultrafast	50 - 200	1	SMD	Vishay
ES2A to ES2D	Ultrafast	50 - 200	2	SMD	Vishay

Table 18. List of Recommended Diodes That May be used With LinkSwitch-XT2 Design.

Select the pre-load resistor such that it will sink 3 mA at the specified voltage. Note that a pre-load resistor also increases the no-load losses, so verify acceptable no-load consumption.

Step 9 – Selection of Output Capacitors

Ripple Current Rating
Select the output capacitor(s) such that the ripple rating is greater than the calculated value, IRIPPLE from the spreadsheet.
Many capacitor manufacturers provide factors that increased the allowable ripple current as the capacitor temperature is reduced or the frequency of the ripple is increased from the data sheet specified values. This should be considered to ensure the capacitor is not oversized, increasing the cost. Two or more capacitors may be used in parallel to give a combined ripple current rating equal to the sum of the individual capacitor ratings.

ESR Specification
Select a low ESR type, which gives acceptable output switching ripple. The switching ripple voltage is equal to the peak secondary current multiplied by the ESR of the output capacitor. Generally the selection the capacitor for ripple current rating will also result in an acceptable ESR

Voltage Rating
Select a voltage rating such that VRATED ≥ 1.25 × V_O.

Step 10 – Choose Feedback Scheme and Select Feedback Components

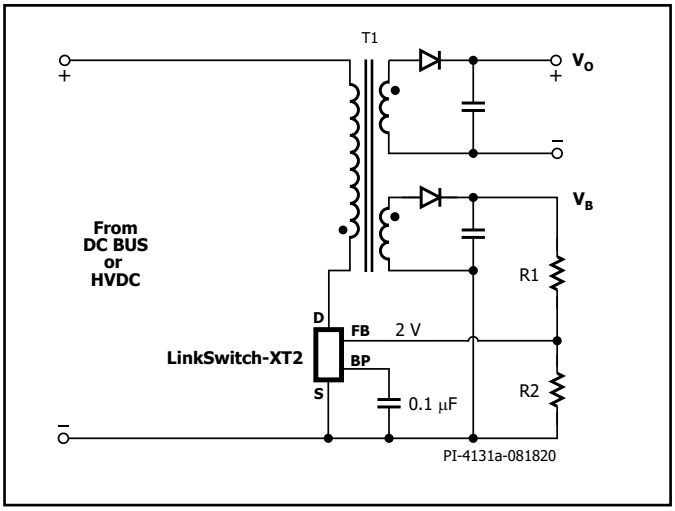


Figure 5. Primary-Side Feedback (Bias Winding Feedback) Scheme Used is a CV Only Output Characteristic Design.

FEEDBACK PARAMETERS					
DIODE_BIAS			1N4003-4007		Recommended diode is 1N4003. Place diode on return leg of bias winding for optimal EMI
RUPPER			500 – 1000	ohms	CV bias resistor for CV/CC circuit. See LinkSwitch-XT2 Design Guide
RLOWER			200 - 820	ohms	Resistor to set CC linearity for CV/CC circuit. See LinkSwitch-XT2 Design Guide

Table 19. Feedback Parameters

Two separate feedback schemes are recommended with the LinkSwitch-XT2. The first is primary-side regulated feedback (also called bias winding feedback), shown in Figure 3. This scheme relies on the bias winding to regulate the output voltage. The bias winding voltage is divided down by a resistor divider such that the feedback pin is 2 V at the specified output voltage. The output voltage is then regulated through the turns ratio of the secondary and bias windings.

In bias winding feedback, the bias winding may be placed closer to the secondary winding for tighter coupling and thus better regulations or it may be placed away from the secondary winding for loose regulation of output voltage. Bias winding feedback (for a CV only output characteristic) is shown in Figure 3 and involves selection of two resistors R1 and R2, which form a divider network to regulate the bias winding. Resistors R1 and R2 are also calculated in the design spreadsheet (see Table 19). As these resistors also draw current from the bias winding, a combined value of 8 kΩ results in a good compromise between no-load consumption and prevention of peak charging due to leakage inductance to improve load regulation.

The alternate choice is secondary-side optocoupler feedback. Here the output signal is directly sensed and fed back to the LinkSwitch-XT2 FEEDBACK pin via an optocoupler (see Figure 6). Secondary-side feedback eliminates the need for a bias winding and is more accurate then primary-side (bias winding) feedback. However, it requires additional components and is higher cost compared to bias winding feedback. Both of these schemes are also summarized in Table 5.

Tips for Clampless designs

The mechanical construction of the transformer plays a crucial role in Clampless designs. Care should be taken to reduce the leakage inductance and increase the intra-winding capacitance of the primary winding. Intra-winding capacitance is defined as the capacitance measured from one end of a winding to the other end while all other windings are open. This is best achieved by using a 2-layer primary winding as noted in Figure 7. It is common to use a layer of tape between 2 primary layers. This should be avoided for Clampless designs, as this tends to reduce intra-winding capacitance. Even with the increased winding capacitance, no-load power of < 100 mW is easily possible with LinkSwitch-XT2. For typical Clampless designs, the leakage inductance is below 90 µH and the intra-winding capacitance is greater than 40 pF.

Figure 8 shows the factors to be considered while deciding the mechanical structure of the transformer.

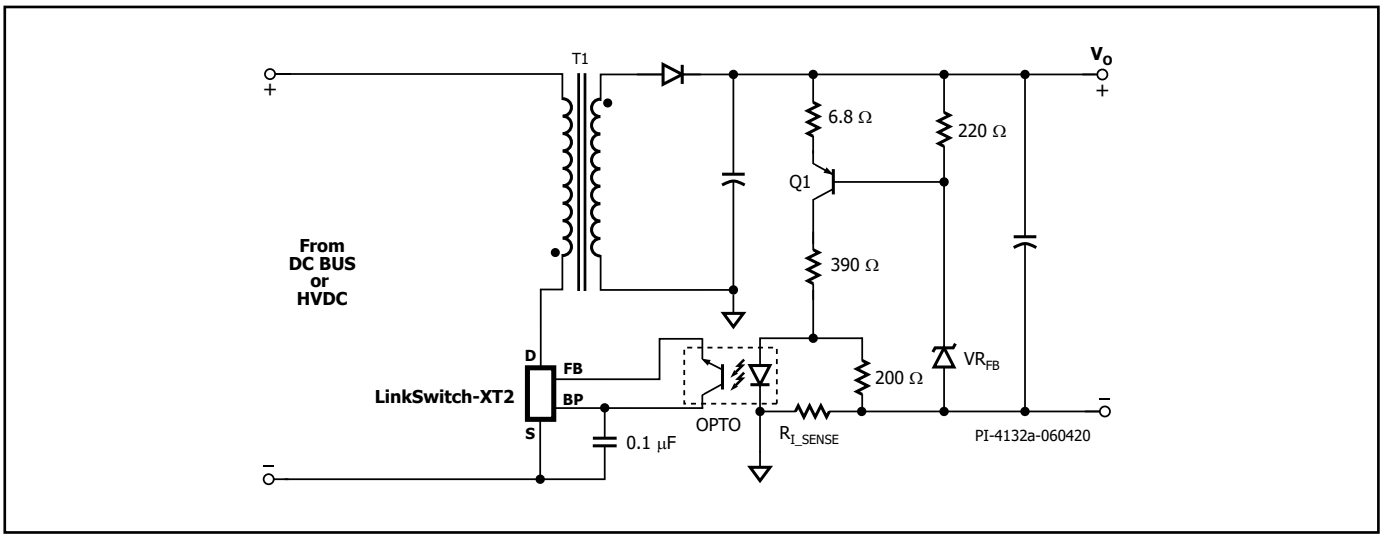


Figure 6. Secondary-Side Feedback Scheme Used for a CV/CC Output Characteristic Design.

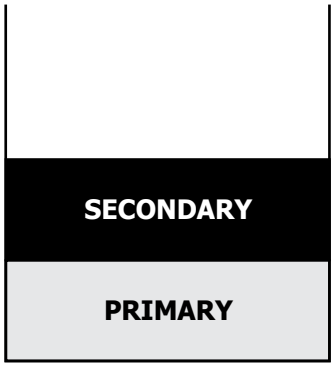
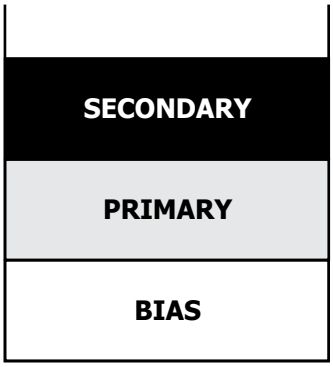
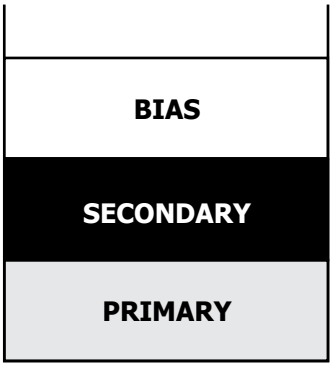
 (a)	 (b)	 (c)
• No bias winding • For Clampless designs use 2 primary layers, LNK3604 and ≤ 2 W only	• For Clampless LNK3604 designs and ≤ 2.5 W only • Bias winding feedback ideal for designs that require loosely regulated output voltage • Improved EMI performance over (a) & (c) due to reduction in leakage inductance ringing	• For Clampless LNK3604 designs, 2 primary layers and ≤ 2 W only • Provides best output voltage regulation with bias winding feedback

Figure 7. Mechanical Structure of the Transformer in LinkSwitch-XT2 Designs.

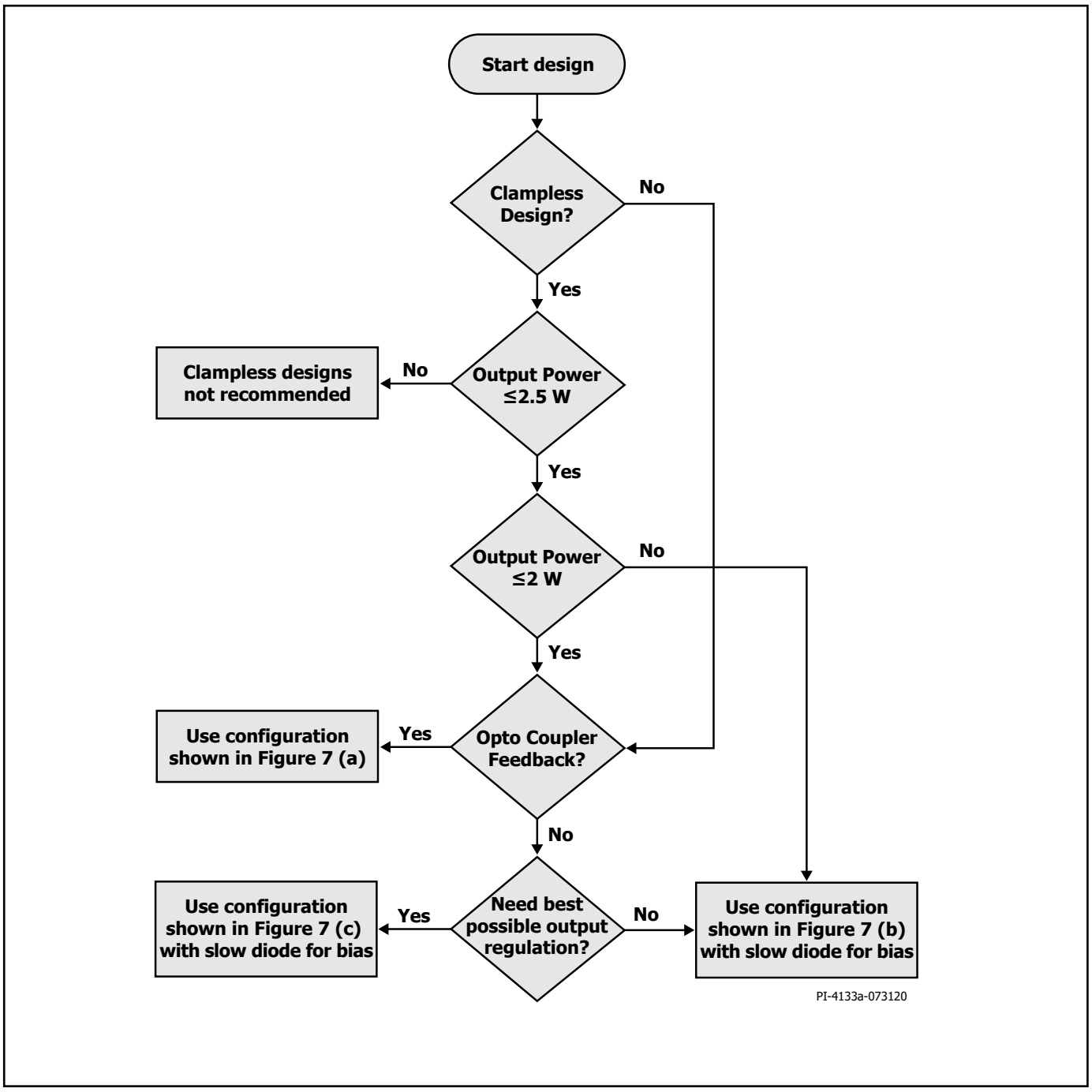


Figure 8. Flowchart for Deciding Mechanical Structure of Transformer.

Key Application Considerations

LinkSwitch-XT2 Design Considerations Output Power Table

The data sheet maximum output power table (Table 1) represents the maximum practical continuous output power level that can be obtained under the following assumed conditions:

1. The minimum DC input voltage is 90 V or higher for 85 VAC input, or 240 V or higher for 230 VAC input or 115 VAC with a voltage doubler. The value of the input capacitance should be large enough to meet these criteria for AC input designs.
2. Secondary output of 6 V with a fast PN rectifier diode.
3. Assumed efficiency of 70%.
4. Voltage only output (no secondary-side constant current circuit).
5. A primary clamp (RCD or Zener) is used.
6. The part is board mounted with SOURCE pins soldered to a sufficient area of copper to keep the SOURCE pin temperature at or below 100 °C.
7. Ambient temperature of 50 °C for open frame designs and an internal enclosure temperature of 60 °C for adapter designs.

Discontinuous mode operation (KP > 1) is recommended for LNK3604. Below a value of 1, KP is the ratio of ripple to peak primary current. Above a value of 1, KP is the ratio of primary power MOSFET OFF-time to the secondary diode conduction time. Due to the flux density requirements described below, typically a LinkSwitch-XT2 design will be discontinuous, which also has the benefits of allowing fast (instead of ultrafast) output diodes and reducing EMI.

Clampless Designs
Clampless designs rely solely on the drain node capacitance to limit the leakage inductance induced peak drain-to-source voltage. Therefore, the maximum AC input line voltage, the value of VOR, the leakage inductance energy, a function of leakage inductance and peak primary current, and the primary winding capacitance determine the peak drain voltage. With no significant dissipative element present, as is the case with an external clamp, the longer duration of the leakage inductance ringing can increase EMI.

The following requirements are recommended for a universal input or 230 VAC only clampless design:

1. A clampless design should only be used for PO ≤ 2.5 W, using the reduced current limit mode (CBP = 1 μF) and a VOR** ≤ 90 V.
2. For designs where PO ≤ 2 W, a two-layer primary should be used to ensure adequate primary intra-winding capacitance in the range of 25 pF to 50 pF.
3. For designs where 2 < PO ≤ 2.5 W, a bias winding should be added to the transformer using a standard recovery rectifier diode to act as a clamp. This bias winding may also be used to externally power the device by connecting a resistor from the bias-winding capacitor to the BYPASS pin. This inhibits the internal high-voltage current source, reducing device dissipation and no-load consumption.
4. For designs where PO > 2.5 W clampless designs are not practical and an external RCD or Zener clamp should be used.
5. Ensure that worst-case high line, peak drain voltage is below the BVDSS specification of the internal power MOSFET and ideally < VDSS × 0.9 to allow margin for design variation.

†For 110 VAC only input designs it may be possible to extend the power range of clampless designs to include the standard current limit mode. However, the increased leakage ringing may degrade EMI performance.

**VOR is the secondary output plus output diode forward voltage drop that is reflected to the primary via the turns ratio of the transformer during the diode conduction time. The VOR adds to the DC bus voltage and the leakage spike to determine the peak drain voltage.

Audible Noise
The cycle skipping mode of operation used in LinkSwitch-XT2 ICs can generate audio frequency components in the transformer. To limit this audible noise generation, the transformer should be designed such that the peak core flux density is below 1500 gauss (150 mT). Following this guideline and using the standard transformer production technique of dip varnishing practically eliminates audible noise. Vacuum impregnation of the transformer should not be used due to the high primary capacitance and increased losses that result. Higher flux densities are possible, however careful evaluation of the audible noise performance should be made using production transformer samples before approving the design.

Ceramic capacitors that use dielectrics, such as Z5U, when used in clamp circuits may also generate audio noise. If this is the case, try replacing them with a capacitor having a different dielectric or construction, for example a film type.

LinkSwitch-XT2 Layout Considerations

See Figures 9, 10, 11 and 12 for a recommended circuit board layout for LinkSwitch-XT2 (D, P and G packages).

Single Point Grounding
Use a single point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pins.

Bypass Capacitor CBP
The BYPASS pin capacitor should be located as near as possible to the BYPASS and SOURCE pins.

Primary Loop Area
The area of the primary loop that connects the input filter capacitor, transformer primary and LinkSwitch-XT2 IC together should be kept as small as possible.

Primary Clamp Circuit
A clamp is used to limit peak voltage on the DRAIN pin at turn-off. This can be achieved by using an RCD clamp or a Zener (~200 V) and diode clamp across the primary winding. In all cases, to minimize EMI, care should be taken to minimize the circuit path from the clamp components to the transformer and LinkSwitch-XT2 IC.

Thermal Considerations
The copper area underneath the LinkSwitch-XT2 IC acts not only as a single point ground, but also as a heat sink. As this area is connected to the quiet source node, it should be maximized for good heat sinking of LinkSwitch-XT2 IC. The same applies to the cathode of the output diode.

Y Capacitor
Y capacitor is generally not used for this power level. If used, the placement of the Y type capacitor should be directly from the primary input filter capacitor positive terminal to the common/ return terminal of the transformer secondary. Such a placement will route high magnitude common mode surge currents away from the LinkSwitch-XT2 device. Note that if an input pi (C, L, C) EMI filter is used, then the inductor in the filter should be placed between the negative terminals of the input filter capacitors.

Feedback Signal
Place the transistor Q2 physically close to the LinkSwitch-XT2 IC to minimize trace lengths from the transistor to FEEDBACK pin. Keep the high current, high-voltage drain and clamp traces away from the feedback signal to prevent noise pick up.

Output Diode

For best performance, the area of the loop connecting the secondary winding, the output diode and the output filter capacitor should be minimized. In addition, sufficient copper area should be provided at the anode and cathode terminals of the diode for heat sinking. A larger area is preferred at the quiet cathode terminal. A large anode area can increase high frequency radiated EMI.

Quick Design Checklist

As with any power supply design, all LinkSwitch-XT2 designs should be verified on the bench to make sure that component specifications are not exceeded under worst-case conditions. The following minimum set of tests is strongly recommended:

1. Maximum drain voltage – Verify that V_{DS} does not exceed 90% of BV_{DSS} at the highest input voltage and peak (overload) output power. The 10% margin versus BV_{DSS} specification gives margin for design variation, especially in clampless designs.
2. Maximum drain current – At maximum ambient temperature, maximum input voltage and peak output (overload) power, verify drain current waveforms for any signs of transformer saturation and excessive leading edge current spikes at start-up. Repeat under steady state conditions and verify that the leading-edge current spike event is below $I_{LIMIT(MIN)}$ at the end of the $t_{LEB(MIN)}$. Under all conditions, the maximum drain current should be below the specified absolute maximum ratings.
3. Thermal Check – At specified maximum output power, minimum input voltage and maximum ambient temperature, verify that the temperature specifications are not exceeded for LinkSwitch-XT2 IC, transformer, output diode and output capacitors. Enough thermal margin should be allowed for part-to-part variation of the $R_{DS(ON)}$ of LinkSwitch-XT2 IC as specified in the data sheet. Under low-line, maximum power, a maximum LinkSwitch-XT2 IC SOURCE pin temperature of 100 °C is recommended to allow for these variations.

Design Tools

Up-to-date information on design tools can be found at the Power Integrations website: www.power.com

Layout Considerations

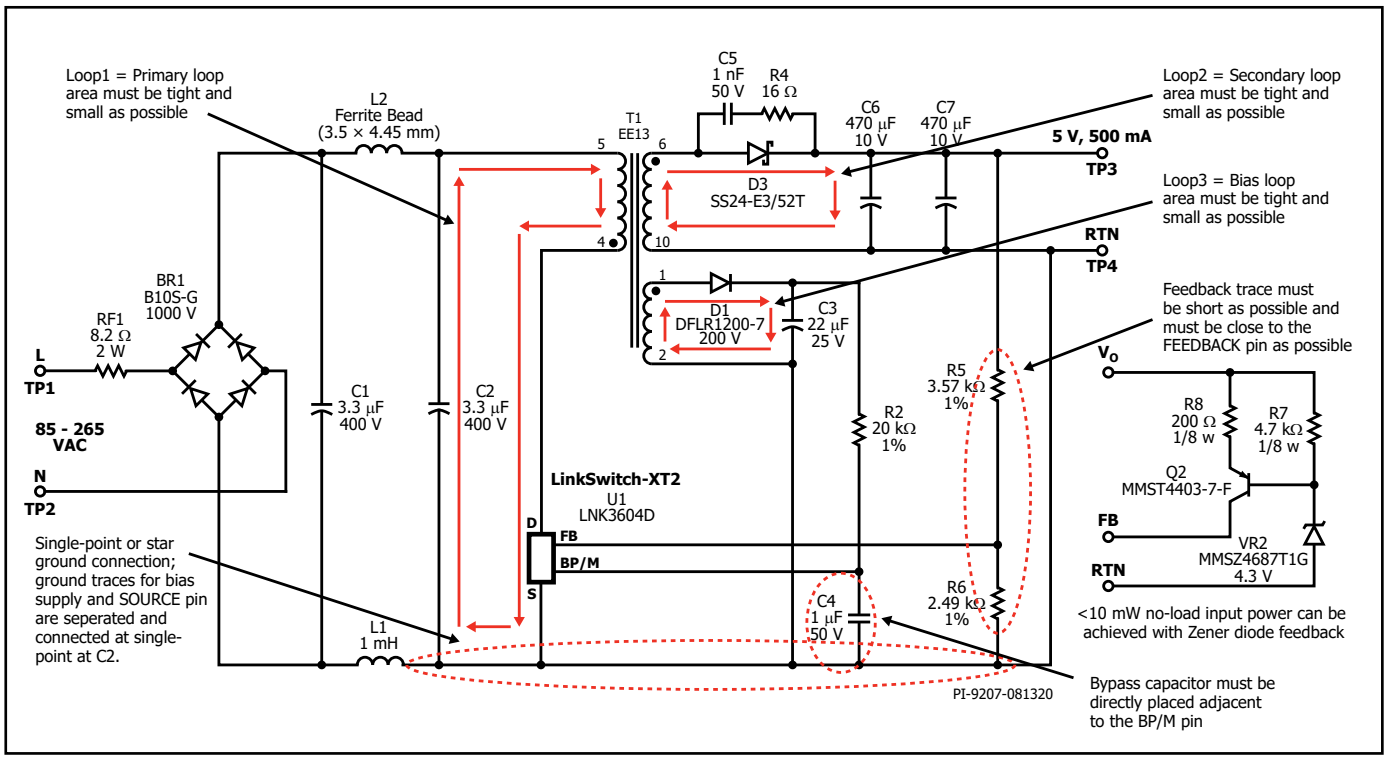


Figure 9. Typical Schematic of LinkSwitch XT2 Critical Loops Area, Critical Component Traces and Single-Point or Star Grounding.

Layout Example

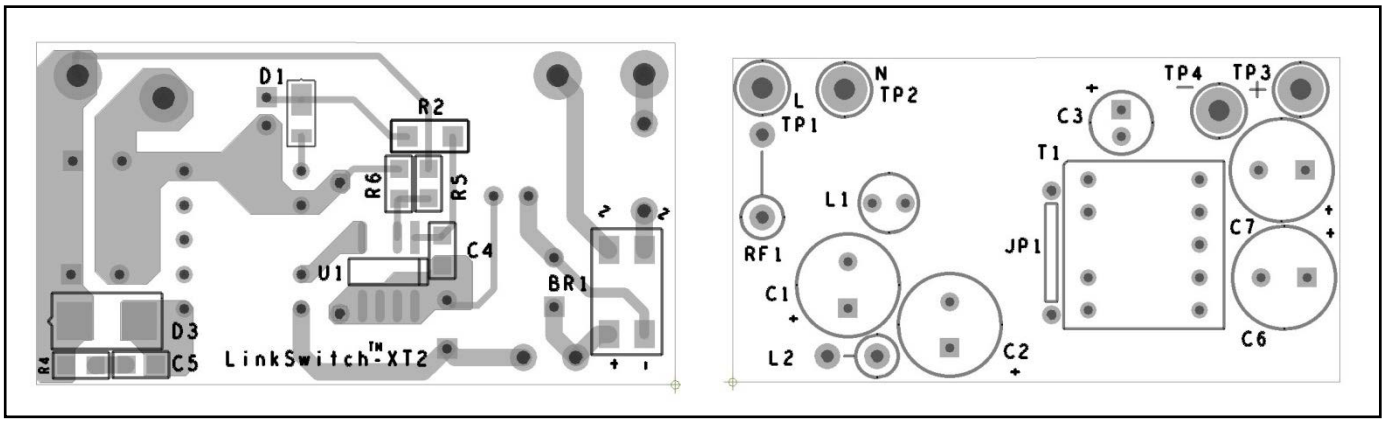


Figure 10. Recommended Printed Circuit Layout for LinkSwitch-XT2 using D Package in a Flyback Converter Configuration (Bottom Left, Top Right).

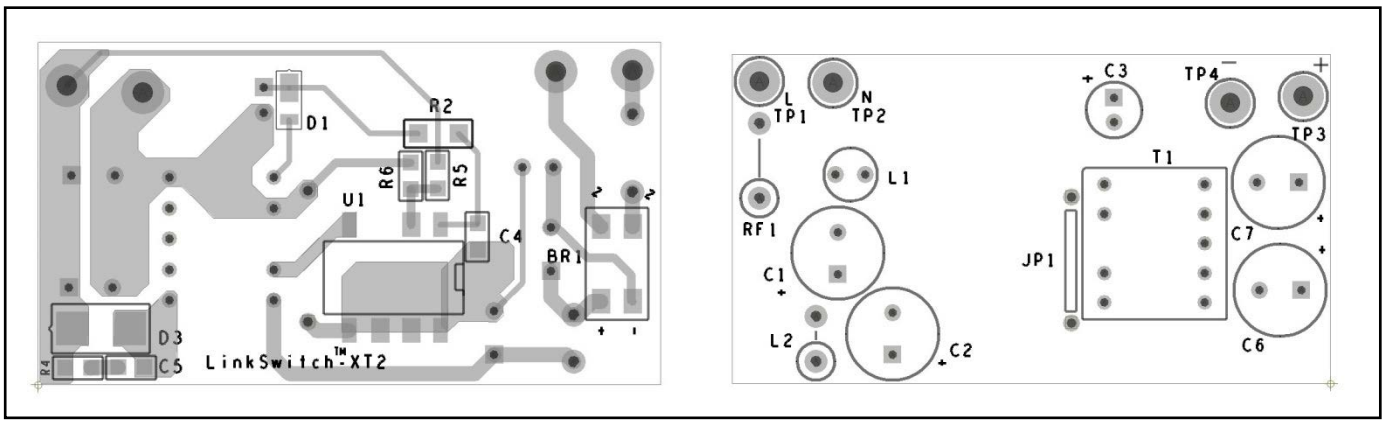


Figure 11. Recommended Printed Circuit Layout for LinkSwitch-XT2 using G Package in a Flyback Converter Configuration (Bottom Left, Top Right).

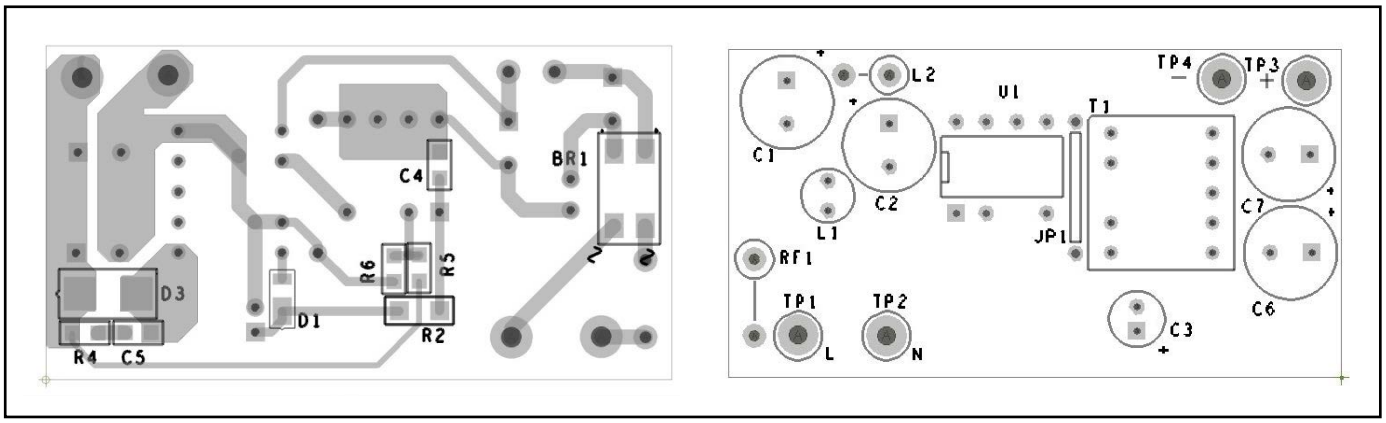


Figure 12. Recommended Printed Circuit Layout for LinkSwitch-XT2 using P Package in a Flyback Converter Configuration (Bottom Left, Top Right).

Appendix A – Application Example

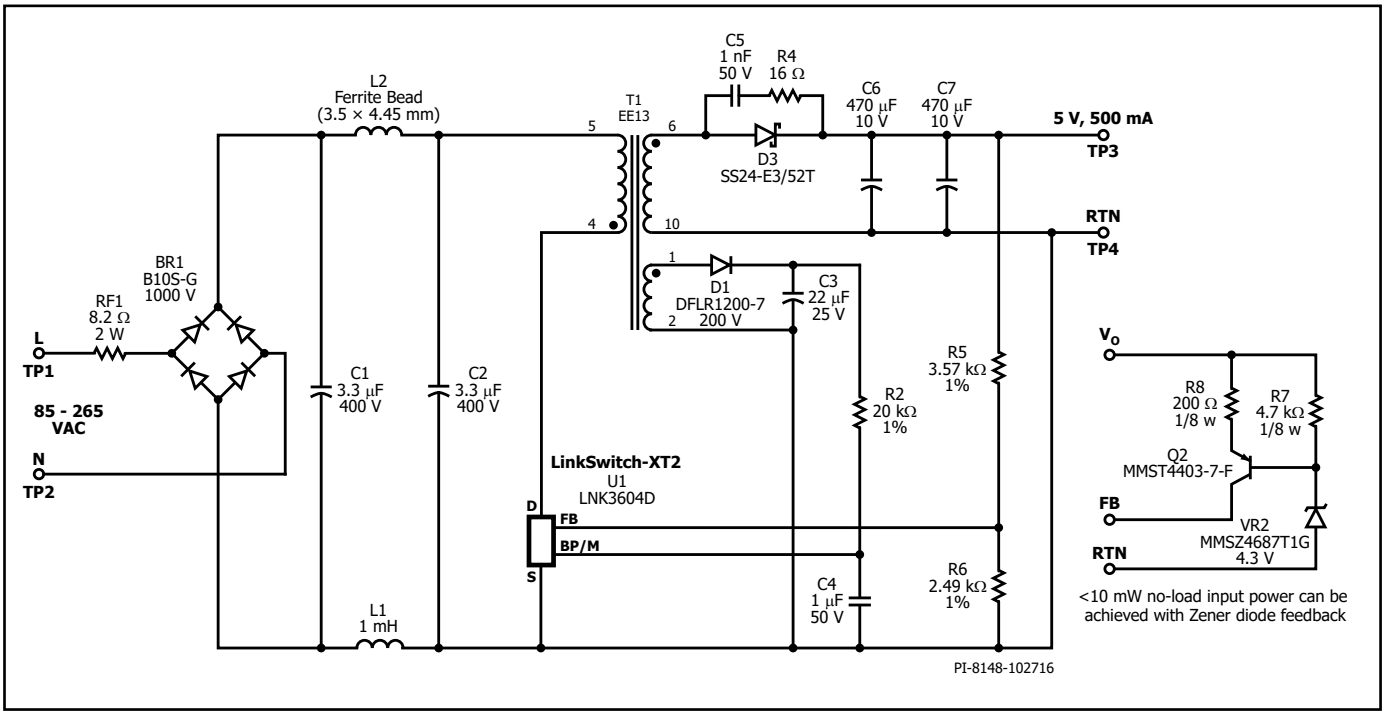


Figure 13. Schematic Diagram of a 5 V, 500 mA (2.5 W) Design.

A 5 V, 500 mA (2.5 W) Design

The schematic shown in Figure 13 is a typical implementation of a universal input, 5 V ±5%, 500 mA adapter using LNK3604D. This circuit makes use of the clampless technique to eliminate the primary clamp components and reduce the complexity of the circuit.

The EcoSmart features built into the LinkSwitch-XT2 family allow this design to easily meet all current and proposed energy efficiency standards, including the mandatory California Energy Commission (CEC) requirement for average operating efficiency.

The AC input is rectified by bridge rectifier BR1 and filtered by the bulk storage capacitors C1 and C2. Resistor RF1 is a flameproof, fusible, wire wound type and functions as a fuse, inrush current limiter and, together with the filter formed by C1, C2, L1 and L2, differential mode noise attenuator.

This simple input stage, together with the frequency jittering of LinkSwitch-XT2 ICs, and PI's E-Shield™ windings within T1, allow the design to meet both conducted EMI limits with ≥10 dBV margin.

The rectified and filtered input voltage is applied to the primary winding of T1. The other side of the primary is driven by the integrated power MOSFET in U1. No primary clamp is required as the low value and tight tolerance of the LNK3604D IC's internal current limit allows the primary winding capacitance of the transformer and drain-source capacitance of the power MOSFET in the LNK3604D to provide adequate clamping of the leakage inductance drain voltage spike. The secondary of the flyback transformer T1 is rectified by D3, a Schottky diode, and filtered by C6, C7, low ESR capacitor. The output voltage is sensed via resistor divider R5 and R6. Output voltage is regulated so as to achieve a voltage of 2 V on the FEEDBACK pin. To achieve <10 mW no-load input power, we can also use the Zener to do the feedback sense. The combined voltage drop across VR2, emitter to base voltage drop of transistor Q2 ($V_{EB(Q2)}$) and R8 determines the output voltage. When the output voltage exceeds this level, current will flow through transistor Q2. As the current increases, the current fed into the FEEDBACK pin of U1 increases until the turnoff threshold current (~49 µA) is load, almost all switching cycles will be enabled, and at very light loads, almost all the switching cycles will be disabled, giving a low effective frequency and providing high light load efficiency and low no-load consumption.

Resistor R7 provides ≈150 µA through VR2 to bias the Zener diode closer to its test current. The diode used is a low test current Zener diode which needs only 50 µA to conduct, this will provide <10 mW no-load input power. Resistor R8 limits the current into FEEDBACK pin to less than 1.2 mA for protection. For higher output accuracy, the Zener diode may be replaced with a reference IC such as the TL431.

The LinkSwitch-XT2 ICs can be completely self-powered from the DRAIN pin, requiring only a small ceramic capacitor C4 connected to the BYPASS pin. Resistor R2 supplies the BYPASS pin externally from the auxiliary winding for significantly lower no-load input power and increased efficiency over all load conditions. To achieve lowest no-load power consumption, the current fed into the BYPASS pin should be slightly higher than 120 µA. For the best full load efficiency and thermal performance, the current fed into the BYPASS pin should be slightly higher than 257 µA.

Appendix B

In-Depth Information

The In-depth Information section is divided into two parts. The first part discusses the Continuous Mode or CCM operation of flyback power supply. The second part is for Discontinuous Mode or DCM operation. The other steps and design equations in the first part are also applicable for DCM and it will be noted to reference those steps for designing power supply in DCM operation.

I. Continuous Conduction Mode

Step 1 – Determine System Requirements: VAC_{MIN}, VAC_{MAX}, f_L, V_O, P_O, η

Determine input voltage using Table 20 as guidelines for the standard worldwide Input Voltage and Line Frequency.

Input (VAC)	V_{ACMIN} (VAC)	V_{ACMAX} (VAC)
110/115	85	132
230	195	265
Universal	85	265

Table 20. Input Voltage Range.

Efficiency η is the ratio of output power to input power. Since efficiency can vary significantly with output voltage due to secondary diode loss, it is best to use a number that is representative of similar power supplies. Switching power supply efficiencies typically range from 75% for supplies delivering most of their power at low voltage outputs (5 V or 3.3 V) to 85% for those supplying most of their power through higher voltage outputs (12 V and above). If this data is not available, 80% is a reasonable choice.

Step 2 – Decide on Feedback / Sense Circuit

There are two types of feedback/sense circuits presented in this document. First is the bias winding feedback implementation as seen on Figure 3. The other is the optocoupler with a zener diode sense implementation as seen on Figure 4 and it is reasonably accurate, particularly at output voltages higher than 5 V.

Step 3 – Determine the Input Capacitor C_{IN} and Minimum DC Input Voltage V_{MIN}

When the full-wave rectified AC line is filtered with an input capacitance C_{IN} (C_{IN1} + C_{IN2} in Figure 13). The resulting high-voltage DC bus has a ripple voltage as shown in Figure 14. The minimum DC voltage V_{MIN} occurring at the lowest line voltage V_{ACMIN} is an important parameter for the design of the power supply. A rule of thumb on choosing the C_{IN} value is to use 2 to 3 μF/watt of output power for 100/115 VAC or universal input, and 1 μF/Watt of output power for 230 VAC. The C_{IN} value obtained by using this rule represents a nearly optimum design in terms of system cost in most applications.

The accurate calculation of V_{MIN} for a given C_{IN} (or vice versa) is a very complicated task which involves the solving of an equation with no closed form solution. The equation shown below represents a good first order approximation which is accurate enough for most situations.

$$V_{MIN} = \sqrt{(2 \times V_{ACMIN}^2) - \frac{2 \times P_O \times \left(\frac{1}{2 \times f_L} - t_C\right)}{\eta \times C_{IN}}}$$

The bridge rectifier conduction time tc is typically at 3 msec, and can be verified by direct measurement.

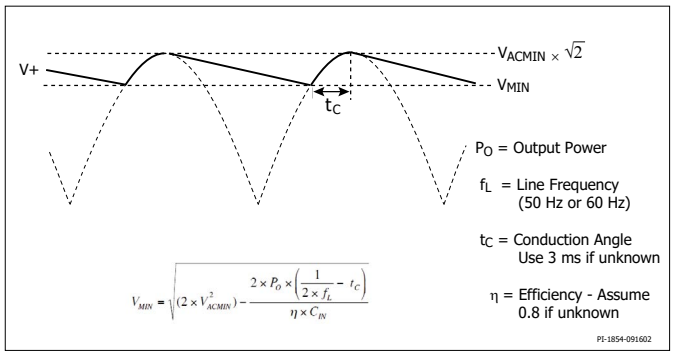


Figure 14. Input Voltage Waveform.

Step 4 – Select Output Diode and Estimate Associated Efficiency Loss

The output diode can be selected based on expected power supply efficiency and cost.

- Use a Schottky diode for highest efficiency requirements especially for low output voltages such 3.3 V and 5 V.
- Output voltages higher than 5 V can use an Ultrafast diode.
- If efficiency is not a concern or cost is paramount, use a Fast PN-diode.
- The Schottky and Ultrafast may be used with continuous mode of operation. And Fast PN-diode should only be used for discontinuous mode of operation.
- Choose output diode type.
- Output diode efficiency loss is the power supply efficiency reduction cause by the diode. Table 21 shows the estimated efficiency loss percentage with different types of output rectifier diode.
- The final diode current rating is to be determined after accommodating the continuous short circuit current I_{OS}.

Diode Type	V_D (V)	Efficiency Loss
Schottky	0.5	$(0.5/V_O) \times 100\%$
Ultrafast	1.0	$(1.0/V_O) \times 100\%$
Fast	1.0	$(1.0/V_O) \times 100\%$

Table 21. Diode Forward Voltage and Efficiency Loss.

Step 5 – Determine Output Diode Peak Inverse Voltage (PIV). Calculate Reflected Output Voltage V_{OR} Based on V_{MAX}, V_O, V_D and PIV

When the power MOSFET integrated to the LinkSwitch-XT2 IC is off and the secondary is conducting, the voltage on the secondary is reflected to the primary side of the transformer by the turns ratio. This reflected voltage VOR adds to the input DC voltage at the LinkSwitch-XT2 drain node. Worst case voltage at the drain occurs at high line when the DC input voltage is at its maximum value. The maximum DC input voltage can be calculated as:

$$V_{MAX} = \sqrt{2} \times V_{ACMAX}$$

Look up output diode rectifier reverse voltage VR from the diode datasheet.

Calculate maximum peak inverse voltage PIV. The usual maximum recommended PIV is 80% of the reverse voltage rating VR.

PIV = 0.8 x VR

Calculate the reflected output voltage V_{OR}:

$$V_{OR} = \frac{V_{MAX} \times (V_O + V_D)}{PIV - V_O}$$

- VOR must be less than 135 V.
- A good starting value for < 20 W output power is to set V_{OR} equals to 100 V.
- Higher than 20 W, set V_{OR} between 100 V – 110 V.

Step 6 – Choose LinkSwitch™-XT2 -4 Based on Input Voltage Range and Output Power

Select appropriate LinkSwitch-XT2 according to Table 22 for LinkSwitch-XT2 for family of devices.

Output Power Table

Products	Peak or Open Frame[1,2]	
	725 V MOSFET	
	230 VAC ± 15%	85-265 VAC ± 15%
LNK3604P/G/D	9.2 W	6.1 W
Products	900 V MOSFET	
	230 VAC ± 15%	85-265 VAC ± 15%
LNK3694P/G/D	6 W	4 W
LNK3696P/G/D	11 W	8 W

Table 22. LinkSwitch-XT2 Family of Devices.

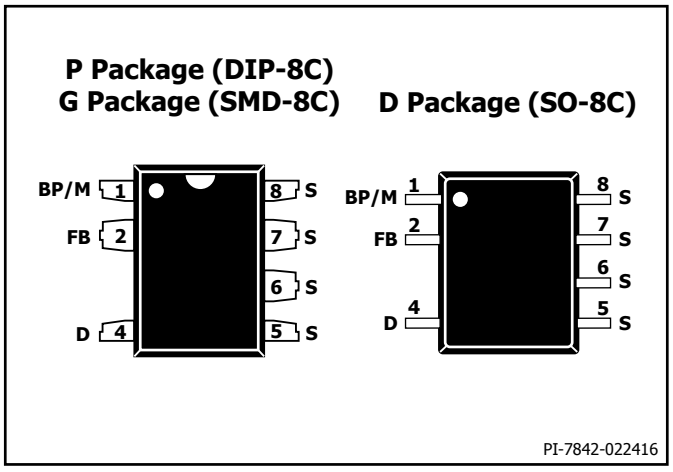


Figure 15. Pin Configuration.

Step 7 – Determine Maximum Duty Cycle D_{MAX} at Low-Line Using V_{OR} and V_{MIN}

For Continuous Mode Operation:

$$D_{MAX} = \frac{V_{OR}}{V_{OR} + (V_{MIN} - V_{DS})}$$

V_{DS} is the average Drain to Source voltage during LinkSwitch-XT2 ON-time. Set V_{DS} to approximately 10 V which results in a slight increase in D_{MAX}.

Higher V_{MIN} directly increases the output power capability of a given LinkSwitch-XT2 , while lower V_{MAX} allows larger V_{OR} and consequently larger D_{MAX} which also increases the output power of a given LinkSwitch-XT2 .

Step 8 – Calculate K_{RP} from V_{MIN}, P_O, η, I_P and D_{MAX}

KRP is the ratio between the primary ripple current IR and primary peak current IP.

The average DC current I_{AVG} at low line is simply the input power divided by V_{MIN}, where the input power is equal to the output power divided by the efficiency.

$$I_{AVG} = \frac{P_{OUT}}{\eta V_{MIN}}$$

By combining the above equations for I_P and I_{AVE}, K_{RP} can be expressed as:

$$K_{RP} = \frac{2 \times (I_P \times D_{MAX} \times \eta \times V_{MIN} - P_O)}{I_P \times D_{MAX} \times \eta \times V_{MIN}}$$

Primary ripple current can be easily derived as,

$$I_R = I_P \times K_{RP}$$

Figure 16a and 16b depicts the primary drain current waveform shapes both continuous and discontinuous mode respectively.

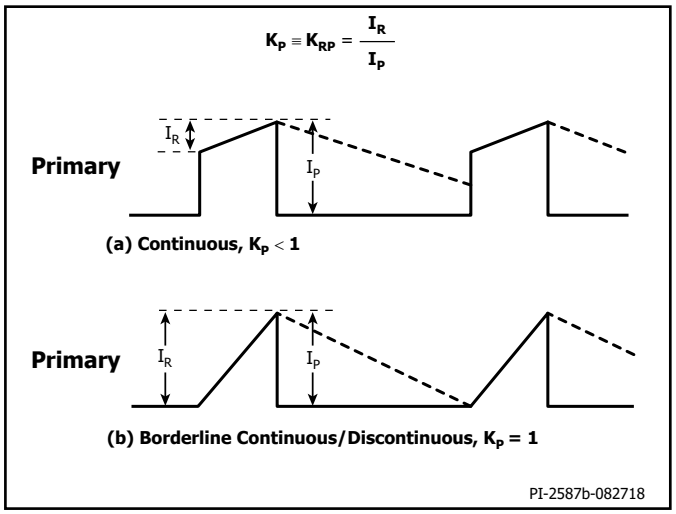


Figure 16. Primary Drain Current and Secondary Diode Current Waveforms.

Step 9 – Check KRP Against 0.6

If K_{RP} > 0.6, go to Step 10.
If K_{RP} < 0.6, set K_{RP} = 0.6, then follow the process below.

- Recalculate D_{MAX} using Step 7 equation.
- Recalculate V_{OR} using Step 5 equation.
- If V_{OR} < 135 V, go to Step 10.
- If V_{OR} > 135 V, go back to Step 6 and select higher current LinkSwitch-XT2 .

Step 10 – Calculate Primary Inductance, L_p

Continuous Mode:

$$L_P = \frac{10^6 \times P_O}{K_{RP} \times \left(1 - \frac{K_{RP}}{2}\right) \times \frac{1}{0.9} \times I_P^2 \times f_S} \times \frac{Z \times (1 - \eta) + \eta}{\eta}$$

The η is the efficiency and Z is the loss factor. If Z = 1, all losses are on the secondary side. If Z = 0, all losses are on the primary side. Z is simply the ratio of secondary loss to total loss. If no better reference information is available, Z should be set to 0.5.

- I_p is the minimum I_{LIMIT} from LinkSwitch-XT2 data sheet as previously defined in Step 8.
- f_S is the minimum switching frequency from LinkSwitch-XT2 data sheet.
- Not the cancellation effect between the over-temperature variations of I_p and f_S resulting in the additional 1/0.9 term.
- Z is the loss allocation factor.

Primary Inductance (L_p) Tolerance

For transformer design manufacturability, the design engineer needs to provide the desired tolerance of the primary inductance. A good design approach typically uses ±10% tolerance of the calculated primary inductance (L_p).

In order to ensure the minimum primary inductance requirement, the +10% should be added on the total required primary inductance.

Step 11 – Transformer Design

- Calculate turns ratio N_P/N_S:

$$N_P = N_S \times \frac{V_{OR}}{V_O + V_D}$$

- Select core and bobbin.

AN-18 Appendix A also provides a table of recommended core types for various power ranges. For single output designs, a triple insulated secondary simplifies transformer construction and allows the use of the smallest size core and bobbin for a given output power. Margin winding, which is suitable for both single and multiple output secondaries, will require wider bobbins and therefore, longer/taller cores. If there is no specific form factor requirement, it is best to start with the smallest EE type core for the power level. EE cores are usually the least expensive type. The two-digit number following the core type indicates the core size in mm. For 100 kHz operation, the selection of core material is not very critical. TDK PC40 material is a good first choice. Other ferrite materials with similar characteristics are available from many manufacturers such as Philips 3C85 and its equivalent will also work at 100 kHz, and could be used if there is a cost advantage.

Once a core has been selected from the catalog, a suitable bobbin can be easily identified.

Manufacturer specified core parameters Ae, Le, AL and bobbin parameter BW are usually found in the same catalog.

- Calculate primary and secondary number of turns for peak flux density (B_p) not to exceed 1500 Gauss. Limit B_p to 1500 Gauss for low audio noise designs. Use the lowest practical value of B_p for the greatest reduction in audio noise. See AN-24 for additional information regarding audio noise suppression technique.
- There are different means to determine number of turns for each winding. One is to calculate first the primary number of turns (N_p) by choosing maximum flux density B_p to be less than 3000 Gauss. Knowing L_p and I'_p from previous steps we can calculate N_p as:

$$N_P = 100 \times I'_P \times \frac{L_P}{B_P \times A_E}$$

Where I'_p equals to maximum I_{LIMIT}.

Another way is to select the secondary number of turns, NS which the spreadsheet applied. A good starting point is to pick the number for the secondary turns. Using 1 turn/volt for 100/115 VAC and 0.6 turn/volt for 230 VAC or universal inputs is a good assumption. As an example, for a 115 VAC and an output VO of 12 V plus the rectifier

forward drop V_D of 0.7, a 13 turn secondary would be used as the initial value. The primary number of turns N_P is related to the secondary number of turns N_S by the ratio between V_{OR} and $V_O + V_D$.

- Calculate secondary number of turns, N_P:

$$N_P = N_S \times \frac{V_{OR}}{V_O + V_D}$$

- Similarly, the number of bias windings NB can be derived from

$$N_B = N_S \times \frac{V_B + V_{DB}}{V_O + V_D}$$

V_B is the bias voltage, and V_{DB} is the bias rectifier forward voltage drop.

- Then after determining the primary number of turns N_P, another critical parameter that must be checked is the maximum flux density in the core (B_M).

$$B_M = \frac{100 \times I_P \times L_P}{N_P \times A_E}$$

Where, A_e is the effective cross sectional area of the core. The primary inductance L_P, calculated from Step 10. And I_P or the primary current which is already given.

- Calculate gap length L_g. Gap length should be larger than 0.1 mm to ensure manufacturability.

$$L_g = 40 \times \pi \times A_e \times \left(\frac{N_P^2}{1000 \times L_P} - \frac{1}{A_L} \right)$$

The core cross sectional Ae and ungapped effective inductance A_L can be found from the datasheets of the core. L_g is usually incorporated as an air gap ground into the center leg of the core and needs to be at least 51 µm or 2 mils for manufacturability. If L_g is less than 51 µm, once again the core size or N_P must be increase.

One other parameter always required by transformer manufacturer is the gapped core effective inductance A_{LG}, which can be determined only after N_P is fixed:

$$A_{LG} = 1000 \times \frac{L_P}{N_P^2}$$

Step 12 – Calculate Primary RMS Current I_{RMS}, Secondary Peak Current I_P, RMS current I_{SRMS} and Output Ripple Current I_{RIPPLE}

Continuous Mode:

- Calculate primary RMS current I_{RMS}

$$I_{RMS} = I_P \times \sqrt{D_{MAX} \times \left(\frac{K_{RP}^2}{3} - K_{RP} + 1 \right)}$$

- Calculate secondary peak current I_{SP} and can be derived from the primary peak current I_p and the turns ratio between primary and secondary N_P/N_S

$$I_{SP} = I_P \times \frac{N_P}{N_S}$$

- Calculate secondary RMS current I_{SRMS}. The K_{RP} of the secondary is always identical to that of the primary, since it is only a reflected version of the primary current with the duty cycle (1-D). Therefore, the secondary RMS current I_{SRMS} can be expressed in a manner similar to the primary RMS current, only with D_{MAX} replaced by $(1 – D_{MAX})$.

$$I_{SRMS} = I_{SP} \times \sqrt{(1 - D_{MAX}) \times \left(\frac{K_{RP}^2}{3} - K_{RP} + 1 \right)}$$

I_{RIPPLE} is the RMS ripple current of the output capacitor and it is calculated as:

$$I_{RIPPLE} = \sqrt{I_{SRMS}^2 - I_O^2}$$

I_O is the power supply output current which can be calculated as:

$$I_O = \frac{P_O}{V_O}$$

Step 13 – Determine Wire Gauge Both on Primary and Secondary

From the core and bobbin size, it is possible to determine the outside diameter of the primary wire OD in mm that is required to accommodate the primary turns on one or two full layers allowing for margins as appropriate.

$$OD = \frac{BW_E}{N_P}$$

BW_E is the effective bobbin width, which takes into account physical bobbin width BW, margins M (all in mm), and the number of winding layers L:

$$BW_E = L \times [BW - (2 \times M)]$$

The closest standard magnet wire gauge that is less than or equal to this diameter can be selected. Determine the bare conductor diameter DIA of this wire gauge using information from a wire table. The next step is to find out if this conductor size is sufficient for the maximum I_{RMS}. The current capacity for magnet wire is specified of "Circular mile per Amp" or CMA, which is the inverse of current density:

$$CMA = \frac{1.27 \times DIA^2 \times \frac{\pi}{4}}{I_{RMS}} \times \left(\frac{1000}{25.4} \right)^2$$

If the CMA is less than 200, a larger gauge wire is needed to handle the current. This could be accommodated by adding a second layer if there is only one existing layer and/or by using a larger core/bobbin and/or smaller NP. On the other hand, a CMA greater than 500 would indicate that a smaller core/bobbin and/or larger NP could be used.

Note that in the AN-17 spreadsheet, DIA is actually derived from OD using an empirical equation. A practical wire size, AWG, is determined according to DIA. CMA is then calculated from AWG.

With the secondary RMS current ISRMS available, the minimum secondary wire diameter DIAS (in mm), can be calculated as follows:

$$DIA_S = \sqrt{\frac{4 \times CMA \times I_{SRMS}}{1.27 \times \pi}} \times \frac{25.4}{1000}$$

If the required secondary wire diameter turns out to be larger than that of the AWG #26 wire size which corresponds to twice the skin depth at 100 kHz, a parallel configuration of windings using a gauge equal to or smaller than 26 AWG should be used to provide the same effective cross sectional area. The parallel windings must have identical number of turns equal to N_S. For example, if the equation above indicates a 23 AWG wire, a winding consisting of N_S turns of two parallel strands of 26 AWG will be a good choice.

Note that if triple insulated wire is to be used for secondary, the insulated wire diameter is actually larger than DIA_S by twice the thickness of the insulator. Therefore, the maximum outside diameter ODS (in mm) must be calculated:

$$OD_S = \frac{BW - (2 \times M)}{N_S}$$

A triple insulated wire should be specified with a conductor diameter equal to or greater than DIA_S and insulated outside diameter equal to or less than OD_S.

As can be seen from steps 11 to 13, the transformer design is a highly iterative process in itself. When N_P is changed, N_S and N_B will change according to ratios already established. Similarly, any change in core size requires a recalculation of CMA, B_M and L_g to make sure that they are within the specified limits. Table 23 shows the relation and effect upon varying the number of layers (L), secondary number of turns (N_S) and Core/Bobbin.

		B_M	L_G	(CMA)
L	↑	–	–	↑
N_S	↑	↓	↑	↓
Core Size	↑	↓	↑	↑

Table 23. Iteration Relation of L, N_S and Core.

Step 14 – Determine Output Short-Circuit Current I_{OS}

- Calculate maximum output short-circuit current I_{OS} from I'_P and N_P/N_S, where I'_P is the maximum I_{LIMIT} from LinkSwitch-XT2 data sheet and NP/NS is the turns ratio from Step 11.

$$I_{OS} = I'_P \times \frac{N_P}{N_S} \times k$$

Where k is the peak RMS current conversion factor.

- The value of k is determined based on empirical measurements: k = 0.9 for Schottky diode and k = 0.8 for PN junction diode.
- Check I_{OS} against diode current rating I_D. If necessary, choose higher current diode.

Step 15 – Select Output Capacitor

ESR is the most important parameter for output filter capacitor selection. Capacitor ESR directly determines the output ripple voltage of the power supply and the ripple current rating of the capacitor. In general, selecting a high ripple current rated capacitor results in an acceptable value of ESR.

$$ESR = \frac{V_{RIPPLE}}{I_{SP}}$$

Ripple current is typically specified at 105 ºC ambient which is much higher than the ambient temperature required in most applications. Therefore, it is possible to operate the capacitor at higher ripple currents determined by a multiplier factor from the capacitor data sheet.

Actual ripple current of the capacitor can be calculated as follows:

$$I_{RIPPLE} = \sqrt{I_{SRMS}^2 - I_O^2}$$

Where I_{SRMS} is the secondary winding RMS current and I_O is the DC output current.

- Choose output capacitor with RMS current rating equal to or larger than output ripple current.
- Use low ESR electrolytic capacitor rated for switching power supply use.
- Example are KZH series from UCC, UHD or UHW series from Nichicon, and EEU series from Panasonic.

The actual output capacitance value is of secondary importance. As long as the capacitance contribution is negligible to the ripple. And this will hold as true by following the selected actual capacitance value as reflected by the equation below for C_{OUT}:

$$C_{OUT} >> \frac{I_{OUT} \times D_{MAX}}{V_{RIPPLE} \times f_{SW}}$$

Where,
C_{OUT} is the actual capacitance value.
I_{OUT} is the DC output current.
D_{MAX} is the maximum duty cycle.
V_{RIPPLE} is the required ripple voltage of the output.
f_{SW} is the switching frequency of operation of the power supply.

Step 16 – **Select Output Post Filter**
If the measured switching ripple voltage at the output capacitor is higher than the required specification, an LC post filter consisting of a 2.2 to 4.7 µH inductor or ferrite bead (only for output current < 1 A) with a low ESR electrolytic capacitor is recommended. This will provide a lower cost solution compared to increasing the capacitance value and/or lowering the ESR of the main output filter capacitor.

Step 17 – **Select Bias Rectifier**
Bias rectifier selection is similar to output rectifier selection with the exception that since the bias winding carries very little current (typically less than 10 mA). The considerations for current capacity and very fast recovery no longer apply.

The peak inverse voltage across the bias rectifier diode is given by:

$$PIV_B = V_B + \left(V_{MAX} \times \frac{N_B}{N_P} \right)$$

Step 18 – **Select Bridge Rectifier Based on Input Voltage V_{ACMAX} and Input RMS Current I_{ACRMS}**
Maximum operating current for the input bridge rectifier occurs at low line:

$$I_{ACRMS} = \frac{P_O}{\eta \times V_{ACMIN} \times PF}$$

PF is the power factor of the power supply. Typically, for a power supply with a capacitor input filter, PF is between 0.5 and 0.7. Use 0.5 if there is no better reference data available.

Select the bridge rectifier such that:

- $I_D > 2 \times I_{ACRMS}$, where I_D is the rated RMS current of the bridge rectifier.
- $V_R > 1.25 \times 1.414 \times V_{ACMAX}$; where VR is the rated reverse voltage of the rectifier diode.

Step 19 – **Design complete for Continuous Current Mode (CCM) Operation of Flyback Power Supply**

II. Discontinuous Mode Operation

This section is dedicated for the step by step procedure for design implementing discontinuous mode operation.

Step 1 – **Follow the Step 1 to 6 Procedures From Part I of In-depth Information**

Step 2 – **Determine Primary Peak Current I_P. Calculate Maximum Duty Cycle D_{MAX} for Discontinuous Mode of Operation Based on V_{MIN}, P_O and I_P**

- Primary peak current is 90% of minimum I_{LIMIT} from the data sheet of the selected LinkSwitch-XT2. $I_P = 0.9 \times I_{LIMIT}$ minimum.
- Calculate maximum duty cycle D_{MAX} for discontinuous mode of operation as:

$$D_{MAX} = \frac{2 \times P_O}{\eta \times V_{MIN} \times I_P}$$

Step 3 – **Calculate K_{DP} from V_{MIN}, V_{OR} and D_{MAX}**
In Discontinuous Current Mode or DCM operation, the secondary current is zero when the MOSFET turns on. Figure 17 illustrates the primary drain current and secondary rectifier currents in DCM operation.

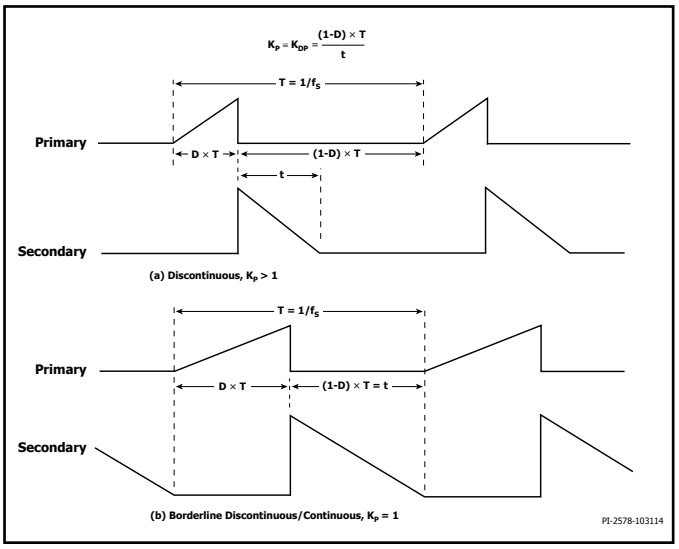


Figure 17. Primary Drain and Secondary Rectifier Current in DCM Operation.

- K_{DP} is the ratio between the off-time of the switch and the reset time of the core:

$$K_{DP} = \frac{V_{OR} \times (1 - D_{MAX})}{V_{MIN} \times D_{MAX}}$$

Step 4 – **Check K_{DP} to Ensure Discontinuous Mode of Operation**
With discontinuous mode of operation, generally, the output filter is smaller, output rectifier is inexpensive using a PN junction diode, EMI and noise are lower.

Fully discontinuous mode of operation (discontinuous under all conditions) may be necessary in some applications to meet specific requirements such in very low output ripple voltage. Use of RC snubber, and/or PN junction diode as output rectifier also demand full discontinuous mode of operation. This can be accomplished by raising VOR higher if necessary. To keep the worst-case drain voltage below recommended level of 725 V for LinkSwitch-XT2 device, V_{OR} should be kept below 135 V.

Mostly discontinuous mode of operation ($K_{DP} > 1$) refers to a design in discontinuous mode under most situations, but do have the possibility of operating in continuous mode occasionally.

Continuous mode operation ($K_{DP} < 1$) provides higher output power. In this mode a Schottky output diode should be used to prevent longer diode reverse recovery time that could exceed leading edge blanking period (t_{LEB}).

Step 5. Check for Fully Discontinuous Operation
$K_{DP} > (1 – D_{MAX}) / (0.67 – D_{MAX})$: Fully discontinuous.

0.67 is the reciprocal of the percentage of duty cycle relaxation caused by various parameters such as the tolerance in LinkSwitch-XT2 current limit and frequency.

Recalculate VOR as:

$$V_{OR} = \frac{K_{DP} \times V_{MIN} \times D_{MAX}}{1 - D_{MAX}}$$

- If V_{OR} < 135 V, go to Step 6.
- If V_{OR} > 135 V, go back to first section of the In-depth Information Step 5 and select higher current LinkSwitch-XT2.

Step 6 – Calculate Primary Inductance LP for Discontinuous Mode

$$L_P = \frac{2 \times P_O \times [Z \times (1 - \eta) + \eta]}{\eta \times f_S \times I_P^2}$$

Where:
I_P is the minimum I_{LIMIT} from LinkSwitch-XT2 data sheet.
f_S is minimum switching frequency from LinkSwitch-XT2 data sheet.
Please note the cancellation effect between the over temperature variations of I_P and f_S resulting in the additional 1/0.9 term.
Z is loss allocation factor. If Z = 0, all losses are on the primary side. If Z = 1, all losses are on the secondary-side. If no reference, Z = 0.5 is a reasonable staring point.

Step 7 – Transformer Design

Transformer design steps done on continuous mode operation is also applicable for DCM. For Step 7, transformer design for discontinuous mode operation, Step 11 of Part I design equations and procedures will be applied.

Step 8 – Calculate Primary RMS Current I_{RMS} and Secondary RMS Current I_{SRMS}

Discontinuous Mode:

- Calculate primary RMS current I_{RMS}.

$$I_{RMS} = \sqrt{D_{MAX} \times \frac{I'^2_P}{3}}$$

Where I'_P equals to maximum I_{LIMIT}.

- Calculate secondary RMS current I_{SRMS}.

$$I_{SRMS} = I_{SP} \times \sqrt{\frac{1 - D_{MAX}}{3 \times K_{DP}}}$$

Where $I_{SP} = I'_P \times [N_P/N_S]$ and $I'_P = I_{LIMITMAX}$.

- Choose wire gauge for primary and secondary windings based on I_{RMS} and I_{SRMS}.
- In some designs, a lower gauge (larger diameter) wire may be necessary to maintain transformer temperature within acceptable limits during continuous short circuit conditions.
- Do not use wire thinner than 36 AWG to prevent excessive winding capacitance and to improve manufacturability.

Step 9 – Determine Wire Gauge Both on Primary and Secondary

Wire gauge calculation both on primary and secondary steps in Part I is also applicable for discontinuous mode. For Step 9 of discontinuous mode, design equations and procedures on Step 12 of Part I will be applied.

Step 10 – Determine Output Short-Circuit Current I_{os} and Selection of Output Capacitor (C_{OUT}), Output Post Filter, Bias Rectifier and Bridge Rectifier

The calculation and selection of other design parameters such as output short circuit (I_{OS}), output capacitor (C_{OUT}), output post filter, bias rectifier and bridge rectifier had the same calculations as in Part I. For Step 10 of discontinuous mode operation, the Steps 14 to 18 of Part I design equations and procedures will be applied.

Step 11 – Design Complete for Discontinuous Current Mode (DCM) Operation of Flyback Power Supply

Appendix C – Protection Feature for Flyback Applications

Hysteretic Output Overvoltage Protection

In flyback topology, the output overvoltage protection provided by the LinkSwitch-XT2 IC uses auto-restart that is triggered by a current $>I_{BP(SD)}$ into the BYPASS pin. To prevent inadvertent triggering of this feature, in addition to an internal filter, the BYPASS pin capacitor provides external filtering. For the bypass capacitor to be effective as a high frequency filter, the capacitor should be located as close as possible to the SOURCE and BYPASS pins of the device.

The OVP function can be realized in a non-isolated flyback converter by connecting a Zener diode from the output to the BYPASS pin. The circuit example shown in Figure 18 describes a simple method for implementing the output overvoltage protection. Additional filtering for the OVP detection feature, can be achieved by inserting a low value (10 Ω to 47 Ω) resistor in series with the OVP Zener diode. The resistor in series with the OVP Zener diode also limits the maximum current into the BYPASS pin. The current should be limited to less than 16 mA.

During a fault condition resulting from loss of feedback, the output voltage will rapidly rise above the nominal voltage. A voltage at the output that exceeds the sum of the voltage rating of the Zener diode and the BYPASS pin voltage will cause a current in excess of $I_{BP(SD)}$ injected into the BYPASS pin, which will trigger the auto-restart and protect the power supply from overvoltage.

Line Overvoltage Protection

In a flyback converter configuration, during the power MOSFET on-time, the LinkSwitch-XT2 IC can sense indirectly the DC bus overvoltage condition by monitoring the current flowing into the FEEDBACK pin depending on circuit configuration. Figure 19 shows one possible circuit implementation. During the power MOSFET on-time, the voltage across the secondary winding is proportional to the voltage across the primary winding. The current flowing through emitter and base of transistor Q3 is therefore directly proportional to the VBUS voltage.

$$V_{PRI} = V_{BUS} - V_{DS} \quad \text{(D1)}$$

V_{DS} is much smaller compared to the bus voltage which can be neglected.

The voltage across the secondary winding is proportional to the voltage across the primary winding.

$$V_{SEC} = \frac{V_{PRI}}{\eta} \quad \text{(D2)}$$

$$-V_{BP} + V_{Q3(EB)} + V_{D3} + V_{VR3} + V_{R3} = V_{SEC} \quad \text{(D3)}$$

The voltage across the Zener diode VR3 is therefore dependent on VBUS. When the line voltage is higher than its threshold and the Zener diode VR3 is turned on, transistor Q3 is turned on and current will flow into FEEDBACK pin from the BYPASS pin capacitor through transistor Q3. When the fed current is higher than FEEDBACK pin

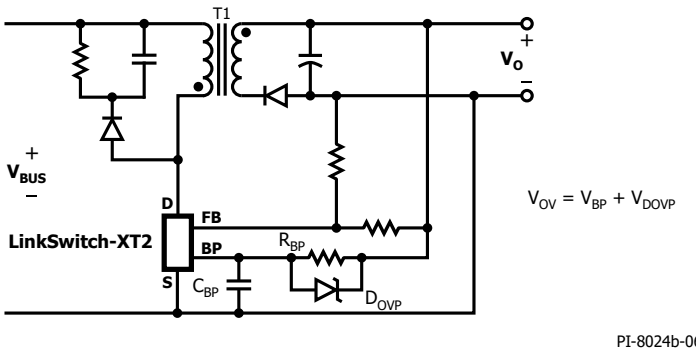


Figure 18. Non-Isolated Flyback Converter with Output Overvoltage Protection.

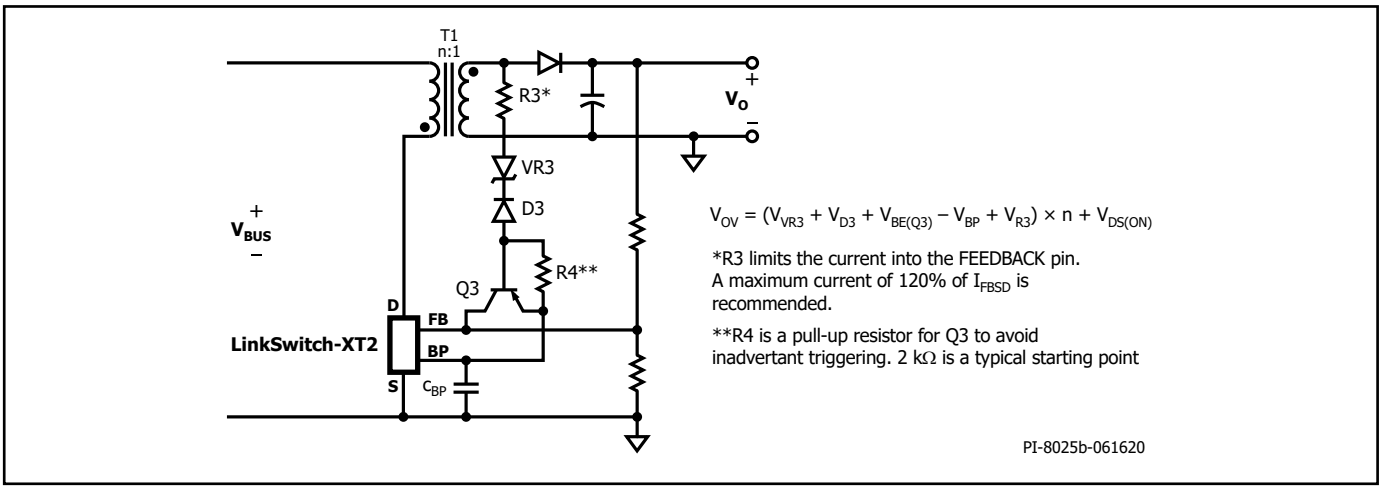


Figure 19. Line-Sensing for Overvoltage Protection by using FEEDBACK Pin.

instant shutdown current $I_{FB(SD)}$ for at least 2 consecutive switching cycles, the line overvoltage protection will be triggered and the LinkSwitch-XT2 IC will go into auto-restart mode.

The threshold for the bus overvoltage is:

$$V_{OV} = (-V_{BP} + V_{Q3(EB)} + V_{D3} + V_{VR3} + V_{R3}) \times \eta + V_{DS} \quad (D4)$$

Indirect line sensing minimizes power dissipation otherwise incurred in a typical primary side line overvoltage detection circuit.

Resistor R4 is used as a weak pull-down resistor to help avoid inadvertent conduction of Q3 during normal operation. A 2 kΩ resistor can be used for R4. Based on the selection of the Zener diode and transistor, the value of R4 may need to be adjusted. R3 is used to limit the current into the FEEDBACK pin. The current through resistor R3 is equal to the sum of current through R4 and current through emitter and base of Q3, which is:

$$I_{R3} = I_{Q3(EB)} + I_{R4} \quad (D5)$$

From equation D4:

$$I_{R3} = \frac{V_{R3}}{R3} = \frac{\frac{(V_{BUS} - V_{DS})}{N} + V_{BP} - V_{Q3(EB)} - V_{DS} - V_{VR3}}{R_3} \quad (D6)$$

And

$$I_{R4} = \frac{V_{BE(Q3)}}{R_4} \quad (D7)$$

From equation D6 and D7:

$$I_{Q3(EB)} = \frac{\frac{(V_{BUS} - V_{DS})}{N} + V_{BP} - V_{Q3(BE)} - V_{D3}}{R3} - \frac{V_{BE(Q3)}}{R4} \quad (D8)$$

The current of $I_{Q3(EC)}$ should not exceed 120% of $I_{FB(SD)}$ in order to limit the current into the FEEDBACK pin.

$$I_{Q3(EC)} = h_{FE} \times I_{Q3(EB)} = h_{FE} \times \left[\frac{\frac{(V_{BUS} - V_{DS})}{N} + V_{BP} - V_{Q3(BE)} - V_{D3} - V_{VR3}}{R3} - \frac{V_{BE(Q3)}}{R4}\right] \quad (D9)$$

In order to have accurate line OV threshold voltage and also for good efficiency, regulation performance and stability, the transformer leakage inductance should be minimized. Low leakage will minimize ringing on the secondary winding and provide accurate line OVP detection. The current into the FEEDBACK pin is sampled and compared to $I_{FB(SD)}$ typically 280 ns after the high-voltage power MOSFET is turned on.

In some designs if the ringing at the secondary winding is longer than 280 ns, a RC snubber across the rectifier diode may be needed to damp the ringing to ensure precise detection of line voltage.

Below is an example with 33 V Zener (VR3) BZX74-C33, and the threshold is at 308 V. When the bus voltage is higher than the threshold, the power supply goes into auto-restart. The first time a fault is asserted the off-time is 150 ms ($t_{AR(OFF)}$ – first off period). If the fault condition persists, subsequent off-times are 1500 ms long ($t_{AR(OFF)}$ subsequent periods).

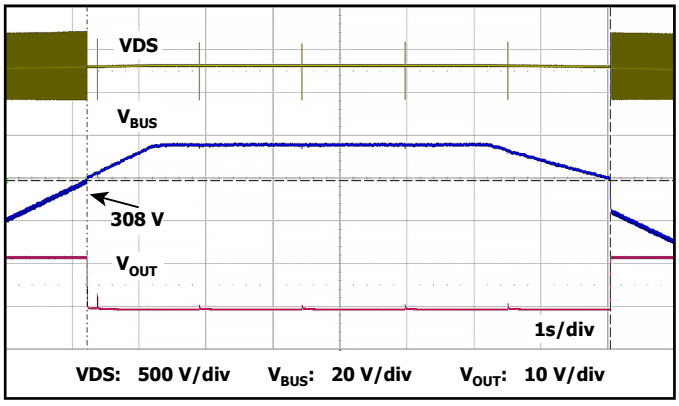


Figure 20. Indirect Line-Sensing for Overvoltage Protection Result.

Revision	Notes	Date
A	Initial release.	09/20

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